Power consumption of LVPECL and LVDS

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Introduction
Single-ended emitter-coupled logic (ECL) has been in existence for over 30 years and is a proven high-speed technology. More recently, differential ECL has been introduced along with the variants of positive ECL (PECL) and low-voltage PECL (LVPECL). The common feature of all these devices is high signaling rates. ECL and its variants use bipolar technology to obtain these high data rates. The major benefit of bipolar technology is the relatively constant consumption of power over frequency, while a major cost of bipolar technology is the required termination.

Even more recent than the introduction of differential ECL is the TIA/EIA-644 introduction of LVDS. While the standard does not specify a technology, CMOS and BiCMOS are common implementations. CMOS technology is often generalized as being low-power and low-speed. While it is true that the power consumption of CMOS devices increases linearly with speed,1,2 new technologies using LinBiCMOS, such as the Texas Instruments LVDS product line, provide the benefits of both high speed and low power consumption.

Power definition
Power, in the context of this document, is broken down into categories of external, drive circuit, and logic power, as shown in Figure 1. The external power consumption is simply the power consumed in the external termination. The drive circuit power is dissipated within the device and is a function of the output currents and the voltage drop across the driver circuit. The logic power is best described as the switch and bias power required by the IC.

The following discussion presents a theoretical approach to calculating the quiescent power dissipation for each of the categories. The devices being compared are LVPECL 1 to 10, LVDS 1 to 8 (SN65LVDS108), and LVDS 1 to 16 (SN65LVDS116) channel repeaters. Table 1 shows the values provided in the data sheets for the LVPECL and LVDS devices.

Table 1. Data sheet power consumption

<table>
<thead>
<tr>
<th></th>
<th>LVPECL</th>
<th>LVPECL</th>
<th>SN65LVDS108</th>
<th>SN65LVDS116</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>2.5 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>$V_{EE}$</td>
<td>GND</td>
<td>GND</td>
<td>NA*</td>
<td>NA*</td>
</tr>
<tr>
<td>$I_{EE}$ (typical)</td>
<td>100 mA</td>
<td>100 mA</td>
<td>NA*</td>
<td>NA*</td>
</tr>
<tr>
<td>$I_{CC}$ (typical)</td>
<td>Not given**</td>
<td>Not given**</td>
<td>62 mA</td>
<td>80 mA</td>
</tr>
<tr>
<td>Power</td>
<td>250 mW</td>
<td>330 mW</td>
<td>204.8 mW</td>
<td>264 mW</td>
</tr>
</tbody>
</table>

* NA = Not applicable, $V_{EE}$ and $I_{EE}$ are defined only on the LVPECL data sheet.
** $I_{CC}$ is not provided in the LVPECL data sheet.

Logic power dissipation
The logic power dissipation includes quiescent and active power. The bipolar device consumes a significant amount of quiescent power but almost no active power; that is to say, the power consumption is expected to be constant over frequency. In contrast, the BiCMOS device consumes very little quiescent power, but more power is consumed as the frequency increases. Since no real insight is given about the bias structures or the switching nodes for either device, the 250 and 330 mW calculated from the LVPECL device parameters represents the quiescent logic power dissipation. This assumption is made because only $I_{EE}$ is provided in the LVPECL parameters and not $I_{CC}$. The LVDS logic power is calculated by subtracting the drive circuit and external power from the total quiescent power dissipation of 205 mW and 264 mW in Table 1.

Continued on next page
Drive circuit dissipation
The drive circuit power consumption does not include power dissipated in the line or the termination. The active components of the circuit driver are also difficult to calculate from the data sheet. However, by using Figure 1 and Equations 1 and 2 (pp. 49 and 51 in Reference 2), the amount of quiescent power consumed in the output structures for both the LVDS and LVPECL repeaters can be calculated. Table 2 lists the output specifications and the calculated drive circuit dissipation.

Table 2. Theoretical quiescent power consumption of driver circuit

<table>
<thead>
<tr>
<th></th>
<th>LVPECL 1:10</th>
<th>LVPECL 1:10</th>
<th>SN65LVDS108</th>
<th>SN65LVDS116</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>2.5 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>R1</td>
<td>50 Ω</td>
<td>50 Ω</td>
<td>50 Ω</td>
<td>50 Ω</td>
</tr>
<tr>
<td>VOH (typical)</td>
<td>1.48 V</td>
<td>2.28 V</td>
<td>1.41 V</td>
<td>1.41 V</td>
</tr>
<tr>
<td>VOL (typical)</td>
<td>0.68 V</td>
<td>1.48 V</td>
<td>1.09 V</td>
<td>1.09 V</td>
</tr>
<tr>
<td>VTERM (VCC–2 V)</td>
<td>0 V*</td>
<td>1.3 V*</td>
<td>NA**</td>
<td>NA**</td>
</tr>
<tr>
<td>Power/channel</td>
<td>54.9 mW</td>
<td>26.5 mW</td>
<td>9.55 mW</td>
<td>9.55 mW</td>
</tr>
<tr>
<td>Number of channels</td>
<td>10</td>
<td>10</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>Total power</td>
<td>549 mW</td>
<td>265 mW</td>
<td>76.4 mW</td>
<td>152.8 mW</td>
</tr>
</tbody>
</table>

* VTERM is the recommended data sheet value.
** NA = Not applicable. No termination voltage is required for LVDS.

External power dissipation
The external power consumption is assumed to have no active component, and any capacitive effects are negligible. The power loss through the media to the load is also considered to be negligible. Therefore, the only source of power dissipation is in the load and termination voltage. Table 3 shows the external power consumption obtained from Equations 3 and 4.

Table 3. Calculated external power consumption

<table>
<thead>
<tr>
<th></th>
<th>LVPECL 1:10</th>
<th>LVPECL 1:10</th>
<th>SN65LVDS108</th>
<th>SN65LVDS116</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>2.5 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Power/channel</td>
<td>53.1 mW</td>
<td>50.0 mW</td>
<td>1.156 mW</td>
<td>1.156 mW</td>
</tr>
<tr>
<td>Number of channels</td>
<td>10</td>
<td>10</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>Total power</td>
<td>531 mW</td>
<td>500 mW</td>
<td>9.25 mW</td>
<td>18.5 mW</td>
</tr>
</tbody>
</table>

\[
P_{ECL} = (V_{CC} - V_{OH})(V_{OH} - V_{TERM}) + (V_{OC} - V_{OL})(V_{OL} - V_{TERM}) \div R1 \tag{1}
\]

\[
P_{LVDS} = R_B \times I^2 + R_A \times I^2 \tag{2}
\]

\[
I = \frac{(V_{OH} - V_{OL})}{2 \times R1}
\]

\[
R_B = \frac{(V_{CC} - V_{OH})}{I}; \quad R_A = \frac{(V_{OL} - V_{GND})}{I}
\]

\[
V_{GND} = 0 \text{ V}
\]

\[
P_{ECL} = \frac{(V_{OH} - V_{TERM})^2}{R1} + \frac{(V_{OL} - V_{TERM})^2}{R1} + V_{TERM} \left[ \frac{(V_{OH} - V_{TERM})}{R1} + \frac{(V_{OH} - V_{TERM})}{R1} \right] \tag{3}
\]

\[
P_{LVDS} = \frac{(V_{OH} - V_{OL})^2}{2 \times R1} \tag{4}
\]
Expected power dissipation of the LVPECL 1:10 repeater and LVDS repeaters

Figure 2 combines the quiescent power calculated from Tables 2 and 3 and uses the quiescent logic power of the LVPECL device and the total quiescent power of the LVDS devices in Table 1. The quiescent power consumption for the LVPECL device is much greater than that for the LVDS devices, even when only a 2.5-V VCC is used. The only caveat is that this is quiescent power. While this is not significant for the bipolar LVPECL device, it is very significant for the CMOS devices, since the power consumption increases as a function of frequency. Figure 3 shows the expected power consumption of the three devices over frequency and extrapolated beyond the 622 Mbps maximum of the LVDS devices. The data over frequency is taken from the SN65LVDS108 and SN65LVDS116 data sheets, and the LVPECL device is assumed to be constant with no active power dissipation over frequency. With the data sheet values, the LVDS repeaters have an obvious power advantage over the LVPECL repeaters.

Conclusion

Actual results of the SN65LVDS116 and the LVPECL repeater are presented in Reference 5. The variances in the LVDS measurements with the expected values in Figure 3 are attributed to differences in the loads used; the values in Figure 3 are taken from the SN65LVDS116 and SN65LVDS108 data sheets, where the loads have a capacitive component. The differences between expected and measured values for the 2.5-V and 3.3-V LVPECL are 9.8% and 4.8%, respectively. While there is a variance between the results in Figure 3 and the actual measurements, the trends are the same and the LVDS device provides low-power performance over the LVPECL from 50 to 600 Mbps operation.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace “litnumber” with the TI Lit. # for the materials listed below.

Document Title

Related Web sites
www.ti.com/sc/docs/products/analog/sn65lvds108.html
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