Low-cost, minimum-size solution for powering future-generation Celeron™-type processors with peak currents up to 26 A

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Introduction

Next-generation microprocessors continue to challenge power system designers by increasing system power consumption. The latest design guidelines from Intel (Reference 4) require a maximum core current of up to 26 A for future processors in a PGA-370 package. The new TPS5211EVM-154 evaluation module with the TPS5211 hysteretic controller has been designed as a low-cost, minimum-size solution for this application. The TPS5211EVM-154 evaluation module includes a synchronous DC-DC buck converter, a socket for a PGA-370 microprocessor package with high-frequency decoupling capacitors, and a load-current transient tester. This module is a high-current modification of the TPS5210EVM-147 that is described in Reference 2. The DC-DC converter has a 5-V input and 1.65-V output and requires a 12-V, 40-mA supply voltage for the controller itself. The DC-DC converter occupies only 3.7 sq. in., while the temperature of the components does not exceed 80°C at room ambient temperature with a load current of 22 A. The transient characteristics of the module have been tested by Voltage Transient Test Tool v.2.0 from Intel and by an internal load-current transient tester at a peak load current of 26 A. A four-layer PCB, which is a very popular solution for a desktop main-board, was used in the module to get electrical and temperature conditions close to real conditions.

TPS5211EVM-154 evaluation module description

The TPS5211EVM-154 evaluation module (5.67″ x 3.19″ x 0.8″) includes three main parts:

• synchronous DC-DC buck converter,

• socket for a PGA-370 package, allowing use of the Transient Test Tool, and

• additional internal transient tester, which can be used if the Transient Test Tool is not available.

The schematic of the DC-DC synchronous buck converter is shown in Figure 1. The input filter includes four

Figure 1. Synchronous DC-DC buck converter schematic

For this application, R5, R6, and R12 are open; and R1 and R3 are 3 Mohm.
10SP470M capacitors (C1–C4), 10-µF ceramic capacitors (C5, C78), and a 1-µH inductor (L1). The input capacitors can handle a total maximum RMS current as high as 18 A to increase the reliability of the power supply. The output filter has four OS-CON type capacitors 4SP560M (C6–C9) and a 1-µH inductor (L2). The fast hysteretic controller and active droop compensation reduce the number of capacitors while having a reliable margin for dynamic tolerance.

The power stage includes two 10-mohm high-side FETs (MTD3302) and two 7-mohm low-side FETs (SUD50N03) in DPAK packages (Q1, Q2, Q3, and Q5). The surface mount heat sinks from AAVID (part number 573100) have been used to improve temperature characteristics. All functions and features of the TPS5211 hysteretic controller are described in References 1–3.

**Test results**

The simplified block diagram of the test set-up and the EVM itself are shown in Figure 2. All measurements were made at room temperature. The electrical and mechanical characteristics of the DC-DC converter are shown in Table 1.

### Table 1. Electrical and mechanical characteristics of the DC-DC converter

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>MEASUREMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>5 V ± 0.5 V</td>
</tr>
<tr>
<td>Input current</td>
<td>12 A max at $V_{in} = 4.5$ V and $I_{out} = 27.5$ A</td>
</tr>
<tr>
<td>$V_{CC}$ voltage and current</td>
<td>12 V ± 0.6 V, 40 mA max</td>
</tr>
<tr>
<td>Nominal output voltage</td>
<td>1.65 V</td>
</tr>
<tr>
<td>DC and peak output current</td>
<td>22-A DC for temperature measurements and 26-A peak</td>
</tr>
<tr>
<td>Output voltage static tolerance</td>
<td>+0% and –3.65% including droop compensation</td>
</tr>
<tr>
<td>Output voltage dynamic tolerance</td>
<td>+3% and –4.8% at 25-A load-current step with 20-A/µs slew rate</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>120 to 145 kHz</td>
</tr>
<tr>
<td>Efficiency</td>
<td>&gt;84% at 22 A, 53.8% at 0.5 A</td>
</tr>
<tr>
<td>Occupied area</td>
<td>3.7 sq. in.</td>
</tr>
</tbody>
</table>

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Efficiency, power losses and temperature through components

The temperatures of components, the efficiency, and power losses were measured after 2 hours of operation when the temperatures of the PCB and components were stabilized. Results of these measurements are presented in Table 2 and Figure 3. The measurements were made at room temperature (22.8°C) with 5-V input voltage and 22-A load current. The cooling conditions were natural air convection in accordance with the specification. The two surface-mount heat sinks from AAVID (part number 573100) have been used for each pair of high- and low-side FETs to improve temperature characteristics. The maximum temperature rise was 56.7°C through the high-side FET, while the temperature rise of the PCB itself was 28.8°C. These are reasonable values because the real motherboard has a much larger cooling area for the components.

One can see that the temperatures of most components are very close to the PCB temperature, except for the FETs and output inductor.

Efficiency at 22.5-A load current is 83.7% and at 0.5 A is 53.8%. This exceeds the specification, which requires 80% and 40%, respectively. The maximum power losses at 22.5-A load current do not exceed 7.1 W.

The electrical requirements and cooling conditions might vary for different applications. To cover more potential applications, the power losses, efficiency, and temperature through high-side FETs have been investigated for different FETs and switching frequencies with and without heat sinks. Results of this investigation are presented in Table 3.

The switching frequency can be decreased using lower ESR (equivalent series resistance) capacitors like OS-CON type 4SP820M or by changing resistor R14 from 51 ohms to 75 ohms. In this case, the hysteresis window increases proportionally.

Table 2. Temperature measurement results

<table>
<thead>
<tr>
<th>COMPONENT</th>
<th>PCB</th>
<th>Q1/05 HIGH-SIDE FETs</th>
<th>Q2/03 LOW-SIDE FETs</th>
<th>L1, INPUT IND.</th>
<th>L2, OUTPUT IND.</th>
<th>U1, IC</th>
<th>INPUT CAPACITORS</th>
<th>OUTPUT CAPACITORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temp. (°C)</td>
<td>51.6</td>
<td>78.5/79.5</td>
<td>66.3/70</td>
<td>47</td>
<td>62.3</td>
<td>45</td>
<td>47.8</td>
<td>46.2</td>
</tr>
<tr>
<td>Temp. rise (°C)</td>
<td>28.8</td>
<td>55.7/56.7</td>
<td>43.5/47.2</td>
<td>24.2</td>
<td>39.5</td>
<td>23.2</td>
<td>25</td>
<td>23.4</td>
</tr>
</tbody>
</table>

Table 3. Power losses, efficiency, and high-side FETs temperature for different FETs and frequencies with and without heat sinks.

<table>
<thead>
<tr>
<th>FETs, HIGH-LOW-SIDE</th>
<th>F_sw (kHz)</th>
<th>P_loss (W)</th>
<th>EFF (%)</th>
<th>HEAT SINK (With/Without)</th>
<th>TEMPERATURE OF HIGH-SIDE FETs (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MTD3302/SUD50N03-7</td>
<td>130</td>
<td>6.62</td>
<td>84.2</td>
<td>With</td>
<td>With 79.5</td>
</tr>
<tr>
<td>MTD3302/SUD50N03-7</td>
<td>87</td>
<td>6.24</td>
<td>84.9</td>
<td>Without</td>
<td>Without 88</td>
</tr>
<tr>
<td>SUD50N03-7/SUD50N03-7</td>
<td>85</td>
<td>6.32</td>
<td>84.8</td>
<td>Without</td>
<td>Without 89</td>
</tr>
<tr>
<td>PSMN005-25D/PSMN005-25D</td>
<td>88</td>
<td>5.97</td>
<td>85.5</td>
<td>Without</td>
<td>Without 82</td>
</tr>
</tbody>
</table>

Figure 3. Efficiency (a) and power losses (b) over entire input voltage and output current range.
Load-current transient response
The transient tests using the Voltage Transient Test Tool v.2.0 from Intel have been performed in accordance with the corresponding manual from Intel. The output-voltage transient waveforms during the load-current transitions are shown in Figure 4. The Test Tool was connected to the TPS5211EVM-154 evaluation module through the PGA-370 socket. The transient waveforms were measured near the output filter (TP1 on TPS5211EVM-154 module) and through the special test points J5–J7, J6–J8, and J2–J4 of the Test Tool, which are located at the microprocessor side of the PGA-370 connector.

The tests were made under the following conditions in accordance with VRM 8.4 requirements: \( I_{CC} \) bias = 2.15 A, \( I_{CC} \) max = 26 A, slew rate = 22.1 A/µs, transient duty cycle = 0.5, and transient frequency = 5.5 kHz. The peak-to-peak output voltage amplitude is 150 mV in the worst case with four OS-CON capacitors 4SP560M. The specification limit is 210 mV for this test.

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**Figure 4. The output-voltage transient response with the Intel Transient Test Tool at transient frequency 5.5 kHz**

The cursors show the output voltage limits for this test: 1.52 V minimum and 1.73 V maximum. Ch2 shows the output voltage (50 mV/div.), and Ch1 shows the drain-source voltage (5 V/div.).
Continued from previous page

The output-voltage transient response using the internal load-current transient tester is shown in Figure 5. The load-current transition was between 2.2 A and 27.2 A, which corresponds to a 25-A step load. The peak-to-peak output-voltage amplitude for this test is 130 mV, which is also well below the allowable maximum of 210 mV.

Conclusions

• The TPS5211EVM-154 evaluation module with the TPS5211 hysteretic controller meets the electrical requirements set forth in Reference 4.
• The load-current transient testing using the internal EVM transient tester and the Voltage Transient Test Tool v.2.0 from Intel have shown excellent dynamic characteristics of the TPS5211 hysteretic controller for up to 26-A core current desktop applications with the minimum number of bulk OS-CON capacitors.
• The component temperature measurements in worst-case cooling conditions have given reasonable results.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace “lit number” with the TI Lit. # for the materials listed below.

<table>
<thead>
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<th>Document Title</th>
<th>TI Lit. #</th>
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</thead>
<tbody>
<tr>
<td>1. “TPS5211 High Frequency Programmable Synchronous Buck Regulator Controller,” September 1999 ..........................</td>
<td>slvs243</td>
</tr>
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</table>

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www.ti.com/sc/docs/tools/analog/powermanagementdevelopmentboards.html
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