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Clamp function of high-speed ADC THS1041

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Introduction
The THS1041 from Texas Instruments (TI) is a 10-bit, 40-MSPS, CMOS high-speed analog-to-digital converter (ADC). It has many good features, including a single 3-V supply, low power, a flexible input configuration, a built-in programmable gain amplifier (PGA), and a built-in clamp function. Because of these features, especially the built-in clamp function, the THS1041 has been used in various applications for many years. The clamp function enables the device to generate and output a buffered dc voltage for flexible ADC applications—for example, to provide a common-mode voltage for the ADC or to allow dc restoration on an ac-coupled video signal at the ADC analog input. This function can be enabled or disabled. As shown in Figure 1, the THS1041 clamp function consists of an on-chip digital-to-analog converter (DAC), logic control, a clamp input, a buffer, and a clamp output. The clamp output can be a continuous or interrupted dc signal depending on whether its Clamp pin receives a dc or pulse signal from an external source. When this interrupted dc signal is applied to the ADC single-ended (SE) input circuit to provide common-mode voltage, the dc stability at the ADC analog input becomes a concern. Some users have questioned dc stability when the clamp function and SE input configuration are applied at the same time. This article presents some test data that explains how the dc voltage behaves in this kind of application condition and how to get the best ADC performance when the clamp function is on.

Clamp function
Figure 1 shows that the THS1041 clamp function is implemented by setting four pins—Clampin, Clampout, Clamp, and Mode—as well as the device internal registers. With on-chip DAC, digital data from the THS1041 internal register written by data bus b0 to b9 can be converted into an analog dc voltage. This dc voltage is then buffered and output to Clampout through internal switches. The internal switch between the buffer and DAC can be on or off depending on how the register is set. The DAC can provide different dc voltages with a range between reference voltages REF+ and REF− for different application needs. Setting different voltage levels at the Mode pin permits the input of the internal buffer to also simply be connected to an internal fixed dc voltage or to Clampin for an external dc voltage input. The Clampout pin can be connected to or disconnected from the buffer output of the clamp function by controlling either the dc or the pulse signal on the Clamp pin. The THS1041 clamp function can be on with an ADC differential input or SE input configuration. Its output from Clampout can be connected to both analog inputs, AIN+ and AIN−, to provide common-mode voltage, or to only one of them for other applications.

Figure 1. THS1041 clamp function block diagram

![THS1041 clamp function block diagram](image-url)
Figure 2 shows a fundamental configuration of the THS1041 with the clamp function at the SE input. Setting Mode as \( AV_{DD}/2 \) puts the device in an internal reference mode; and dc voltage at Clampout is from Clampin, not an internal DAC. The output of the clamp function, Clampout, is connected to AIN+ and also to a capacitor C2 through a small resistor R for a clamp pulse control application. Capacitor C2 is used to hold dc voltage when Clampout is disconnected internally during the clamp pulse interval. It is also used to couple ac signals from the source to AIN+. Another ADC analog input, AIN–, is connected to an external dc source and should have the same dc voltage as AIN+ for normal operation. The Clamp pin controls the internal switch between Clampout and the buffer output. When Clamp is logic high, Clampout is internally connected to the buffer output; and when Clamp is logic low, Clampout is disconnected from the buffer output.

Testing dc behavior with clamp dc control

Clamp dc control means adding a dc signal at the Clamp pin to control the Clampout pin’s access to the internal buffer. To see dc behavior at AIN+ and AIN– when the clamp function is on, two different dc voltages are added to AIN+ and AIN–, and the logic level at Clamp is controlled manually. Based on the configuration in Figure 2, V2 is set at 1.5 V at Clampin, V1 is set at 1 V at AIN–, C2 is 0.6 \( \mu \)F, and R is 10 \( \Omega \). No ac signal is added to analog input AIN+ in this case. The ADC clock is running at 40 MHz. When Clamp is manually set to logic high (3 VDC), the AIN+ is stable at 1.5 V; and when Clamp is set to logic low (0 VDC), the AIN+ is stable at 1 V. In other words, when the Clamp pin is logic high, the voltage at AIN+ is driven by an internal buffer; and when the Clamp pin is logic low, AIN+ is disconnected from the buffer and its voltage drifts toward the voltage at AIN–. On the other hand, if AIN– is floating, then the voltage at AIN– follows the voltage at AIN+. The dc voltages at AIN+ and AIN– drift toward each other after their voltage sources are disconnected. This is because significant charge or discharge occurs internally between the sampling capacitors in the ADC’s sample-and-hold circuit during the hold phases after many clock cycles. The test data is shown in Tables 1 and 2.

The test data in Tables 1 and 2, measured when the ADC clock was active, shows that disconnecting the analog input pins from the source makes their dc voltages affect each other. When the ADC clock is not running, the dc voltages at AIN+ and AIN– drift toward each other because significant charge or discharge occurs internally between the sampling capacitors in the ADC’s sample-and-hold circuit during the hold phases after many clock cycles. The test data is shown in Tables 1 and 2.

Table 1. Analog input dc voltage when clock is active and AIN– is connected to dc supply

<table>
<thead>
<tr>
<th>Clamp Logic</th>
<th>Clampin (connected to dc supply) (V)</th>
<th>AIN– (connected to dc supply) (V)</th>
<th>AIN+ (charged or discharged based on Clamp logic) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>1.5</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>High</td>
<td>1.5</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>Low</td>
<td>1.5</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 2. Analog input dc voltage when clock is active and AIN– is floating

<table>
<thead>
<tr>
<th>Clamp Logic</th>
<th>Clampin (connected to dc supply) (V)</th>
<th>AIN– (charged or discharged) (V)</th>
<th>AIN+ (charged or discharged based on Clamp logic) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>High</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>Low</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
voltages at AIN+ and AIN– don’t affect each other (see Tables 3 and 4). In addition, whether or not capacitor C2 is used does not affect the dc voltage test result but does affect the transition time of the voltage change at AIN+.

### Table 3. Analog input dc voltage when clock is not active

<table>
<thead>
<tr>
<th>Clamp Logic</th>
<th>Clampin (connected to dc supply) (V)</th>
<th>AIN– (connected to dc supply) (V)</th>
<th>AIN+ (charged or discharged based on Clamp logic) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>1.5</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>High</td>
<td>1.5</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>Low</td>
<td>1.5</td>
<td>1</td>
<td>0*</td>
</tr>
</tbody>
</table>

*Discharge slowly

### Table 4. Analog input dc voltage when clock is not active and AIN– is floating

<table>
<thead>
<tr>
<th>Clamp Logic</th>
<th>Clampin (connected to dc supply) (V)</th>
<th>AIN– (charged or discharged) (V)</th>
<th>AIN+ (charged or discharged) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>1.5</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>High</td>
<td>1.5</td>
<td>0</td>
<td>1.5</td>
</tr>
<tr>
<td>Low</td>
<td>1.5</td>
<td>0</td>
<td>0*</td>
</tr>
</tbody>
</table>

*Discharge slowly

**Testing dc behavior with clamp pulse control**

Clamp pulse control means adding a pulse signal at the Clamp pin to control the Clampout pin’s access to the internal buffer. To observe dc behavior at the THS1041 analog input, a pulse signal instead of a dc signal is added to the Clamp pin with a frequency of 16 kHz and a duty cycle of 6% (see Figure 2). Similar to the previous test, a fixed dc voltage of 1 V from a well decoupled supply is added to Clampin, and a variable dc voltage is added to AIN–. In this case, AIN+ is driven to 1 V by the internal buffer during the clamp pulse and is well maintained at that level by capacitor C2 during the clamp pulse interval when AIN– is 1 V. The capacitance C2 must be large enough and the clamp pulse interval short enough to keep the dc voltage at AIN+ the same level as the dc voltage at Clampin. However, the dc signal will be distorted if the dc offset at AIN– is set differently from AIN+. As mentioned earlier, the dc voltages at the analog input pins can drift when one pin or the other is floating. The test with clamp pulse control further proves this statement. The dc drift appears as a voltage spike when a pulse is applied to the Clamp pin, and this is observed by oscilloscope as shown in Figure 3.

The spike periodically appears at AIN+ at clamp pulse frequency, and its amplitude increases as the dc voltage difference between the analog input pins increases. The test data shows that when Clampin is connected to a 1-V supply and AIN– is connected to a 0.5-V supply, the dc measurement at AIN+ is 1 V during the clamp pulse logic high and low. The ac measurement at AIN+ is a positive spike at about 20 mV and appears when the clamp pulse transitions from low to high. When AIN– is connected to a 1.5-V supply and Clampin is still connected to a 1-V supply, the dc measurement at AIN+ is 1 V. The ac measurement at AIN+ is a negative spike at about 30 mV and appears when the clamp pulse transitions from low to high. When AIN– is connected to a 1-V supply, the same as the dc voltage at AIN+, the spike disappears and the 1-V dc voltage at AIN+ is smooth and stable.

Further testing shows that the spike gets smaller when the duty cycle of the clamp pulse goes higher. Adding a capacitor C3 at the Clampout pin will significantly limit the spike.

**THS1041 ac performance with clamp pulse control**

The spike at analog input AIN+ can degrade the ac performance of the THS1041 (see Figures 4 and 5 and Table 5). Figures 4 and 5 are FFT plots of the THS1041 with clamp pulse control and different dc voltage conditions on the analog input pins. The FFT plots are generated from a Labview FFT program based on the data captured from the THS1041 EVM by an HP1600 logic analyzer. The test signal at the analog input of the EVM is a 2.2-MHz sine wave with an amplitude of –20 dBFS (20 dB below the ADC’s full scale). It is generated from an HP8644 sine-wave generator and received by the SE input of the THS1041 through an onboard transformer. (Detailed settings of the EVM board for this test are described later in this article.) A pulse generator triggered by the HP8644 is running the THS1041 input clock at 40 MHz. The clamp pulse is generated from a pulse generator with a frequency of 15.6 kHz and a 50% duty cycle.

In frequency domain the spike appears periodically at clamp pulse frequency as shown in Figure 3. In frequency domain the spike appears at 15.6 kHz (the low end of the frequency axis) on the FFT. When the dc voltage difference at the analog input pins is 0.5 V (AIN+ is 1 V and AIN– is 0.5 V), the spike at 15.6 kHz is –67 dBFS, the largest spike in the
FFT (see Figure 4). This spike is much higher than any harmonic on the FFT and contributes to the spurious-free dynamic range (SFDR) with a low value. When the dc voltage difference is zero (AIN+ and AIN− are 1 V), the spike at the same frequency is –82 dBFS, a 15-dB improvement (see Figure 5). This spike is lower than the second and third harmonics and lower than the total harmonic distortion (THD).

Figures 4 and 5 show that with the dc voltage difference between AIN+ and AIN− increasing to a certain degree, the SFDR decreases and could be significantly worse than the THD if the input analog signal was small. This would
be especially true if the decoupling capacitance C3 at 
Clampout (see Figure 2) was not large enough. Based on 
these test results, a further test was conducted with a 
different decoupling capacitance at Clampout. With an 
analog input amplitude of –21 dBFS (21 dB below the 2-V 
full-scale input of the THS1041), a C3 value of 0.4 µF, and 
a dc voltage difference between AIN+ and AIN– of 0.5 V, 
the SFDR is about 16 dB worse than the THD. At the 
same value of C3, the SFDR is 3 dB worse than the THD 
when the dc voltage difference between AIN+ and AIN– is 
decreased to 0 V. If C3 is increased to 1.4 µF, the overall 
ac performance—including the SFDR, THD, and signal-to-
noise ratio (SNR)—improves significantly. In this case 
the SFDR is about 5 dB better than the THD when the dc 
input amplitude between AIN+ and AIN– is zero, and about 
6 dB worse than the THD when the dc voltage difference 
is 0.5 V. The test data is shown in Table 5.

<table>
<thead>
<tr>
<th>AIN+ (V)</th>
<th>AIN– (V)</th>
<th>SFDR Relative to THD (C3 = 0.4 µF) (dB)</th>
<th>SFDR Relative to THD (C3 = 1.4 µF) (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5</td>
<td>–16</td>
<td>–6</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>–3</td>
<td>5</td>
</tr>
<tr>
<td>1</td>
<td>1.5</td>
<td>–17</td>
<td>–5</td>
</tr>
</tbody>
</table>

The test data shows that the dc voltage differences 
between AIN+ and AIN– cause not only a spike at the 
analog input but also early output saturation, therefore 
decreasing the maximum analog input amplitude. For 
example, when the dc voltage difference between AIN+ 
and AIN– is 0.5 V with AIN+ at 1 V, the maximum analog 
input amplitude has to be 20 dB below full scale to avoid 
output saturation. When the dc voltage difference is 0.3 V 
with AIN+ at 1 V, the maximum analog input amplitude is 
3.5 dB below full scale. So the dc voltage at AIN+ and 
AIN– should be the same as the dc voltage at AIN+ with an SE 
input configuration. Adding different dc voltages to AIN+ 
and AIN– can cause a spike at the analog input when the 
clamp function is on and a pulse signal is applied to Clamp. 
The higher the dc voltage difference between analog inputs 
AIN+ and AIN–, the larger the spike. The spike also gets 
worse if the duty cycle of the clamp pulse is decreased. 
This is because the dc voltages at AIN+ and AIN– drift 
toward each other after their external voltage sources are 
disconnected. In this case the charge or discharge occurs 
internally between the sampling capacitors in the ADC’s 
sample-and-hold circuit during the hold phases. The dc 
input amplitude between AIN+ and AIN– also causes 
early output saturation and degrades the maximum analog 
input amplitude, so the difference should be limited. 
Increasing decoupling capacitance at Clampout will mini-
nize the spike, increase dc voltage difference tolerance at 
the analog input, and improve overall THS1041 ac perfor-
mane. This conclusion is based on the THS1041 bench test. 
The observation and test method in this article are also 
helpful for other high-speed ADCs.

References
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2. “THS1040/41 Evaluation Module for the 
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