High-Performance Analog Products

Analog Applications Journal

Third Quarter, 2008

© Copyright 2008 Texas Instruments
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI’s standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

**Products**
- Amplifiers: [amplifier.ti.com](http://amplifier.ti.com)
- Data Converters: [dataconverter.ti.com](http://dataconverter.ti.com)
- DSP: [dsp.ti.com](http://dsp.ti.com)
- Interface: [interface.ti.com](http://interface.ti.com)
- Logic: [logic.ti.com](http://logic.ti.com)
- Power Management: [power.ti.com](http://power.ti.com)
- Microcontrollers: [microcontroller.ti.com](http://microcontroller.ti.com)

**Applications**
- Audio: [www.ti.com/audio](http://www.ti.com/audio)
- Automotive: [www.ti.com/automotive](http://www.ti.com/automotive)
- Broadband: [www.ti.com/broadband](http://www.ti.com/broadband)
- Digital control: [www.ti.com/digitalcontrol](http://www.ti.com/digitalcontrol)
- Military: [www.ti.com/military](http://www.ti.com/military)
- Telephony: [www.ti.com/telephony](http://www.ti.com/telephony)
- Video & Imaging: [www.ti.com/video](http://www.ti.com/video)
- Wireless: [www.ti.com/wireless](http://www.ti.com/wireless)

Mailing Address: Texas Instruments
Post Office Box 655303
Dallas, Texas 75265
Contents

Introduction .............................................................................................................. 4

Data Acquisition
A DAC for all precision occasions ................................................................. 5
Applications such as automatic test equipment, instrumentation, portable equipment, and digitally controlled calibration need precision digital-to-analog converters (DACs) to convert digital data back into the analog domain. This article describes three of the DAC topologies that achieve this task: the R-2R MDAC, R-2R back-DAC, and the string DAC.

Power Management
New current-mode PWM controllers support boost, flyback, SEPIC, and LED-driver applications ................................................................. 9
This article provides an overview on how the TPS40210/1 PWM controllers support isolated and non-isolated power converters used in industrial, automotive, and battery-powered applications. Advanced features such as programmable soft start, adjustable/synchronizable oscillator frequency, internal slope compensation, and the flexibility to provide different power levels by simply changing the power stage gives these controllers universal appeal.

Interface (Data Transmission)
When good grounds turn bad—isolate! ............................................................ 11
Industrial communication systems often require long transmission lines. This article will help designers be more aware of how large ground-potential differences (GPDs) between remote bus locations can compromise the integrity of the transmission signal, which can lead to system lockup and, at worst, destroy the bus transceivers.

Cascading of input serializers boosts channel density for digital inputs ............ 16
Traditional parallel interface to analog I/O devices typically required bulky components, many isolation channels, and a large-footprint host controller which limited channel density and subject to significant power dissipation. TI’s SN66HV88x devices serializes inputs into a single SPI data stream and reduces the number of isolators by 50% and power dissipation by more than 75%.

Amplifiers: Op Amps
A new filter topology for analog high-pass filters .......................................... 18
Nearly all common high-pass filter topologies include capacitors in the forward signal path. The venerable "servo" feedback technique instead uses an integrator in the feedback path of a gain block to create a first-order high-pass filter. A new topology is described which extends this technique to second-order filters and beyond. Both techniques allow the designer to add circuitry "wrapped around" another circuit to add a high-pass function without changing the circuit in the forward path.

Index of Articles.................................................................................................. 25

TI Worldwide Technical Support ...................................................................... 29

To view past issues of the Analog Applications Journal, visit the Web site
www.ti.com/aa
Introduction

*Analog Applications Journal* is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as “how-to” instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.
A DAC for all precision occasions

By Bonnie C. Baker, Senior Applications Engineer

Introduction
Analog-to-digital converters (ADC) routinely convert analog signals such as temperature, pressure, sound, or images to a precise digital representation. Microcontrollers and microprocessors store, massage, and transmit this digital information throughout a system. There are also times when precision digital-to-analog converters (DAC) convert the digital representation of these real-world events back into the analog domain. Three of the DAC topologies that achieve this feat are the R-2R MDAC, R-2R back-DAC, and the string DAC. These three topologies service applications such as automatic test equipment, instrumentation, portable equipment, and digitally controlled calibration.

The R-2R MDAC
Automatic test equipment or instrumentation typically uses the R-2R multiplying DAC (MDAC, Figure 1). The external operational amplifier augments the DAC function by providing the opportunity for differing supply voltages and high output currents. MDAC manufacturers are able to design high resolution devices (16 bit) with ±1 LSB integral non-linearity (INL) and differential non-linearity (DNL) specifications. With an appropriate external amplifier, the MDAC exhibits fast settling time (< 0.3 ms) with a multiplying bandwidth that can be greater than 10 MHz.

The MDAC generates a current that is proportional to an input digital code. The external amplifier, along with RFB (internal in the MDAC), converts the DAC’s current-output signal to a usable voltage level. It would seem that a simple current-to-voltage conversion is easy to implement with a DAC, an amplifier, and a resistor. However, this application circuit has a set of stability issues.

The output model of the MDAC contains a current source, variable resistor, and variable capacitor (Figure 2a). The output resistance and capacitance of the MDAC is dependent on the input code to the DAC. Programming the MDAC to zero causes the output resistance (RD) to be near infinite. If you program the MDAC to full scale or all ones, RD is equal to RFB. The output capacitance (CD) changes according to the number of internal gate-source junctions across the MDAC output. At full scale, the MDAC output capacitance is equal to the data sheet specification. When programmed to zero scale, the MDAC output capacitance is equal to approximately half the full-scale value. As we calculate the worst-case stability condition, we will use the full-scale output values of RD and CD.

To maintain precision, most MDACs have a feedback resistor (RFB) on-chip. The feedback capacitor, CF, is external and discrete. The unity gain bandwidth (fU) of

Figure 1. An R-2R multiplying DAC

Figure 2a. MDAC model
the operational amplifier, as well as the input-differential capacitance \( (C_{DIF}) \) and common-mode capacitance \( (C_{CM}) \), directly affect the stability of this circuit.

At the input of the amplifier, the total capacitance in this system is equal to \( C_{IN} = C_{D} + C_{DIF} + C_{CM} \). The pole and zero in the feedback loop of the amplifier are equal to (see Figure 2b and c):

\[
\begin{align*}
\frac{1}{f_1} &= \frac{1}{2\pi(C_{IN} + C_F) \times (R_D || R_P)} \quad \text{[feedback circuit zero]} \\
\frac{1}{f_2} &= \frac{1}{2\pi(C_{IN} + C_F)} \quad \text{[feedback circuit pole]}
\end{align*}
\]

You determine the system stability by keeping the difference of the rate of change of the operational amplifier open-loop gain curve and the closed-loop gain curve at 20 dB/decade. You can do this by selecting an amplifier with unity gain bandwidth \( (f_U) \) less than \( f_1 \) or higher than \( f_2 \) (Figure 2b and c).

From here, it is easy to design a stable circuit. If \( f_1 \) is higher than the unity gain crossing of the amplifier \( f_U \), the following formula applies to this design.

\[
C_P \geq \frac{1 + \sqrt{1 + 8\pi C_{IN} R_F f_U}}{2\pi R_F f_U}
\]

If \( f_2 \) is lower than the intersection of the open-loop gain curve and the closed-loop gain curve, use this formula.

\[
C_F \leq \frac{1}{2\pi(R_D || R_P) f_U} - C_{IN}
\]

These calculated values of \( C_F \) are a starting point. As you test your circuit, parasitics, device manufacturing variations, etc. can prompt you to modify the value of \( C_F \).

Making the MDAC analog voltage signal stable is critical. However, there are other issues to take into account. At the risk of covering this topic too briefly, consider issues such as amplifier noise, input bias current, and offset voltage, as well as MDAC resolution and glitch energy.

The MDAC is a low-noise solution for a variety of applications. The voltage-reference, current-output change with digital codes to the MDAC is constant. The trade-off for this advantage is varying ground currents with digital input codes. Typically, you will find MDACs in digital gain and attenuation control circuits as well as waveform generators.

**The R-2R back-DAC**

You usually use the R-2R back-DAC (Figure 3) in industrial applications. Some other applications for the R-2R back-DAC include instrumentation and digitally controlled calibration. With the R-2R back-DAC, each new update switches the 2R legs to either the voltage reference high (VREF-H) or the voltage reference low (VREF-L). Notice that the arrangement of the R-2R ladder is upside down as compared to the MDAC. This is where the name “back-DAC” came from. This architecture is simple to manufacture, assuming the resistors for each current source can be properly adjusted.

Gate-switch timing skews manifest themselves at the output of the MDAC and back-DAC as glitches. The glitch is most prevalent during the MSB transition, when bits are...
switching from 7FFFh to 8000h (for a 16-bit DAC). The R-2R back-DAC, like the MDAC, typically has excellent low noise, INL, and DNL performance, with medium settling-time capability.

DAC glitches result from capacitive-charge injection from the internal, asynchronous gate switching. The DAC glitch for R-2R DACs typically has two lobes (Figure 4a), while string topologies typically have a single-lobe glitch impulse (Figure 4b).

The units of a glitch impulse is volts/seconds. Glitch impulses are most dramatic between consecutive codes where a major code transition occurs. In Figure 4a the total glitch impulse equals $G_2$ minus $G_1$, where $G_1$ and $G_2$ are the calculated areas. In Figure 4b the total glitch impulse equals the shaded area of $G_1$. In most systems, you can ignore the glitches that occur at the output of a DAC during code transition; however, in a control loop, glitches are typically undesirable. In a control system, the DAC glitch impulse from a one-bit code transition, where the MSB is switching, confuses the loop by momentarily sending an erroneous output-voltage signal.

The glitch-impulse area in Figure 4a occurs during the DAC’s output-voltage transition region as it switches from one code to another. As the 16-bit DAC switches from 8000h to 7FFFh (or half the full-scale output voltage), the output glitch impulse becomes noticeable to the extent that it appears as if the DAC is momentarily non-monotonic. Secondary glitches occur around the one-fourth full-scale and three-fourths full-scale voltages. If the control system is fast enough to respond to this glitch, the circuit may oscillate.

You can try to reduce the impact of this glitch impulse by using a low-pass filter at the output of the DAC. However, while a low-pass filter reduces the glitch-impulse amplitude, it increases the glitch time. For example, consider a glitch-impulse response of the 16-bit DAC is equal to 96 nV-s, with a peak voltage of 60 mV and duration of 1.6 µs. You can filter that glitch impulse so that the peak voltage is 30 mV with duration of 3.2 µs. You can also add sampling circuitry on the output of the DAC and time it with DAC conversions. This technique may work for lower resolution, slow DACs; however, the sampling mechanism may create more problems by adding to the analog errors and conversion time. The best way to overcome larger glitch impulses is to select a string DAC with lower glitch-impulse errors from the start.

The R-2R back-DAC has medium settling time capability; however, you can build high-performance circuits with its superior INL and DNL performance. Texas Instruments achieves higher accuracy specifications with final test trimming. The R-2R ladder also facilitates low-noise performance from the DAC.

### String DAC topology

The string DAC is best suited for portable instrumentation, closed-loop servo control, and process control. Figure 5 shows a model of a 3-bit string DAC. In this figure, the digital input code 101b is decoded to 5/8 $V_{REF}$. The string DAC’s output-stage amplifier isolates the internal resistive elements from output loads. The string DAC is a low-power solution that guarantees monotonicity.

**Figure 4a. Glitch impulse of a DAC producing two regions of code transition error**

**Figure 4b. Glitch impulse of DAC producing one region of overshoot**

**Figure 5. String DAC topology**
with good DNL performance across the entire input code range. The glitch energy is typically lower than other types of DACs; however, the INL performance is generally larger and dependent on resistive, on-chip matching. On the other hand, a DAC in a control loop lessens the impact of high linearity. The noise of string DACs is also relatively high because of the resistive string-array impedance.

The string DAC operates with low power and very low glitch energy. An on-chip output buffer simplifies the interface to this device.

**DAC calibration**

With any of the three DACs in this article, you may see a need to calibrate the analog output for higher precision results. If you calibrate any DAC, you initially determine the code-to-voltage error at one-third of the output range and again at two-thirds of the output range. The range between one-third full scale (FS) and two-thirds FS avoids the output amplifier errors near the power supply rails. You achieve the calibration of the offset and gain errors with the formula \( V_{OUT} = a + bV_{IN} \) (“a” is the offset error and “b” is the gain error). You can calibrate your DAC in the digital domain with the help of an ADC that is more accurate than the target specifications of a DAC.

A more challenging DAC calibration activity is to adjust the linearity of the converter’s entire output range. Once again, you will require an ADC that has four times the resolution of the DAC. You can calibrate every DAC code with 8, 10, or 12 bits of resolution. In this environment there are fewer DAC codes to calibrate and the memory requirements are lower. The accuracy of the calibrating low-bit ADC is not as demanding, allowing faster ADC conversion times. For DACs with resolution of 14+ bits, the total number of codes becomes unmanageable in terms of processor memory. Additionally, you will need to use a slower ADC with higher accuracy, such as a delta-sigma converter. Higher cost and slower speeds will encourage you to consider alternative DAC calibration strategies.

An effective alternative to linearizing every DAC code is to select several small groups of codes. The plot in Figure 6a shows an example of the integral non-linearity of a 16-bit string DAC. The universal formula for calculating any DAC correction code is

\[
DAC_{COR} = INL_v + (INL_v - INL_w) \times \frac{x - w}{v - w},
\]

where \( INL_v \) and \( INL_w \) are the INL error of the v and w code, x is a code between codes v and w. If (v – w) is equal to an integer that is a power of two, you can implement the division with right shifts, reducing the processor calculation time and complexity. Figure 6b illustrates the benefit of this linearization technique using 1024 code groupings, 64 codes per group.

This technique is best suited for DACs that are monotonic, with INL error in excess of ±8 LSB. Additionally, you must exercise care when selecting the size of the code sets. If there are large, sudden jumps from one code to the next, as may be with R-2R architectures, this technique may prove to be counterproductive instead of an improvement in DAC performance. The string DAC topology is best suited for this calibration technique because it is inherently monotonic (a requirement for this technique) and jumps from one code to the next are relatively small as compared to other DAC topologies.

**Conclusion**

A precision DAC uses a limited number of discrete digital input codes to produce a corresponding number of discrete analog output values. For a DAC, 1 LSB corresponds to the height of a step between successive analog outputs, with the value defined in the same way as for the ADC. The MDAC, R-2R back-DAC, and string DAC architectures do not encompass all of the possible DAC topologies, but if you know about these topologies you will have a good start on knowing the basics.

**Related Web sites**

dataconverter.ti.com
New current-mode PWM controllers support boost, flyback, SEPIC and LED-driver applications

By Jürgen Schneider, Systems Engineer Power Solutions

Introduction
With their wide input voltage range, the TPS40210 and TPS40211 PWM controllers are targeted for isolated and non-isolated power converters used in industrial, automotive, and battery-powered applications. The full freedom in selecting the power stage and its compensation—as well as the advanced features, such as programmable soft start, adjustable/synchronizable oscillator frequency and internal slope compensation—supports the use of the devices in many applications. The basic converter architecture can provide different power levels by simply changing the power stage. While the TPS40210 is designed for general-purpose applications, the TPS40211 is tailored for driving high-brightness LEDs.

Boost converter application
The devices and their basic configuration are described in detail in Reference 1.

SEPIC converter application
The SEPIC-converter shown in Figure 1 allows the input voltage to be smaller, larger, or equal to the targeted output voltage. The topology requires two single inductors or one coupled inductor, L1, and a capacitor C9, which is responsible for the energy transfer. The filter formed by L2 and C11 is optional. It reduces the output ripple voltage to 50 mV_{p-p} in the example shown. When operating the converter at 1 MHz, the size of the power stage (inductors/capacitors) can be minimized. However, due to the increased switching loss at this high frequency, a greater than 1-A continuous output current requires Q1 to be mounted on a heat sink. Operation without a heat sink is possible at a reduced switching frequency and/or reduced maximum input voltage.

With a 2-A current output and a 1-MHz switching frequency, converter efficiency was measured as follows: 90% with a 12-V source, 88% with a 24-V source, and 85% with a 36-V source.

Figure 1. SEPIC 1-MHz converter with 8- to 36-V input and 12-V/3-A output

Features

- Input voltage: 4.5 to 52 V
- Current-mode architecture
- Switching frequency: 35-kHz to 1-MHz (programmable and synchronizable)
- Programmable soft start (closed loop)
- Reference voltage: 700 mV for TPS40210 and 260 mV for TPS40211
- Internal slope compensation
- Threshold for overcurrent detection: 150 mV
- Internal 8-V regulator and N-channel MOSFET driver
- Quiescent current when disabled: 10 µA
- MSOP10 PowerPAD™ and 3-mm x 3-mm SON package
Flyback converter application

Figure 2 shows the TPS40210 controller configured in a flyback-converter topology for a dual-output isolated supply. Key components include the transformer (T1), the snubbers (R5, C7, D1, R8, C9, R10, R11, C12 and C13), the optocoupler (U2), the secondary-side reference and error amplifier (U3), the bias resistor (R15) belonging to U3, the loop compensation (C19, C20 and R16), the output-voltage divider (R17 and R18), and the secondary-side soft-start and overshoot control (D5, R14 and C18). The circuit shown directly controls the positive output rail (VOUT+) only. Negative-rail regulation is based on the cross regulation between the two secondary windings of T1. When the negative output does not have a load, R12 and D4 provide a basic load.

High-brightness LED-driver application

DC/DC regulators are usually designed to provide a constant-voltage output; however, LED applications require a constant-current output. In Figure 3, R1 is used to sense the LED current. The losses in R1 are minimized with the TPS40211 because of its low 250-mV reference voltage. D1 protects against output overvoltage in the event of an LED-string open circuit. The brightness can be programmed by altering R1, current injection into the FB pin, or by PWM dimming. See Reference 1 for more information.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace “litnumber” with the TI Lit. # for the materials listed below.

<table>
<thead>
<tr>
<th>Document Title</th>
<th>TI Lit. #</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. “TPS40210/211” data sheet</td>
<td>slus772</td>
</tr>
</tbody>
</table>

Related device

TPS40200—4.5- to 52-V wide input range step-down converter

www.ti.com/sc/device/TPS40200

Related Web sites

power.ti.com

www.ti.com/sc/device/TPS40210
When good grounds turn bad—isolate!

By Thomas Kugelstadt
Senior Applications Engineer

Industrial communication via fieldbus-transceiver systems often requires long transmission lines. Designers, unaware of the large ground-potential differences (GPDs) between remote bus locations, either rely on the local earth ground as a reliable signal return path or directly connect remote grounds to each other—thus creating noisy ground loops. In both cases the integrity of the transmission signal is compromised, which can lead to system lockup and, at worst, destroy the bus transceivers.

To make designers aware of these design pitfalls, this article explains where GPDs originate in the electrical installation, how ground loops are created unintentionally, and how isolation circumvents both conditions to yield a robust data-transmission system.

Linking grounds
The link between the direct-current (DC) ground of a local electronic circuit and the earth reference potential of the mains is usually provided by the local power supply converting the line voltage into the required DC output. Figure 1 shows a simplified block diagram of a low-cost switched-mode power supply (SMPS) typically used in personal computers, laser printers, and other equipment. Here the DC ground of the SMPS output is referenced to the protective earth (PE) conductor of the mains via the SMPS chassis. This direct link, therefore, acts as a sense conductor, establishing the PE voltage as the local DC ground potential.

Linear and nonlinear loads
Large office and industrial buildings operate a vast number of nonlinear loads such as PCs, laser printers, solid-state heater controls, fluorescent tubes, uninterruptible power supplies, and variable-speed drives. In comparison to linear loads such as incandescent lamps, whose phase currents maintain a sinusoidal waveform, nonlinear loads distort phase currents, introducing large harmonic content (see Figure 2).

**Figure 1. Simplified block diagram of an SMPS**

**Figure 2. Distorted phase current and its frequency components**
While the third and fifth harmonics of the fundamental 60-Hz line frequency make up the lion’s share of the harmonic content, the vector sum of all frequency components (including the 60-Hz fundamental) can reach peak values that exceed the amplitude of the fundamental phase current by more than 100%.

All neutral conductors merge into one neutral conductor of large diameter within the distribution panel, running towards the transformer (Figure 5). In the case of linear loads, the neutral currents of multi-phase systems cancel each other to a certain extent. Only a fraction of the total neutral current remains due to loading imbalance (Figure 3).

For nonlinear loads, however, the individual currents add up to a total neutral current consisting primarily of third harmonics (Figure 4). The large neutral currents of nonlinear loads, therefore, cause significantly higher voltage drops across the line resistance of the electrical installation than those of linear loads.

**Earthing systems**

Most electrical installations use either the TN-C or the TN-C-S earthing system, both shown in Figure 5.

“TN” means the neutral is grounded to earth (French terre) at the transformer. The letter “C” indicates the combined use of PE and neutral lines via one conductor, designated as “PEN.” The PEN runs through the entire system up to a distribution point (i.e., a subpanel) close to the loads, where it is split into separate PE and neutral conductors that directly connect to the loads.
Although TN-C represents an old earthing system, it has regained interest because it is less costly than a system requiring an additional PE conductor. The TN-C method, however, has a major drawback. Because the split into PE and neutral lines occurs close to a load, the voltage potential at the local PE connection includes the large voltage drops across the line resistance, $R_{L-N}$, of long neutral conductors. These voltage drops are caused by high neutral currents from nonlinear loads. The TN-C system, therefore, has the potential to cause large GPDs between remote grounds in the tens of volts.

The TN-C-S system reduces GPDs by starting an extra PE conductor within the distribution panel. Additionally, the star connection of the system's neutral and PE conductors receives a second grounding to earth, reducing the equipotential at this point and counteracting the otherwise large voltage drop at the PEN across the source line resistance, $R_{LS}$.

According to the United States National Electrical Code (NEC), the PE conductor is supposed to be currentless under normal operation. However, most nonlinear loads leak currents in the lower milliamperes into the PE conductor. This amount, although small for one circuit, easily reaches amperes when hundreds of circuits contribute into the same line.

Although negligible in comparison with neutral currents, leakage currents do create potential differences between remote ground locations due to the voltage drops across the line resistance of the PE conductors. These GPDs, however, are in the millivolts range or lower and are thus significantly lower than in TN-C systems.

GPDs are not a problem for an electronic circuit limited to operation from only one local supply. GPDs do become of concern in the design of a communication link between two remote circuits (i.e., fieldbus-transceiver stations), each operating from a different supply.

**Designing a remote data link**

When designing a remote data link, the designer must assume GPDs exist. These voltages add as common-mode noise, $V_n$, to the transmitter output. Even if the total superimposed signal is within the receiver's input common-mode range, relying on the local earth ground as a reliable path for the return current remains dangerous (see Figure 6a). This applies even to “super” RS-485 transceivers such as the Texas Instruments SN65HVD2x family, whose input common-mode range stretches from $-20 \text{ V}$ to $+25 \text{ V}$.

Any modifications of the electrical installation (i.e., during regular maintenance work) are out of the designer’s control. The modifications can increase the GPD to the extent that the receiver's input common-mode range is either sporadically or permanently exceeded. Thus, a data link that works perfectly today might cease operation sometime in the future.

Removing the GPD by directly connecting remote grounds through a ground wire is also not recommended (Figure 6b). Bear in mind that the electrical installation constitutes a highly complex resistance network consisting of:

![Figure 6. Design pitfalls](image)
of multiple cross-connected line and grounding resistances caused by multiphase systems, different cable lengths, and various grounding electrode paths (Figure 7).

A direct connection between remote grounds shunts this network while creating a current loop. The initial GPD tries to compensate its collapse by driving a large loop current through the low-impedance ground wire. The loop current couples to the data-line circuit and generates noise voltage that is superimposed on the transmission (common-mode) signal. This again carries the risk of a highly unreliable data-transmission system.

To allow for a direct connection of remote grounds, the RS-485 standard recommends the separation of the device ground and the local system ground via the insertion of resistors (Figure 6c). While this approach reduces loop current, the existence of a large ground loop keeps the data link sensitive to noise generated somewhere else along the loop. Thus, a robust data link still has not yet been established. The most robust RS-485 data link over a long distance, withstanding GPDs of up to hundreds and thousands of volts, is via galvanic isolation of the signal and supply lines of a bus transceiver from its local signal and supply sources (Figure 8).

Supply isolators such as isolated DC/DC converters, and signal isolators such as digital capacitive isolators, avoid the creation of current loops and prevent current flow between remote system grounds with GPDs of up to several thousand volts.

Without a reference to ground, the bus transceivers would be operating from a floating supply. Thus, current or voltage surges caused by lightning, ground faults, or other noisy environments would be able to lift the floating bus common to dangerously high levels. These events won’t destroy components connected to the bus, as their signal and supply levels are referenced to the bus common and ride on the varying common reference potential. However, where the transmission wires connect to PCB connectors at the various transceiver nodes, the high voltages, if not removed, can lead to arcing and destroy PCB components close to the connector. To suppress current and voltage transients on the bus common, it is necessary to reference the bus common at one point to the system ground. This location usually is at a non-isolated transceiver node, which provides the single-ground reference for the entire bus system.
While Figure 8 shows the detailed connection of two remote transceiver nodes, Figure 9 shows an example of an isolated data-transmission system using multiple transceivers. Here all but one transceiver connect to the bus via isolation. The non-isolated transceiver on the left provides the single-ground reference for the entire bus.

**Conclusion**

Designing remote data links requires the isolation of supply and signal lines of fieldbus-transceiver stations to circumvent the detrimental effects of GPDs and ground loops on the signal integrity and the components.

While some of the figures in this article illustrate differential data transmission, the principles discussed also hold true for single-ended transmission systems such as the RS-232.

**Related Web site**

interface.ti.com
Cascading of input serializers boosts channel density for digital inputs

By Frank Dehmelt, Systems Engineer Analog Products

Introduction
Programmable logic controllers (PLCs) play an integral role in industrial automation. They allow inputs from digital as well as analog sensors and provide outputs to drive actuators. The digital inputs represent a significant share of those I/Os, accepting inputs from end switches, proximity switches, fuel sensors, light barriers, over-temperature sensors and many others.

The traditional approach
There are several types of digital inputs; the IEC-61131-2-standard defines those most commonly used. Traditionally, digital inputs used discrete components and required a parallel processor interface. Current limitation was achieved by a series of high-power resistors. Resistor-capacitor (RC) filters reduced bouncing of mechanical switches, while a per-channel optocoupler connected to the parallel processor interface. This design, however, requires bulky components, many isolation channels, and a large footprint host controller to allow for the parallel inputs. It also creates significant power dissipation.

With a typical resistor chain providing about 2.2 kΩ, the current at the nominal 24 V rises to 11 mA and results in power consumptions of 260 mW or 400 mW at 30 V. Considering that this dissipation may occur simultaneously for all input channels — along with the bulky components and the processor interface — it severely limits channel density.

A new approach
TI’s SN65HVS88x product family addresses these limitations and more. The digital input serializer (as the name implies) serializes the inputs into a single SPI data stream and reduces the number of isolators by 50%.

The resistors and LEDs shown in Figure 1 are required by the IEC-61131-2-standard; they can be omitted for inputs that do not require conformance with this standard. Regardless, the integrated current limit allows use of a lower power resistor.

The input current is fed to an output pin, which allows to drive an external LED to indicate the current state of the input. Without the LED, this pin simply connects to ground.

The HVS88x family allows for the cascading of several devices, all sharing the same SPI interface. For a 32-channel input, it still provides a four-channel isolation, saving 87% of ISO channels.

And what about power dissipation with a 32-channel interface? We previously calculated a worst-case dissipation of 400 mW/channel totaling almost 13 W: this is too much for a PLC slice which is about the size of a deck of cards. The HVS88x family allows the designer to set current limitation anywhere between 200 µA and 5.2 mA. For a type-1 or type-3 switch, choose a limit in the 3-mA range, limiting the per-channel dissipation to 90 mW at 30 V. This reduces power dissipation by more than 75% vs. a discrete approach.

Figure 1. 8-channel digital input using HVS882 and ISO7241
The designer can further reduce the number of external components by using the integrated debounce filter, set to filter pulses of less than 3 ms or 1 ms in duration. For the fastest acquisition of glitch-free switches, bypass the filter as well.

The parts operate from the 24-V nominal field supply and generate the internally used 5 V themselves. This supply is also available to drive external circuitry such as the field side of the isolation barrier on the SPI interface.

The HVS88x family allows high-density digital inputs by serialization, cascading, a significant reduction of power dissipation, and elimination of external components. Production material, samples, and evaluation boards are available.

### Related device
ISO721 – High-speed digital isolator
[www.ti.com/iso721](http://www.ti.com/iso721)

### Related Web sites
interface.ti.com/
[www.ti.com/sn65hvs882](http://www.ti.com/sn65hvs882)

### Table 1. The SN65HVS88x digital input serializer family digital isolator

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SN65HVS880</th>
<th>SN65HVS882</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serialization</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Cascading</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Current Limitation</td>
<td>(0.2 to 5.2 mA)</td>
<td>(0.2 to 5.2 mA)</td>
</tr>
<tr>
<td>Debounce Filter</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td>(0 ms, 1 ms, 3 ms)</td>
<td>(0 ms, 1 ms, 3 ms)</td>
</tr>
<tr>
<td>VCC</td>
<td>18 V to 30 V</td>
<td>10 V to 34 V</td>
</tr>
<tr>
<td>Undervoltage Indicator</td>
<td>Yes (~15 V)</td>
<td>No</td>
</tr>
<tr>
<td>5-V Output</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>0 V to 30 V</td>
<td>0 V to 34 V</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>–40°C to 85°C</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>Over-Temperature Protection</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

### Figure 2. Simplified 32-channel digital input with cascading, using four HVS88x serializers and one ISO7241 digital isolator
A new filter topology for analog high-pass filters

By Mark Fortunato
Analog Field Applications Manager

The analog circuit designer today has literally dozens of circuit topologies available to implement filters, from the venerable Sallen-Key (SK) filter, in use for well over fifty years,\(^1\) to more esoteric and hard-to-pronounce filters such as the Mikhail-Bhattacharyya (MB) filter or the Padukone-Mulawka-Ghausi (PMG) filter.\(^2\) Each of these filters has advantages and disadvantages relative to its cousins. Nearly all of the filter topologies used today were developed in the 1950s, ’60s, and ’70s.\(^2-6\) Can we come up with a filter topology that has an advantage over all the many topologies that have been in use for decades? For some specific needs, the new topology presented here has some unique advantages.

Almost all the common high-pass filters (HPFs) tend to have one thing in common—capacitors in series with the forward signal path. For most applications, having capacitors in the signal path is not a problem. However, there are applications where such capacitors can be problematic. For example, in broadband low-noise circuits such as many audio circuits, there is a need to keep resistance values, and thus noise, low. These applications also often call for high-pass functions that roll off at low frequencies, below 10 Hz in some audio applications. These cases can thus call for very large capacitor values. Large-value capacitors tend to be very expensive or have voltage coefficients and other non-idealities that can ruin the fidelity of the signals being passed through them.

Another limitation of the HPFs commonly used is that the entire filter circuit is implemented separately and placed either before or after another circuit functional block. Sometimes a filter in front and one after a block is needed. The technique we will discuss here allows an engineer to design a circuit without consideration of the high-pass function required. After the circuit is designed, another circuit can be “wrapped around” the original one that will cause the overall circuit to have a high-pass function without affecting the operation of the original circuit at frequencies above the high-pass rolloff.

Adding a high-pass function to block DC offsets

Figure 1 is a simplified schematic of a circuit with a gain block driving a high-order low-pass filter (LPF) in a signal-processing application. In this example there is an offset in the input signal and an offset caused by the filter, both of which must be removed. Typically a designer would place a capacitor in series with the input and the output as shown in Figure 2. For many applications this approach is just fine; but for some applications, this simple AC-coupling scheme can cause problems. Besides the reasons already
discussed, the characteristics of these high-pass stages may adversely affect the signal-processing function that is the primary purpose of the overall circuit. Each of these AC-coupling stages creates a single real (i.e., simple) pole at the frequency determined by the applicable RC time constant. Especially as the number of AC-coupling stages in the signal chain increases, the composite high-pass function is unlikely to be the optimal one for the full circuit and system. More commonly, a filter with complex pole pairs is necessary to optimize the HPF response.

**Using servo feedback rather than blocking capacitors**

In our example, let’s assume that the input signal presents the largest of the offsets and that the filter’s output offset, though small, is objectionable for the latter stages. Let’s further assume that the desirable HPF function is that of a single pole. If we eliminate the input AC-coupling filter, the output filter will certainly remove all DC offsets for the subsequent stages; but then that input offset will cause the signal applied to and processed by the filter to be significantly shifted “off center,” which can cause significant distortion.

An old technique referred to as “servo feedback” is often used in cases like this. This technique provides AC coupling, removing all offsets at the output of the circuit without putting any circuitry in series with the amplifier/filter chain of Figure 1. Servo feedback is fully covered in Reference 7.

The feedback path added in Figure 3 is an inverting integrator. The integrator output is fed to the inverting terminal of the input amplifier so that the overall loop has negative feedback. Assuming that the rolloff of the LPF is at least a decade above the desired high-pass rolloff, we can treat the LPF as a flat gain block for the purposes of calculating the high-pass response. A simple analysis shows that we have added a high-pass function with the transfer function

\[
\frac{V_{OUT}}{V_{IN}} = -G_{LPF} \frac{R_1}{R_2 + \frac{R_2 R_3 C_1}{R_1 G_{LPF}}} \left( 1 + \frac{R_2 R_3 C_1}{R_1 G_{LPF}} \right)
\]

where \( G_{LPF} \) is the absolute value of the LPF gain. \( G_{LPF} \) is a high-pass function with a 3-dB (pole) frequency of

\[
f = \frac{R_1 G_{LPF}}{2\pi R_2 R_3 C_1}
\]

Since the LPF in this circuit has a gain of -1, we get the frequency response shown in Figure 3 with a pole frequency of 15.92 Hz.

This servo technique solves the problem of putting capacitors in series with the signal path, eliminates the need for multiple high-pass stages, and allows a designer to add a high-pass function to a gain/low-pass block without modifying the block itself. However, this technique is capable of implementing only simple poles and thus does
not allow us to create complex pole pairs. Therefore we need a similar technique that will provide a complex second-order function.

**A new circuit topology implements a complex pole pair**

Figure 4 shows just such a circuit, drawn two different ways. Figure 4a shows a gain block with the frequency-dependent part of the circuit wrapped around it like the first-order servo filter discussed earlier. Figure 4a is very similar to the previous schematics except that there are two integrators in the feedback path, one of which has an added resistor included to set the Q of the second-order function. Figure 4b shows the identical circuit just shifted around to be in-line. Anyone familiar with three-op-amp biquad circuits such as the Kerwin-Huelsman-Newcomb (KHN) and Tow-Thomas (TT) filters will see a distinct similarity. In fact, this topology is the same as the TT filter except that, rather than having a resistor in parallel with \( C_1 \), it has \( R_2 \) in series with \( C_2 \).

The end result of this subtle change from the TT filter is that, whereas the TT filter implements an LPF and a band-pass filter (BPF) but no HPF, this circuit can implement an HPF and a BPF but no LPF. In our new circuit the HPF
output is the node labeled “Output” in both Figures 4 and 5. Figure 5 identifies the BPF output as “BPFOUT.”

The transfer function, pole frequency, and Q for our new HPF are respectively given by

\[
\frac{V_{OUT}}{V_{IN}} = -\frac{R_5}{R_1} \frac{S^2 C_1 C_2 R_3 R_6 R_4}{R_5} + S C_2 R_2 + 1, \tag{3}
\]

\[
f_0 = \frac{1}{2\pi \sqrt{C_1 C_2 R_3 R_6 R_4 / R_5}}, \tag{4}
\]

and

\[
Q = \frac{1}{R_2 \sqrt{R_4 R_3 R_6 C_1 / C_2}}. \tag{5}
\]

Using sensitivity analysis as covered in References 2, 5, 6, and 8, we find that, as with the KHN and TT filters, all sensitivities of \( f_0 \) or Q to the passive components are 1 or lower. It is quite difficult to get lower sensitivities.

Of course, this filter could be used as a separate filter block like any other HPF topology. In the first example given earlier, we could add a three-op-amp circuit like this to the front of the gain block/filter section and another following the filter. In this case, our new HPF topology would have no real advantage over the KHN filter, and the only
advantage it would have over any other common topology is that it can implement an HPF with no capacitors in the forward signal path.

The unique feature that this filter provides is that it is easily applied around a gain block to add a high-pass function without putting any additional circuitry in the forward signal path. Later we will see that is a variation of this circuit that works with an inverting amplifier while feeding back to the non-inverting terminal, and that there are other variations that work with non-inverting gain blocks. All of these variations feed back to only one input.

**Applying this technique to a non-inverting amplifier**

If the gain block to which we want to add a high-pass function is non-inverting, we can use the variation of the topology shown in Figure 6.

The transfer function for this circuit, Equation 6, is identical to that of the circuit in Figure 5, except that the gain term is \((R_4 + R_5)/R_4\) rather than \(-R_5/R_1\):

\[
\frac{V_{OUT}}{V_{IN}} = \frac{R_4 + R_5}{R_4} \cdot \frac{S^2C_1C_2R_3R_6R_4}{R_5} \cdot \frac{R_4}{R_5} \cdot \frac{S}{R_4 + R_5 + SC_2R_2 + 1}
\]

(6)

Since the rest of Equation 6 is the same as Equation 3, the pole frequency and Q for this HPF variation are also given by Equations 4 and 5.

**Maintaining gain-bandwidth product with an inverting amplifier**

In Figure 5 we demonstrated this filter technique for an inverting amplifier. Note that both the input signal and the feedback signal are applied to the inverting terminal via \(R_1\) and \(R_4\), respectively. While the addition of \(R_5\) to add the HPF feedback has no effect on the nominal forward gain for the gain block, it does increase the division ratio of the feedback path of the gain block from

\[
\frac{R_1}{R_1 + R_5} \quad \text{to} \quad \frac{R_1\parallel R_4}{R_1\parallel R_4 + R_5},
\]

(7)

where \(R_1\parallel R_4\) represents that \(R_1\) is parallel to \(R_4\). This change in local feedback around op amp 1 has the effect of decreasing the effective gain-bandwidth product (GBWP) of the op amp by the same amount. In our case, \(R_1 = R_4\), which means the GBWP will be decreased by 33%.

For an inverting amplifier, rather than feeding back to the inverting terminal as in Figure 5, we can feed back to the non-inverting terminal, thus avoiding decreasing the effective GBWP of the op amp. Figure 7 shows this variation.

Notice that \(R_2\) is missing in this configuration. Recall that \(R_2\) was needed to add a zero to the feedback path, which allowed the Q to be set to a reasonable value; without \(R_2\), the Q of the circuit would always be very high. In this circuit we get a zero by reconfiguring the op amp 3 stage from inverting to non-inverting. This reconfiguration was necessary to keep the feedback negative. The resulting transfer function, along with the pole frequency and Q, are respectively given by

\[
\frac{V_{OUT}}{V_{IN}} = \frac{R_5}{R_1}\cdot\frac{S^2C_1C_2R_3R_6R_4}{R_5\parallel R_1\parallel R_4 + SC_2R_2 + 1},
\]

(8)

\[
f_0 = \frac{1}{2\pi C_1C_2R_3R_6R_4},
\]

(9)

\[
Q = \frac{R_1\parallel R_3\parallel C_1}{R_1 + R_5\parallel R_6\parallel C_2}.
\]

(10)
With this configuration there is no component that can independently set the Q. Also, since \( R_1 \) and \( R_5 \) set the gain of the forward amplifier, we cannot use them to set the pole frequency or the Q. Instead, \( C_1 \), \( C_2 \), \( R_3 \), and \( R_6 \) have to be manipulated to set both the pole frequency and the Q. Fortunately, \( f_0 \) is a function of the product of these four component values, while Q is a function of the ratio of the resistors and the ratio of the capacitors. These mathematical relationships make it fairly easy to choose the right component values. We can simply set \( R_3 = R_6 \) and \( C_1 = C_2 \), then choose their values to set \( f_0 \). Then the desired Q can be set by altering the ratio of the resistors and/or the capacitors while keeping their products constant.

Implementing higher-order HPF functions

Since the new second-order filter topology and the older first-order servo technique can both be used to wrap a high-pass function around a gain block and/or an LPF function, we can use any number of these in a signal chain to create a composite HPF function of any practical order we want.

Figure 8 shows how we have created a third-order filter by combining the first-order servo feedback HPF function from Figure 5 with the second-order circuit from Figure 7.

While many DC-blocking applications can be readily handled with the insertion of capacitors in the signal path, and many others can be satisfied with older circuit topolo-

![Figure 8. Combining two sections for a third-order HPF](image-url)
gies, the first-order servo feedback HPF and the new second-order HPF we have described can provide a great advantage in some applications due to their unique features. These features include the ease of adding to gain/LPF blocks without adding circuitry in the signal path or modifying the gain/LPF blocks, and the ability to implement HPF functions without capacitors in the signal path. The combination of the two topologies provides the ability to implement HPFs of higher orders while maintaining these advantages.

References
For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/litnumber and replace “litnumber” with the TI Lit. # for the materials listed below.

Document Title TI Lit. #

Document Title TI Lit. #

Related Web site
amplifier.ti.com
Index of Articles

Data Acquisition

Aspects of data acquisition system design
Low-power data acquisition sub-system using the TI TLV1572
Evaluating operational amplifiers as input amplifiers for A-to-D converters
Precision voltage references
Techniques for sampling high-speed graphics with lower-speed A/D converters
A methodology of interfacing serial A-to-D converters to DSPs
The operation of the SAR-ADC based on charge redistribution
The design and performance of a precision voltage reference circuit for 14-bit and
16-bit A-to-D and D-to-A converters
Introduction to phase-locked loop system modeling
New DSP development environment includes data converter plug-ins
Higher data throughput for DSP analog-to-digital converters
Efficiently interfacing serial data converters to high-speed DSPs
Smallest DSP-compatible ADC provides simplest DSP interface
Hardware auto-identification and software auto-configuration for the
TLV320AIC10 DSP Codec — a “plug-and-play” algorithm
Using quad and octal ADCs in SPI mode
Building a simple data acquisition system using the TMS320C31 DSP
Using SPI synchronous communication with data converters — interfacing the
MSP430F149 and TLV5616
A/D and D/A conversion of PC graphics and component video signals, Part 1: Hardware
A/D and D/A conversion of PC graphics and component video signals, Part 2: Software
and control

Intelligent sensor system maximizes battery life: Interfacing the MSP430F123
Flash MCU, ADS7822, and TPS60311
SHDSL AFE1230 application
Synchronizing non-FIFO variations of the THS1206
Adjusting the A/D voltage reference to provide gain
MSC1210 debugging strategies for high-precision smart sensors
Using direct data transfer to maximize data acquisition throughput
Interfacing op amps and analog-to-digital converters
ADS82x ADC with non-uniform sampling clock
Calculating noise figure and third-order intercept in ADCs
Evaluation criteria for ADSL analog front end
Two-channel, 500-kSPS operation of the ADS8361
ADS809 analog-to-digital converter with large input pulse signal
Streamlining the mixed-signal path with the signal-chain-on-chip MSP430F169
Supply voltage measurement and ADC PSRR improvement in MSC12xx devices
14-bit, 125-MSPS ADS5500 evaluation
Clocking high-speed data converters
Implementation of 12-bit delta-sigma DAC with MSC12xx controller
Using resistive touch screens for human/machine interface
Simple DSP interface for ADS784x/834x ADCs
Operating multiple oversampling data converters
Low-power, high-intercept interface to the ADS5424 14-bit, 105-MSPS converter for
undersampling applications
Understanding and comparing datasheets for high-speed ADCs
Matching the noise performance of the operational amplifier to the ADC
Using the ADS8361 with the MSP430 USI port
Clamp function of high-speed ADC THS1041
Conversion latency in delta-sigma converters
Calibration in touch-screen systems
Data Acquisition (Continued)
Using a touch-screen controller’s auxiliary inputs ................................................. 4Q, 2007 ........ 5
Understanding the pen-interrupt (PENIRQ) operation of touch-screen controllers ........ 2Q, 2008 ........ 5
A DAC for all precision occasions ........................................................................... 3Q, 2008 ........ 5

Power Management
Stability analysis of low-dropout linear regulators with a PMOS pass element ................. August 1999 .... 10
Extended output voltage adjustment (0 V to 3.5 V) using the TI TPS5210 ........................... August 1999 .... 13
Migrating from the TI TL770x to the TI TLC770x ......................................................... August 1999 .... 14
TI TPS5602 for powering TIs DSP ............................................................................. November 1999 ... 8
Synchronous buck regulator design using the TI TPS5211 high-frequency hysteretic controller .............................................................................................................. November 1999 ... 10
Understanding the stable range of equivalent series resistance of an LDO regulator ........ November 1999 ... 14
Power supply solutions for TI DSPs using synchronous buck converters ....................... February 2000 .... 12
Powering Celeron-type microprocessors using TIs TPS5210 and TPS5211 controllers ........ February 2000 .... 20
Simple design of an ultra-low-ripple DC/DC boost converter with TPS60100 charge pump May 2000 ........ 11
Low-cost, minimum-size solution for powering future-generation Celeron™-type processors with peak currents up to 26 A ........................................................................... May 2000 ........ 14
Advantages of using PMOS-type low-dropout linear regulators in battery applications ........ August 2000 .... 16
Optimal output filter design for microprocessor or DSP power supply ......................... August 2000 .... 22
Understanding the load-transient response of LDOs ..................................................... November 2000 ... 19
Comparison of different power supplies for portable DSP solutions working from a single-cell battery ....................................................................................................................... November 2000 ... 24
Optimal design for an interleaved synchronous buck converter under high-slew-rate, load-current transient conditions ....................................................................................... February 2001 .... 15
48-V/48-V hot-swap applications ..................................................................................... February 2001 .... 20
Power supply solution for DDR bus termination ......................................................... July 2001 ........ 9
Runtime power control for DSPs using the TPS62000 buck converter ............................. July 2001 ........ 15
Power control design key to realizing InfinitiBand™ benefits ........................................ 1Q, 2002 ........ 10
Comparing magnetic and piezoelectric transformer approaches in CCFL applications .... 1Q, 2002 ........ 12
Why use a wall adapter for ac input power? ................................................................... 1Q, 2002 ........ 18
SWIFT™ Designer power supply design program ......................................................... 2Q, 2002 ........ 15
Optimizing the switching frequency of ADSL power supplies ..................................... 2Q, 2002 ........ 23
Powering electronics from the USB port ...................................................................... 2Q, 2002 ........ 28
Using the UCC3580-1 controller for highly efficient 3.3-V/100-W isolated supply design 4Q, 2002 ........ 8
Power conservation options with dynamic voltage scaling in portable DSP designs .......... 4Q, 2002 ........ 12
Understanding piezoelectric transformers in CCFL backlight applications 4Q, 2002 ........ 18
Load-sharing techniques: Paralleling power modules with overcurrent protection .......... 1Q, 2003 ........ 5
Using the TPS61042 white-light LED driver as a boost converter ................................... 3Q, 2003 ........ 7
A better bootstrap/bias supply circuit ......................................................................... 3Q, 2003 ........ 5
Soft-start circuits for LDO linear regulators .................................................................... 3Q, 2003 ........ 10
UCC28517 100-W PFC power converter with 12-V, 8-W bias supply, Part 1 ................. 3Q, 2003 ........ 13
UCC28517 100-W PFC power converter with 12-V, 8-W bias supply, Part 2 ................. 4Q, 2003 ........ 21
LED-driver considerations ............................................................................................ 1Q, 2004 ........ 14
Tips for successful power-up of today’s high-performance FPGAs ................................. 3Q, 2004 ........ 11
A better bootstrap/bias supply circuit ......................................................................... 1Q, 2005 ........ 33
Understanding noise in linear regulators .................................................................... 2Q, 2005 ........ 5
Understanding power supply ripple rejection in linear regulators .............................. 2Q, 2005 ........ 8
Miniature solutions for voltage isolation .................................................................... 3Q, 2005 ........ 13
New power modules improve surface-mount manufacturability ................................... 3Q, 2005 ........ 18
Li-ion switching charger integrates power FETs ........................................................... 4Q, 2005 ........ 19
TLC5940 dot correction compensates for variations in LED brightness ..................... 4Q, 2005 ........ 21
Powering today’s multi-rail FPGAs and DSPs, Part 1 ..................................................... 1Q, 2006 ........ 9
TPS70918 RF LDO supports migration to StrataFlash® Embedded Memory (P30) .......... 1Q, 2006 ........ 14
Practical considerations when designing a power supply with the TPS6211x ............... 1Q, 2006 ........ 17
TLC5940 PWM dimming provides superior color quality in LED video displays 2Q, 2006 ........ 10
Wide-input DC/DC modules offer maximum design flexibility .................................... 2Q, 2006 ........ 13
Powering today’s multi-rail FPGAs and DSPs, Part 2 ..................................................... 2Q, 2006 ........ 18
# Index of Articles

## Power Management (Continued)
- TPS61059 powers white-light LED as photoflash or movie light  
  3Q, 2006  . . . . . . . . .8  
- TPS65552A powers portable photoflash  
  3Q, 2006  . . . . . . . . .10  
- Single-chip bq2403x power-path manager charges battery while powering system  
  3Q, 2006  . . . . . . . . .12  
- Complete battery-pack design for one- or two-cell portable applications  
  3Q, 2006  . . . . . . . . .14  
- A 3-A, 1.2-V_QTH linear regulator with 80% efficiency and _i_LoST < 1 W_  
  4Q, 2006  . . . . . . . . .10  
- bq5012 single-chip, Li-ion charger and dc/dc converter for Bluetooth® headsets  
  4Q, 2006  . . . . . . . . .13  
- Fully integrated TPS6300x buck-boost converter extends Li-ion battery life  
  4Q, 2006  . . . . . . . . .15  
- Selecting the correct IC for power-supply applications  
  1Q, 2007  . . . . . . . . .5  
- LDO white-LED driver TPS7510x provides incredibly small solution size  
  1Q, 2007  . . . . . . . . .9  
- Power management for processor core voltage requirements  
  1Q, 2007  . . . . . . . . .11  
- Enhanced-safety, linear Li-ion battery charger with thermal regulation and input overvoltage protection  
  2Q, 2007  . . . . . . . . .8  
- Current balancing in four-pair, high-power PoE applications  
  2Q, 2007  . . . . . . . . .11  
- Power-management solutions for telecom systems improve performance, cost, and size  
  3Q, 2007  . . . . . . . . .10  
- TPS6108x: A boost converter with extreme versatility  
  3Q, 2007  . . . . . . . . .14  
- Get low-noise, low-ripple, high-PSRR power with the TPS717xx  
  3Q, 2007  . . . . . . . . .17  
- Simultaneous power-down sequencing with the TPS740x01 family of linear regulators  
  3Q, 2007  . . . . . . . . .20  
- Driving a WLED does not always require 4 V  
  4Q, 2007  . . . . . . . . .9  
- Host-side gas-gauge-system design considerations for single-cell handheld applications  
  4Q, 2007  . . . . . . . . .12  
- Using a buck converter in an inverting buck-boost topology  
  4Q, 2007  . . . . . . . . .16  
- Understanding output voltage limitations of DC/DC buck converters  
  2Q, 2008  . . . . . . . . .11  
-Battery-charger front-end IC improves charging-system safety  
  2Q, 2008  . . . . . . . . .14  
- New current-mode PWM controllers support boost, flyback, SEPIC, and LED-driver applications  
  3Q, 2008  . . . . . . . . .9  

## Interface (Data Transmission)
- TIA/EIA-568A Category 5 cables in low-voltage differential signaling (LVDS)  
  September 2009  . . . . .16  
- Keep an eye on the LVDS input levels  
  November 1999  . . . . .17  
- Skew definition and jitter analysis  
  February 2000  . . . . .29  
- LVDS receivers solve problems in non-LVDS applications  
  February 2000  . . . . .33  
- LVDS: The ribbon cable connection  
  May 2000  . . . . . . . . .19  
- Performance of LVDS with different cables  
  August 2000  . . . . .30  
- A statistical survey of common-mode noise  
  November 2000  . . . . .30  
- The Active Fail-Safe feature of the SN65LVDS32A  
  November 2000  . . . . .35  
- The SN65LVDS33/34 as an ECL-to-LVTTTL converter  
  July 2001  . . . . . . . . .19  
- Power consumption of LVPECL and LVDS  
  1Q, 2002  . . . . . . . . .23  
- Estimating available application power for Power-over-Ethernet applications  
  1Q, 2004  . . . . . . . . .18  
- The RS-485 unit load and maximum number of bus connections  
  1Q, 2004  . . . . . . . . .21  
- Failsafe in RS-485 data buses  
  3Q, 2004  . . . . . . . . .16  
- Maximizing signal integrity with M-LVDS backplanes  
  2Q, 2005  . . . . . . . . .11  
- Device spacing on RS-485 buses  
  2Q, 2006  . . . . . . . . .25  
- Improved CAN network security with TI’s SN65HVD1050 transceiver  
  3Q, 2006  . . . . . . . . .17  
- Detection of RS-485 signal loss  
  4Q, 2006  . . . . . . . . .18  
- Enabling high-speed USB OTG functionality on TI DSPs  
  2Q, 2007  . . . . . . . . .18  
- When good grounds turn bad—isolate!  
  3Q, 2008  . . . . . . . . .11  
- Cascading of input serializers boosts channel density for digital inputs  
  3Q, 2008  . . . . . . . . .16  

## Amplifiers: Audio
- Reducing the output filter of a Class-D amplifier  
  August 1999  . . . . .19  
- Power supply decoupling and audio signal filtering for the Class-D audio power amplifier  
  August 1999  . . . . .24  
- PCB layout for the TPA065D1x and TPA092D0x Class-D APAs  
  February 2000  . . . . .39  
- An audio circuit collection, Part 1  
  November 2000  . . . . .39  
- 1.6- to 3.6-volt BTL speaker driver reference design  
  February 2001  . . . . .23  
- Notebook computer upgrade path for audio power amplifiers  
  February 2001  . . . . .27  
- An audio circuit collection, Part 2  
  February 2001  . . . . .41  
- An audio circuit collection, Part 3  
  July 2001  . . . . . . . . .34  
- Audio power amplifier measurements  
  July 2001  . . . . . . . . .40  
- Audio power amplifier measurements, Part 2  
  1Q, 2002  . . . . . . . . .26
<table>
<thead>
<tr>
<th>Title</th>
<th>Issue</th>
<th>Page</th>
<th>Lit. No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifiers: Op Amps</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single-supply op amp design</td>
<td>November 1999</td>
<td>.20</td>
<td>SLYT108</td>
</tr>
<tr>
<td>Reducing crosstalk of an op amp on a PCB</td>
<td>November 1999</td>
<td>.23</td>
<td>SLYT109</td>
</tr>
<tr>
<td>Matching operational amplifier bandwidth with applications</td>
<td>February 2000</td>
<td>.36</td>
<td>SLYT110</td>
</tr>
<tr>
<td>Sensor to ADC — analog interface design</td>
<td>May 2000</td>
<td>.22</td>
<td>SLYT111</td>
</tr>
<tr>
<td>Using a decompensated op amp for improved performance</td>
<td>May 2000</td>
<td>.26</td>
<td>SLYT112</td>
</tr>
<tr>
<td>Design of op amp sine wave oscillators</td>
<td>August 2000</td>
<td>.33</td>
<td>SLYT113</td>
</tr>
<tr>
<td>Fully differential amplifiers</td>
<td>August 2000</td>
<td>.38</td>
<td>SLYT114</td>
</tr>
<tr>
<td>The PCB is a component of op amp design</td>
<td>August 2000</td>
<td>.42</td>
<td>SLYT115</td>
</tr>
<tr>
<td>Reducing PCB design costs: From schematic capture to PCB layout</td>
<td>August 2000</td>
<td>.48</td>
<td>SLYT116</td>
</tr>
<tr>
<td>Thermistor temperature transducer-to-ADC application</td>
<td>November 2000</td>
<td>.44</td>
<td>SLYT117</td>
</tr>
<tr>
<td>Analysis of fully differential amplifiers</td>
<td>November 2000</td>
<td>.48</td>
<td>SLYT118</td>
</tr>
<tr>
<td>Fully differential amplifiers applications: Line termination, driving high-speed ADCs, and differential transmission lines</td>
<td>February 2001</td>
<td>.32</td>
<td>SLYT119</td>
</tr>
<tr>
<td>Pressure transducer-to-ADC application</td>
<td>February 2001</td>
<td>.38</td>
<td>SLYT120</td>
</tr>
<tr>
<td>Frequency response errors in voltage feedback op amps</td>
<td>February 2001</td>
<td>.48</td>
<td>SLYT121</td>
</tr>
<tr>
<td>Designing for low distortion with high-speed op amps</td>
<td>July 2001</td>
<td>.25</td>
<td>SLYT122</td>
</tr>
<tr>
<td>Fully differential amplifier design in high-speed data acquisition systems</td>
<td>2Q, 2002</td>
<td>.35</td>
<td>SLYT123</td>
</tr>
<tr>
<td>Worst-case design of op amp circuits</td>
<td>2Q, 2002</td>
<td>.42</td>
<td>SLYT124</td>
</tr>
<tr>
<td>Using high-speed op amps for high-performance RF design, Part 1</td>
<td>2Q, 2002</td>
<td>.46</td>
<td>SLYT125</td>
</tr>
<tr>
<td>Using high-speed op amps for high-performance RF design, Part 2</td>
<td>3Q, 2002</td>
<td>.21</td>
<td>SLYT126</td>
</tr>
<tr>
<td>FilterPro™ low-pass design tool</td>
<td>3Q, 2002</td>
<td>.24</td>
<td>SLYT127</td>
</tr>
<tr>
<td>Active output impedance for ADSL line drivers</td>
<td>4Q, 2002</td>
<td>.24</td>
<td>SLYT128</td>
</tr>
<tr>
<td>RF and IF amplifiers with op amps</td>
<td>1Q, 2003</td>
<td>.9</td>
<td>SLYT129</td>
</tr>
<tr>
<td>Analyzing feedback loops containing secondary amplifiers</td>
<td>1Q, 2003</td>
<td>.14</td>
<td>SLYT130</td>
</tr>
<tr>
<td>Video switcher using high-speed op amps</td>
<td>3Q, 2003</td>
<td>.20</td>
<td>SLYT131</td>
</tr>
<tr>
<td>Expanding the usability of current-feedback amplifiers</td>
<td>3Q, 2003</td>
<td>.23</td>
<td>SLYT132</td>
</tr>
<tr>
<td>Calculating noise figure in op amps</td>
<td>4Q, 2003</td>
<td>.31</td>
<td>SLYT133</td>
</tr>
<tr>
<td>Op amp stability and input capacitance</td>
<td>1Q, 2004</td>
<td>.24</td>
<td>SLYT134</td>
</tr>
<tr>
<td>Integrated logarithmic amplifiers for industrial applications</td>
<td>1Q, 2004</td>
<td>.28</td>
<td>SLYT135</td>
</tr>
<tr>
<td>Active filters using current-feedback amplifiers</td>
<td>3Q, 2004</td>
<td>.21</td>
<td>SLYT136</td>
</tr>
<tr>
<td>Auto-zero amplifiers ease the design of high-precision circuits</td>
<td>2Q, 2005</td>
<td>.19</td>
<td>SLYT137</td>
</tr>
<tr>
<td>So many amplifiers to choose from: Matching amplifiers to applications</td>
<td>3Q, 2005</td>
<td>.24</td>
<td>SLYT138</td>
</tr>
<tr>
<td>Instrumentation amplifiers find your needle in the haystack</td>
<td>4Q, 2005</td>
<td>.25</td>
<td>SLYT139</td>
</tr>
<tr>
<td>High-speed notch filters</td>
<td>1Q, 2006</td>
<td>.19</td>
<td>SLYT140</td>
</tr>
<tr>
<td>Low-cost current-shunt monitor IC revives moving-coil meter design</td>
<td>2Q, 2006</td>
<td>.27</td>
<td>SLYT141</td>
</tr>
<tr>
<td>Accurately measuring ADC driving-circuit settling time</td>
<td>1Q, 2007</td>
<td>.14</td>
<td>SLYT142</td>
</tr>
<tr>
<td>New zero-drift amplifier has an Iq of 17 μA</td>
<td>2Q, 2007</td>
<td>.22</td>
<td>SLYT143</td>
</tr>
<tr>
<td>A new filter topology for analog high-pass filters</td>
<td>3Q, 2008</td>
<td>.18</td>
<td>SLYT144</td>
</tr>
<tr>
<td>Low-Power RF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Using the CC2430 and TIMAC with low-power wireless sensors: A power-consumption study</td>
<td>2Q, 2008</td>
<td>.17</td>
<td>SLYT145</td>
</tr>
<tr>
<td>Selecting antennas for low-power wireless applications</td>
<td>2Q, 2008</td>
<td>.20</td>
<td>SLYT146</td>
</tr>
<tr>
<td>General Interest</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Synthesis and characterization of nickel manganite from different carboxylate precursors for thermistor sensors</td>
<td>February 2001</td>
<td>.52</td>
<td>SLYT147</td>
</tr>
<tr>
<td>Analog design tools</td>
<td>2Q, 2002</td>
<td>.50</td>
<td>SLYT148</td>
</tr>
<tr>
<td>Spreadsheet modeling tool helps analyze power- and ground-plane voltage drops to keep core voltages within tolerance</td>
<td>2Q, 2007</td>
<td>.29</td>
<td>SLYT149</td>
</tr>
</tbody>
</table>
TI Worldwide Technical Support

Internet
TI Semiconductor Product Information Center Home Page
support.ti.com

TI Semiconductor KnowledgeBase Home Page
support.ti.com/sc/knowledgebase

Product Information Centers

**Americas**

**Phone**  +1(972) 644-5580
**Fax**  +1(972) 927-6377
**Internet/Email**  support.ti.com/sc/pic/americas.htm

**Europe, Middle East, and Africa**

**Phone**
- European Free Call  00800-ASK-Texas (00800 275 89327)
- International  +49 (0) 8161 80 2121
- Russian Support  +7 (4) 95 98 10 701

**Note:** The European Free Call (Toll Free) number is not active in all countries. If you have technical difficulty calling the free call number, please use the international number above.

**Fax**  +49 (0) 8161 80 2045
**Internet**  support.ti.com/sc/pic/euro.htm

**Japan**

**Fax**
- International  +81-3-3344-5317
- Domestic  0120-81-0036

**Internet/Email**
- International  support.ti.com/sc/pic/japan.htm
- Domestic  www.tij.co.jp/pic

**Asia**

**Phone**
- International  +91-80-41381665
- Domestic  Toll-Free Number
- Australia  1-800-999-084
- China  800-820-8682
- Hong Kong  800-96-5941
- India  1-800-425-7888
- Indonesia  001-803-8861-1006
- Korea  080-551-2804
- Malaysia  1-800-80-3973
- New Zealand  0800-446-934
- Philippines  1-800-765-7404
- Singapore  800-886-1028
- Taiwan  0800-006800
- Thailand  001-800-886-0010

**Fax**  +886-2-2378-6808
**Email**  tiasia@ti.com or ti-china@ti.com
**Internet**  support.ti.com/sc/pic/asia.htm

**Important Notice:** The products and services of Texas Instruments Incorporated and its subsidiaries described herein are sold subject to TI’s standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer’s applications or product designs, software performance, or infringement of patents. The publication of information regarding any other company’s products or services does not constitute TI’s approval, warranty or endorsement thereof.

Auto-Track, FilterPro, Impedance Track and SWIFT are trademarks of Texas Instruments. The Bluetooth word mark and logos are owned by the Bluetooth SIG, Inc., and any use of such marks by Texas Instruments is under license. Celeron is a trademark and StrataFlash is a registered trademark of Intel Corporation. InfiniBand is a service mark of the InfiniBand Trade Association. All other trademarks are the property of their respective owners.