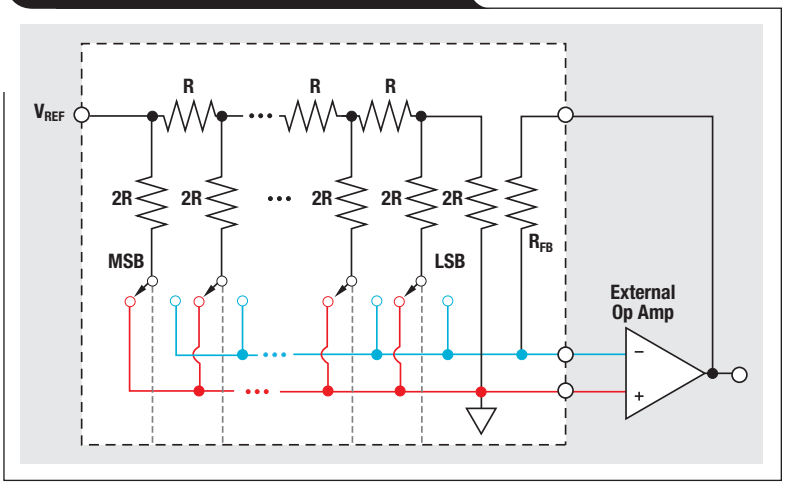
A DAC for all precision occasions

By Bonnie C. Baker, *Senior Applications Engineer*

Introduction

Analog-to-digital converters (ADC) routinely convert analog signals such as temperature, pressure, sound, or images to a precise digital representation. Microcontrollers and microprocessors store, massage, and transmit this digital information throughout a system. There are also times when precision digital-to-analog converters (DAC) convert the digital representation of these real-world events back into the analog domain. Three of the DAC topologies that achieve this feat are the R-2R MDAC, R-2R backDAC, and the string DAC. These three topologies service applications such as automatic test equipment, instrumentation, portable equipment, and digitally controlled calibration.

Figure 1. An R-2R multiplying DAC



The R-2R MDAC

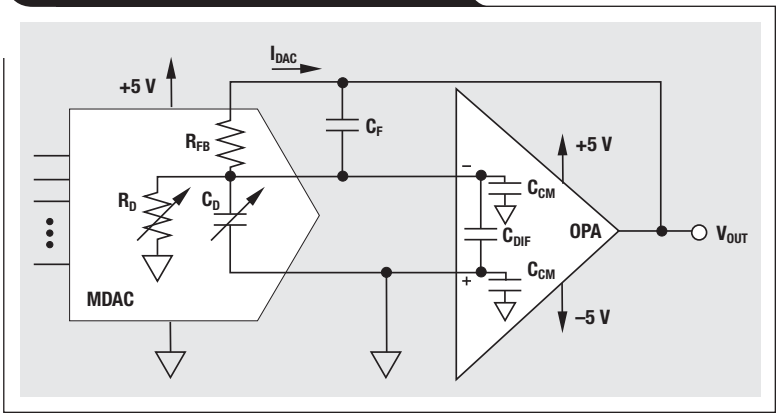
Automatic test equipment or instrumentation typically uses the R-2R multiplying DAC (MDAC, Figure 1). The external operational amplifier augments the DAC function by providing the opportunity for differing supply voltages and high output currents. MDAC manufacturers are able to design high resolution devices (16 bit) with ±1 LSB integral non-linearity (INL) and differential non-linearity (DNL) specifications. With an appropriate external amplifier, the MDAC exhibits fast settling time (< 0.3 ms) with a multiplying bandwidth that can be greater than 10 MHz.

The MDAC generates a current that is proportional to an input digital code. The external amplifier, along with R_{FB} (internal in the MDAC), converts the DAC's current-output signal to a usable voltage level. It would seem that a simple current-to-voltage conversion is easy to implement with a DAC, an amplifier, and a resistor. However, this application circuit has a set of stability issues.

The output model of the MDAC contains a current source, variable resistor, and variable capacitor (Figure 2a). The output resistance and capacitance of the MDAC is dependent on the input code to the DAC. Programming the MDAC to zero causes the output resistance (R_D) to be near infinite. If you program the MDAC to full scale or all ones, R_D is equal to R_{FB}. The output capacitance (C_D) changes according to the number of internal gate-source junctions across the MDAC output. At full scale, the MDAC output capacitance is equal to the data sheet specification. When programmed to zero scale, the MDAC output capacitance is equal to approximately half the full-scale value. As we calculate the worst-case stability condition, we will use the full-scale output values of R_D and C_D.

To maintain precision, most MDACs have a feedback resistor (R_{FB}) on-chip. The feedback capacitor, C_F, is external and discrete. The unity gain bandwidth (f_U) of

Figure 2a. MDAC model



the operational amplifier, as well as the input-differential capacitance (C_{DIF}) and common-mode capacitance (C_{CM}), directly affect the stability of this circuit.

At the input of the amplifier, the total capacitance in this system is equal to $C_{IN} = C_D + C_{DIF} + C_{CM}$. The pole and zero in the feedback loop of the amplifier are equal to (see Figure 2b and c):

$$f_1 = \frac{1}{2\pi(C_{IN} + C_F) \times (R_D \parallel R_F)} \quad \text{[feedback circuit zero]}$$

$$f_2 = \frac{1}{2\pi(C_{IN} + C_F)} \quad \text{[feedback circuit pole]}$$

You determine the system stability by keeping the difference of the rate of change of the operational amplifier open-loop gain curve and the closed-loop gain curve at 20 dB/decade. You can do this by selecting an amplifier with unity gain bandwidth (f_U) less than f_1 or higher than f_2 (Figure 2b and c).

From here, it is easy to design a stable circuit. If f_1 is higher than the unity gain crossing of the amplifier f_U, the following formula applies to this design.

$$C_F \geq \frac{1 + \sqrt{1 + 8\pi C_{IN} R_F f_U}}{2\pi R_F f_U}$$

If f_2 is lower than the intersection of the open-loop gain curve and the closed-loop gain curve, use this formula.

$$C_F \leq \frac{1}{2\pi(R_D \parallel R_F) f_U} - C_{IN}$$

These calculated values of C_F are a starting point. As you test your circuit, parasitics, device manufacturing variations, etc. can prompt you to modify the value of C_F.

Making the MDAC analog voltage signal stable is critical. However, there are other issues to take into account. At the risk of covering this topic too briefly, consider issues such as amplifier noise, input bias current, and offset voltage, as well as MDAC resolution and glitch energy.

The MDAC is a low-noise solution for a variety of applications. The voltage-reference, current-output change with digital codes to the MDAC is constant. The trade-off for this advantage is varying ground currents with digital input codes. Typically, you will find MDACs in digital gain and attenuation control circuits as well as waveform generators.

The R-2R back-DAC

You usually use the R-2R back-DAC (Figure 3) in industrial applications. Some other applications for the R-2R back-DAC include instrumentation and digitally controlled calibration. With the R-2R back-DAC, each new update switches the 2R legs to either the voltage reference high (VREF-H) or the voltage reference low (VREF-L). Notice that the arrangement of the R-2R ladder is upside down as compared to the MDAC. This is where the name "back-DAC" came from. This architecture is simple to manufacture, assuming the resistors for each current source can be properly adjusted.

Gate-switch timing skews manifest themselves at the output of the MDAC and back-DAC as glitches. The glitch is most prevalent during the MSB transition, when bits are

Figure 2b. Model's frequency response with a high-bandwidth amplifier

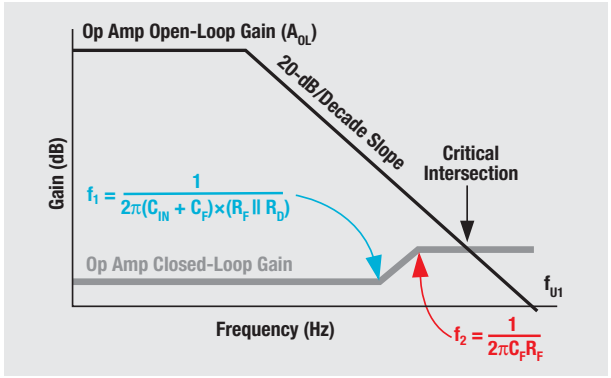


Figure 2c. Model's frequency response with a low-bandwidth amplifier

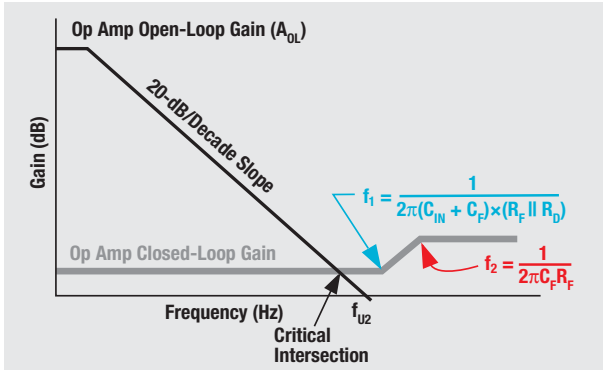


Figure 3. An R-2R Back-DAC

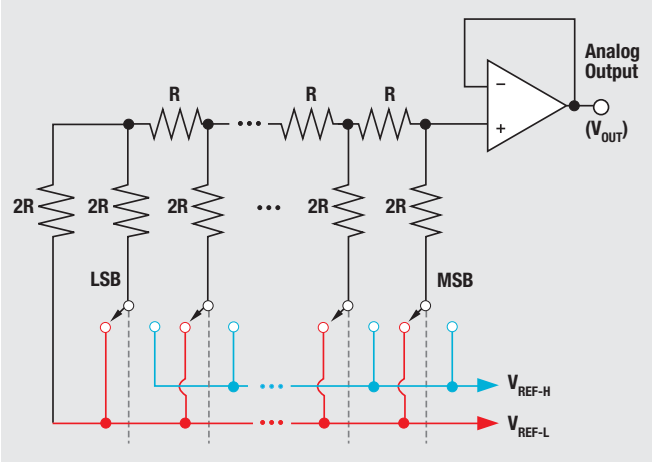


Figure 4a. Glitch impulse of a DAC producing two regions of code transition error

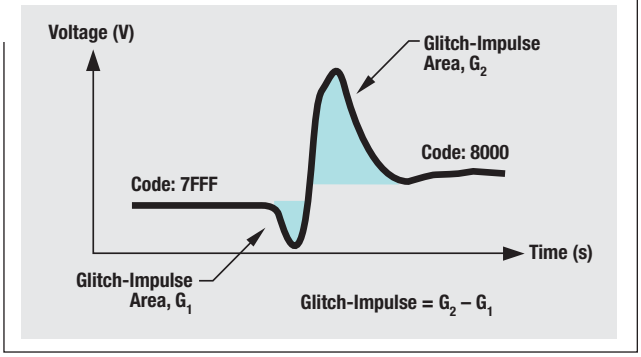
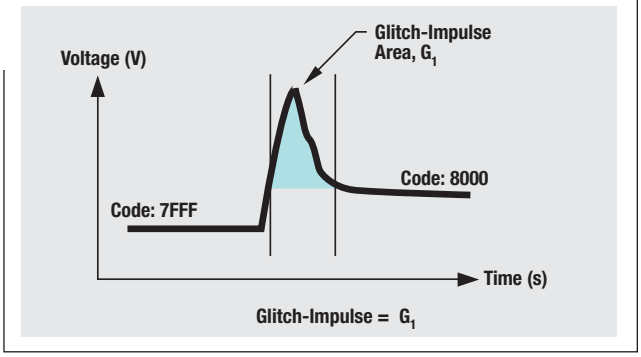


Figure 4b. Glitch impulse of DAC producing one region of overshoot



switching from 7FFFh to 8000h (for a 16-bit DAC). The R-2R back-DAC, like the MDAC, typically has excellent low noise, INL, and DNL performance, with medium settling-time capability.

DAC glitches result from capacitive-charge injection from the internal, asynchronous gate switching. The DAC glitch for R-2R DACs typically has two lobes (Figure 4a), while string topologies typically have a single-lobe glitch impulse (Figure 4b).

The units of a glitch impulse is volts/seconds. Glitch impulses are most dramatic between consecutive codes where a major code transition occurs. In Figure 4a the total glitch impulse equals G_2 minus G_1, where G_1 and G_2 are the calculated areas. In Figure 4b the total glitch impulse equals the shaded area of G_1. In most systems, you can ignore the glitches that occur at the output of a DAC during code transition; however, in a control loop, glitch impulses are typically undesirable. In a control system, the DAC glitch impulse from a one-bit code transition, where the MSB is switching, confuses the loop by momentarily sending an erroneous output-voltage signal.

The glitch-impulse area in Figure 4a occurs during the DAC's output-voltage transition region as it switches from one code to another. As the 16-bit DAC switches from 8000h to 7FFFh (or half the full-scale output voltage), the output glitch impulse becomes noticeable to the extent that it appears as if the DAC is momentarily non-monotonic. Secondary glitches occur around the one-fourth full-scale and three-fourths full-scale voltages. If the control system is fast enough to respond to this glitch, the circuit may oscillate.

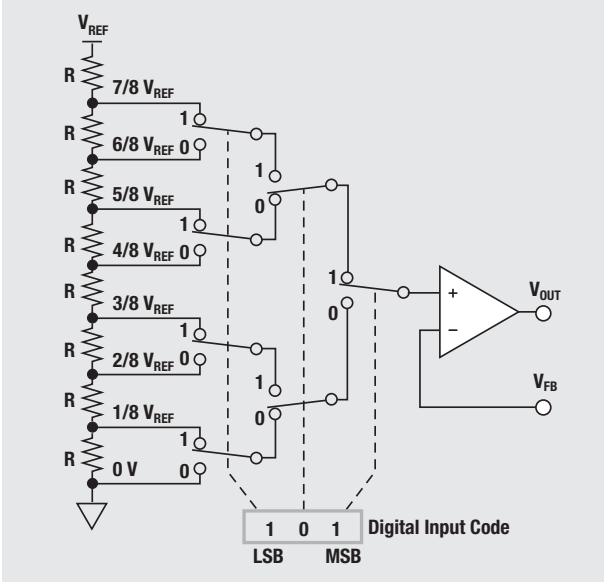
You can try to reduce the impact of this glitch impulse by using a low-pass filter at the output of the DAC. However, while a low-pass filter reduces the glitch-impulse amplitude, it increases the glitch time. For example, consider a glitch-impulse response of the 16-bit DAC is equal to 96 nV-s, with a peak voltage of 60 mV and duration of 1.6 µs. You can filter this glitch impulse so that the peak voltage is 30 mV with duration of 3.2 µs. You can also add sampling circuitry on the output of the DAC and time it with DAC conversions. This technique may work for lower resolution, slow DACs; however, the sampling mechanism may create more problems by adding to the analog errors and conversion time. The best way to overcome larger glitch impulses is to select a string DAC with lower glitch-impulse errors from the start.

The R-2R back-DAC has medium settling time capability; however, you can build high-performance circuits with its superior INL and DNL performance. Texas Instruments achieves higher accuracy specifications with final test trimming. The R-2R ladder also facilitates low-noise performance from the DAC.

String DAC topology

The string DAC is best suited for portable instrumentation, closed-loop servo control, and process control. Figure 5 shows a model of a 3-bit string DAC. In this figure, the digital input code 101b is decoded to 5/8 V_{REF}. The string DAC's output-stage amplifier isolates the internal resistive elements from output loads. The string DAC is a low-power solution that guarantees monotonicity

Figure 5. String DAC topology



with good DNL performance across the entire input code range. The glitch energy is typically lower than other types of DACs; however, the INL performance is generally larger and dependent on resistive, on-chip matching. On the other hand, a DAC in a control loop lessens the impact of high linearity. The noise of string DACs is also relatively high because of the resistive string-array impedance.

The string DAC operates with low power and very low glitch energy. An on-chip output buffer simplifies the interface to this device.

DAC calibration

With any of the three DACs in this article, you may see a need to calibrate the analog output for higher precision results. If you calibrate any DAC, you initially determine the code-to-voltage error at one-third of the output range and again at two-thirds of the output range. The range between one-third full scale (FS) and two-thirds FS avoids the output amplifier errors near the power supply rails. You achieve the calibration of the offset and gain errors with the formula $V_{OUT} = a + bV_{IN}$ ("a" is the offset error and "b" is the gain error). You can calibrate your DAC in the digital domain with the help of an ADC that is more accurate than the target specifications of a DAC.

A more challenging DAC calibration activity is to adjust the linearity of the converter's entire output range. Once again, you will require an ADC that has four times the resolution of the DAC. You can calibrate every DAC code with 8, 10, or 12 bits of resolution. In this environment there are fewer DAC codes to calibrate and the memory requirements are lower. The accuracy of the calibrating low-bit ADC is not as demanding, allowing faster ADC conversion times. For DACs with resolution of 14+ bits, the total number of codes becomes unmanageable in terms of processor memory. Additionally, you will need to use a slower ADC with higher accuracy, such as a delta-sigma converter. Higher cost and slower speeds will encourage you to consider alternative DAC calibration strategies.

An effective alternative to linearizing every DAC code is to select several small groups of codes. The plot in Figure 6a shows an example of the integral non-linearity of a 16-bit string DAC. The universal formula for calculating any DAC correction code is

$$DAC_{COR} = INL_V + (INL_V - INL_W) \times \frac{v - x}{v - w},$$

where INL_V and INL_W are the INL error of the v and w code. x is a code between codes v and w. If (v – w) is equal to an integer that is a power of two, you can implement the division with right shifts, reducing the processor calculation time and complexity. Figure 6b illustrates the benefit of this linearization technique using 1024 code groupings, 64 codes per group.

This technique is best suited for DACs that are monotonic, with INL error in excess of ±8 LSB. Additionally, you must exercise care when selecting the size of the code sets. If there are large, sudden jumps from one code to the next, as may be with R-2R architectures, this technique may prove to be counterproductive instead of an improvement in DAC performance. The string DAC topology is best suited for this calibration technique because it is inherently monotonic (a requirement for this technique) and jumps from one code to the next are relatively small as compared to other DAC topologies.

Figure 6a. INL of a 16-bit string DAC

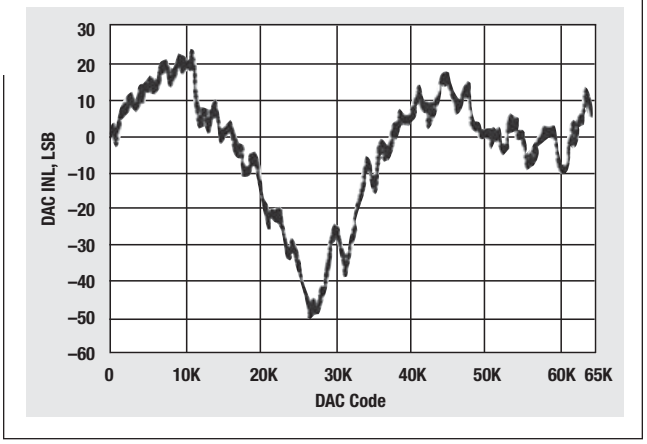
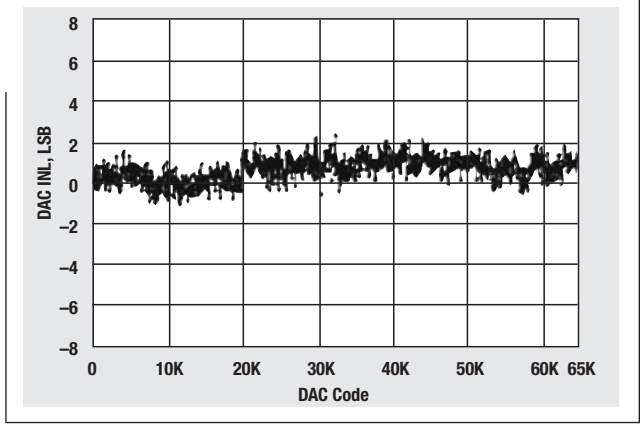


Figure 6b. A correction step of 64 LSB (1024 out of the 65,536 points) reduces the INL error to less than ± 3 LSB



Conclusion

A precision DAC uses a limited number of discrete digital input codes to produce a corresponding number of discrete analog output values. For a DAC, 1 LSB corresponds to the height of a step between successive analog outputs, with the value defined in the same way as for the ADC. The MDAC, R-2R back-DAC, and string DAC architectures do not encompass all of the possible DAC topologies, but if you know about these topologies you will have a good start on knowing the basics.

Related Web sites

dataconverter.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products	
Amplifiers	**amplifier.ti.com**
Data Converters	**dataconverter.ti.com**
DSP	**dsp.ti.com**
Interface	**interface.ti.com**
Logic	**logic.ti.com**
Power Management	**power.ti.com**
Microcontrollers	**microcontroller.ti.com**
Applications	
Audio	**www.ti.com/audio**
Automotive	**www.ti.com/automotive**
Broadband	**www.ti.com/broadband**
Digital control	**www.ti.com/digitalcontrol**
Military	**www.ti.com/military**
Optical Networking	**www.ti.com/opticalnetwork**
Security	**www.ti.com/security**
Telephony	**www.ti.com/telephony**
Video & Imaging	**www.ti.com/video**
Wireless	**www.ti.com/wireless**

TI Worldwide Technical Support

Internet

TI Semiconductor Product Information Center Home Page
support.ti.com

TI Semiconductor KnowledgeBase Home Page
support.ti.com/sc/knowledgebase

Product Information Centers

Americas

Phone	+1(972) 644-5580	Fax	+1(972) 927-6377
Internet/Email	support.ti.com/sc/pic/americas.htm		

Europe, Middle East, and Africa

Phone

European Free Call	00800-ASK-TEXAS (00800 275 83927)
International	+49 (0) 8161 80 2121
Russian Support	+7 (4) 95 98 10 701

Note: The European Free Call (Toll Free) number is not active in all countries. If you have technical difficulty calling the free call number, please use the international number above.

Fax	+(49) (0) 8161 80 2045
Internet	support.ti.com/sc/pic/euro.htm

Japan

Fax			
International	+81-3-3344-5317	Domestic	0120-81-0036
Internet/Email			
International	support.ti.com/sc/pic/japan.htm		
Domestic	www.tij.co.jp/pic		

Asia

Phone			
International	+886-2-23786800		
Domestic	Toll-Free Number		Toll-Free Number
Australia	1-800-999-084	Malaysia	1-800-80-3973
China	800-820-8682	New Zealand	0800-446-934
Hong Kong	800-96-5941	Philippines	1-800-765-7404
India	+91-80-41381665 (Toll)	Singapore	800-886-1028
Indonesia	001-803-8861-1006	Taiwan	0800-006800
Korea	080-551-2804	Thailand	001-800-886-0010
Fax	+886-2-2378-6808	Email	tiasia@ti.com
Internet	support.ti.com/sc/pic/asia.htm		ti-china@ti.com

C010208

Safe Harbor Statement: This publication may contain forward-looking statements that involve a number of risks and uncertainties. These "forward-looking statements" are intended to qualify for the safe harbor from liability established by the Private Securities Litigation Reform Act of 1995. These forward-looking statements generally can be identified by phrases such as TI or its management "believes," "expects," "anticipates," "foresees," "forecasts," "estimates" or other words or phrases of similar import. Similarly, such statements herein that describe the company's products, business strategy, outlook, objectives, plans, intentions or goals also are forward-looking statements. All such forward-looking statements are subject to certain risks and uncertainties that could cause actual results to differ materially from those in forward-looking statements. Please refer to TI's most recent Form 10-K for more information on the risks and uncertainties that could materially affect future results of operations. We disclaim any intention or obligation to update any forward-looking statements as a result of developments occurring after the date of this publication.

Trademarks: All trademarks are the property of their respective owners.

Mailing Address: Texas Instruments
Post Office Box 655303
Dallas, Texas 75265