Designing with digital isolators

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Introduction

The purpose of this article is to help engineers use the Texas Instruments (TI) ISO72xx family of digital isolators to design galvanically isolated systems in the shortest time possible. The article explains the basic operating principle of the TI isolator, suggests where to place it within a system design, and recommends guidelines for an electromagnetic-compatible (EMC) circuit-board design.

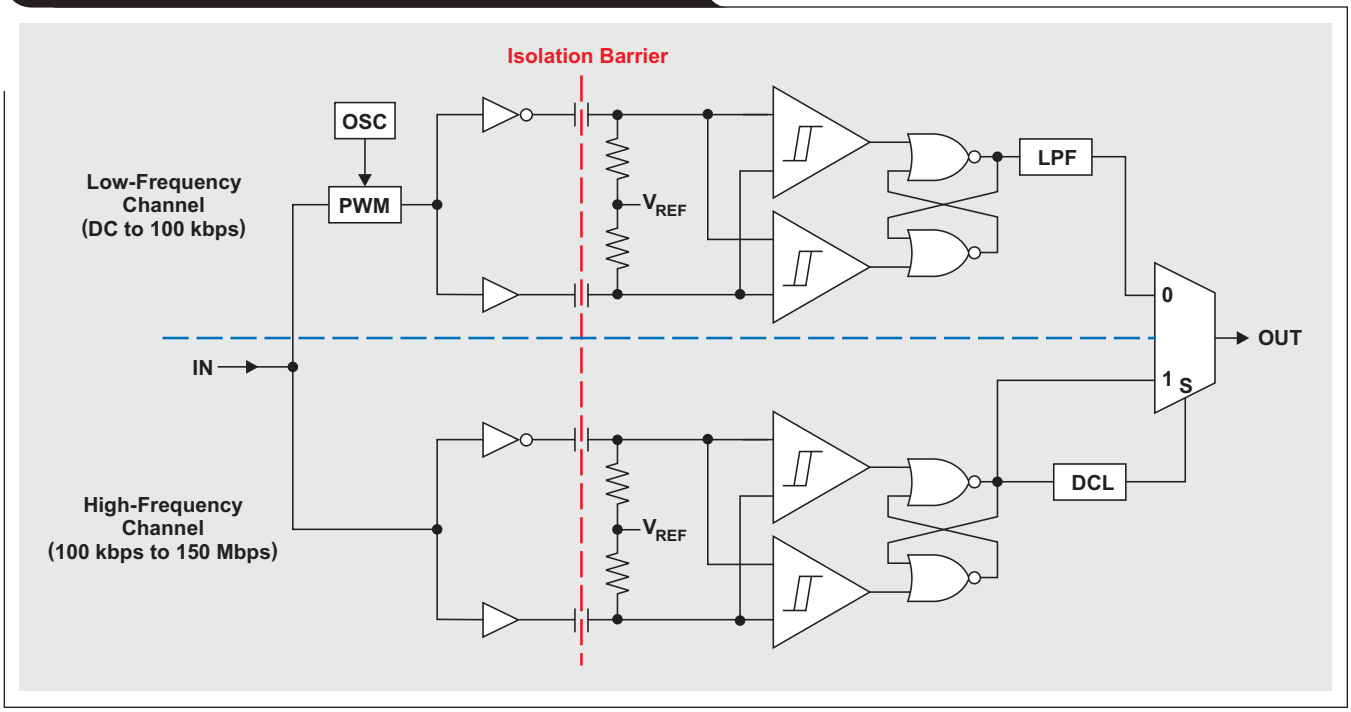
Operating principle

The isolator in Figure 1 is based on a capacitive-isolation-barrier technique. The device consists of two data channels —a high-frequency channel with a bandwidth ranging from 100 kbps up to 150 Mbps, and a low-frequency channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the high-frequency channel is split into a differential signal via the inverter gate at the input. The subsequent capacitor-resistor networks differentiate the signal into transients, which are then converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, as in the case of a low-frequency signal, the DCL forces the output multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, a pulse-width modulator (PWM) is used to modulate these signals with the carrier frequency of an internal oscillator (OSC), thus creating a frequency high enough to pass the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before it is passed on to the output multiplexer.

Figure 1. Block diagram of a digital capacitive isolator



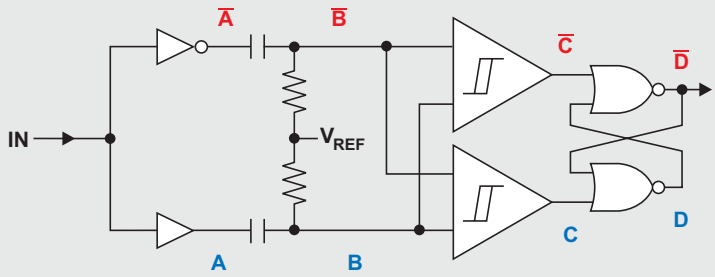
High-frequency-channel operation

Figure 2 presents the high-frequency channel and the waveforms at specific points of the signal chain. The single-ended input signal is split into the differential signal components, A and $\overline{A}$. Each signal component is then differentiated into the transients, B and $\overline{B}$. The subsequent comparators compare the differential transients to one another. As long as the positive input of a comparator has a higher potential than its negative input, the comparator output will present a logical high, thus converting an input transient into a short output pulse.

The output pulses set and reset a NOR-gate flip-flop. From the "NOR-Gate Truth Table" in Figure 2 we see that the NOR-gate configuration presents an inverting flip-flop, meaning that a high at input C sets output $\overline{D}$ to high, and a high at $\overline{C}$ sets D to high. Because the comparator output pulses are of short duration, there will be times when both outputs are low. During this time the flip-flop stores its previous output condition. Since the signal at $\overline{D}$ is identical to the input signal in shape and phase, $\overline{D}$ becomes the output of the high-frequency channel and is connected to the output multiplexer.

While input signals with symmetrical duty cycles cause equidistant pulses at the comparator outputs, asymmetrical signals (shown in the "Data Transfer" timing diagram in Figure 2) move the comparator pulses closer to each other to maintain the shape and phase relationships of the input signal.

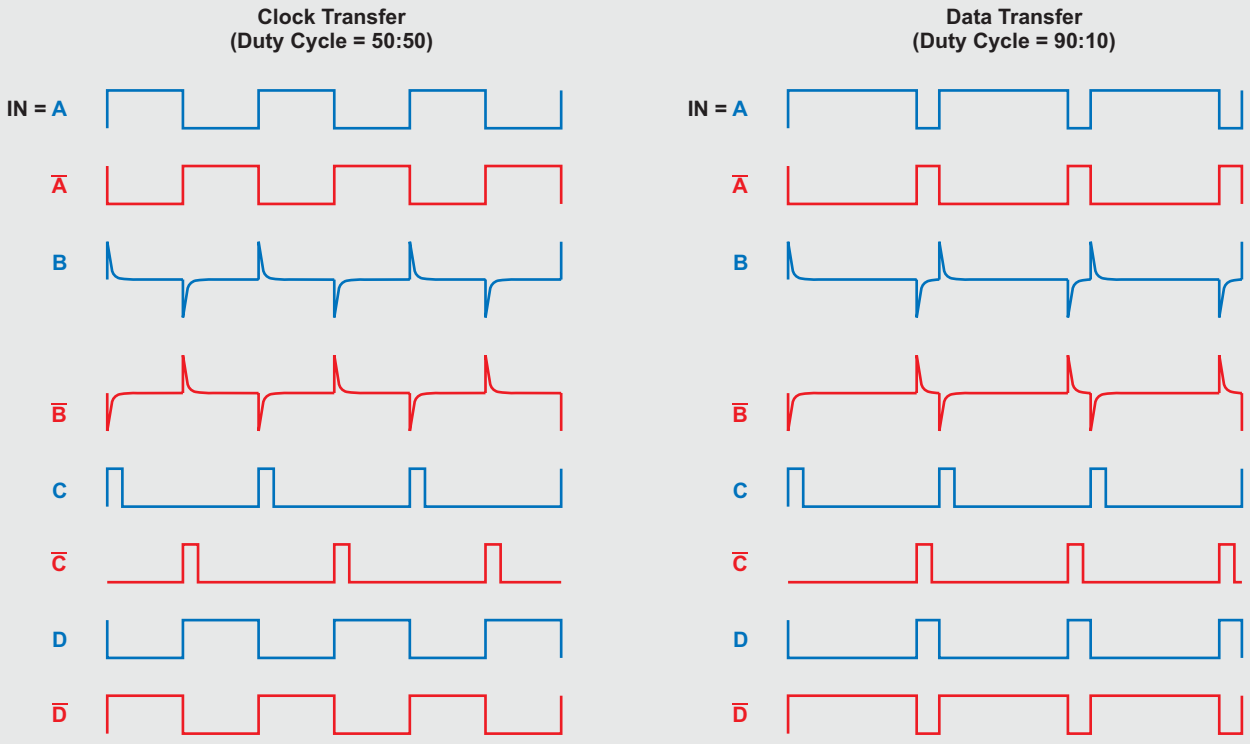
Figure 2. Timing in high-frequency-channel operation



NOR-Gate Truth Table

C	$\overline{C}$	D	$\overline{D}$
L	L	S*	S
L	H	H	L
H	L	L	H
H	H	L	L

*S = Store previous condition



Low-frequency-channel operation

As shown in Figure 3, a PWM modulates slow input signals with a high-frequency carrier such that, at location A, a high-level input yields a 90:10 duty cycle, and a low-level input yields a 10:90 duty cycle. From there on, signal processing is identical to the asymmetrical signal processing in the high-frequency channel. The only exception is that the high-frequency content of $\overline{D}$, the low-frequency channel, is filtered by an R-C LPF before being passed on to the output multiplexer, E.

Isolator technology and requirements

The successful proof of the single isolator's ability to transmit wideband data (from DC to above 150 Mbps) inspired TI to fabricate unidirectional and bidirectional devices in dual-, triple-, and quad-channel versions that accommodate the most common digital interfaces encountered in industrial applications (see Figure 4). All TI digital isolators utilize single-ended, 3-V/5-V CMOS-logic switching technology. Their nominal supply-voltage range is specified

Figure 3. Timing in low-frequency-channel operation

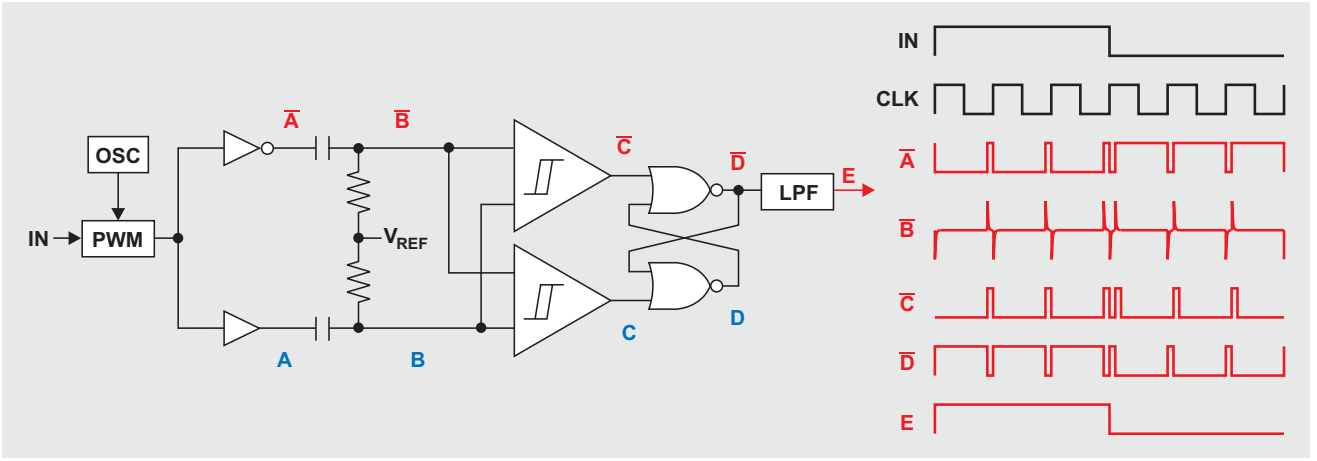
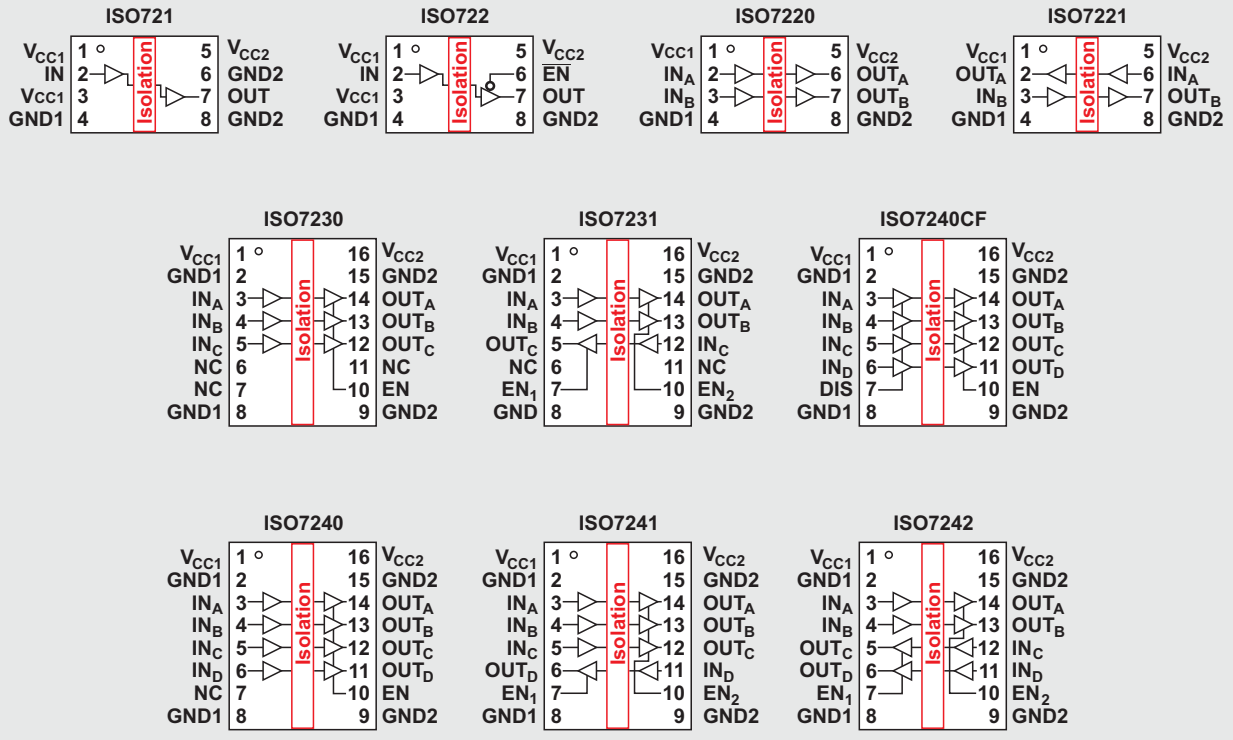


Figure 4. TI family of stand-alone digital isolators



from 3.3 V to 5 V for both supplies, V_{CC1} and V_{CC2}, and allows any combination of these values.

It is important for the designer to keep in mind that digital isolators, due to their single-ended design structure, do not conform to any specific interface standard and are intended only for isolating single-ended, 3-V/5-V digital signal lines.

Figures 5 to 7 give examples of isolated interfaces for SPI, RS-232, and RS-485 applications. Note that the isolator is always placed between the data controller (i.e., the microcontroller or UART) and a data converter or line transceiver, regardless of the interface type or standard.

Figure 5 presents the simplest isolator application. Here the entire circuit constitutes a single-ended, low-voltage system in which a digital isolator connects the SPI interface of a controller with the SPI interface of a data converter. The most commonly applied TI isolators in SPI interfaces are ISO7231 and ISO7241, often designated as 3- and 4-channel SPI isolators.

The full-blown, isolated RS-232 interface in Figure 6 requires two quad isolators because six control signals are required in addition to the actual data lines, RX and TX. Although the entire system is single-ended, the high-voltage requirements of the symmetrical, ±13-V bus supply make it necessary to galvanically isolate the data link between the UART and the low-voltage side of the bus transceiver.

Figure 5. Isolated SPI interface

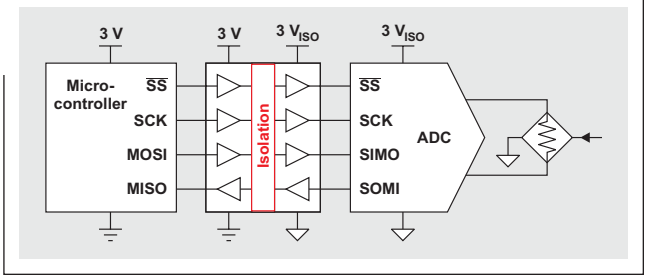
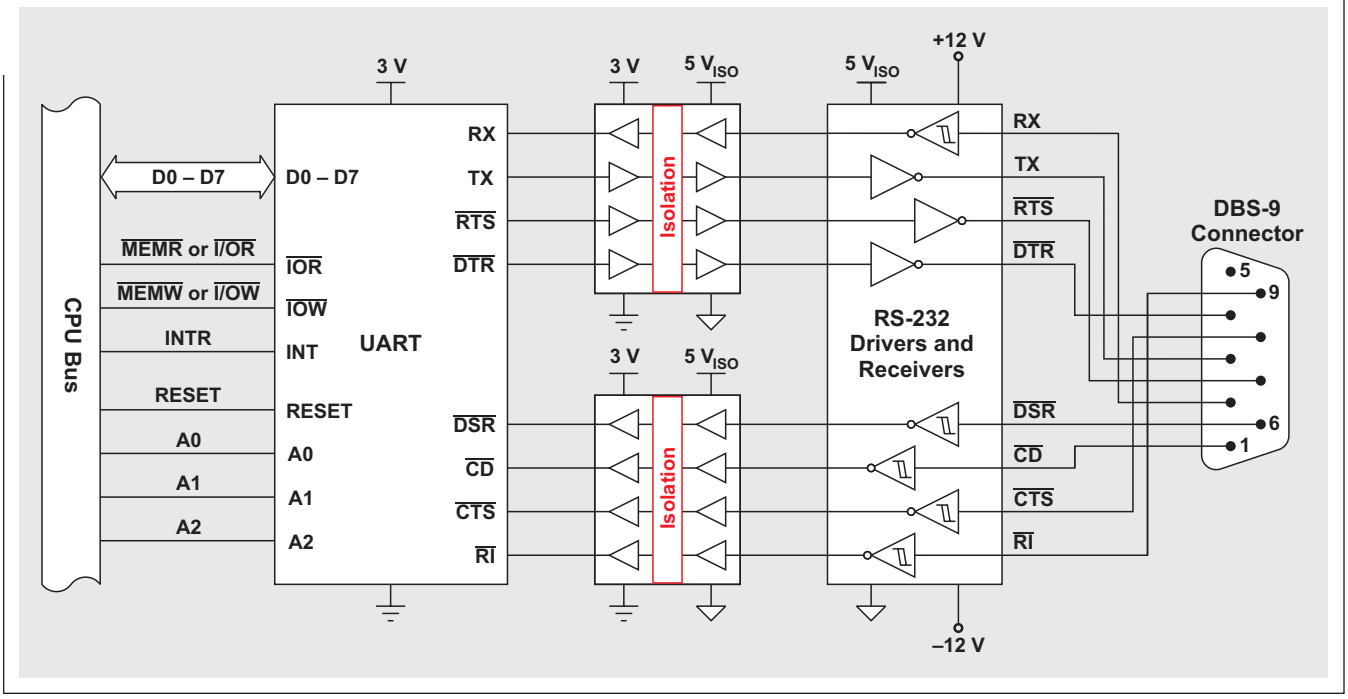


Figure 6. Isolated RS-232 interface



As in the previous example, the isolation of the RS-485 interface in Figure 7a occurs between the controller and the bus transceiver. Despite the entire interface circuit being a low-voltage system, the differential nature of the transmission bus requires prior isolation on the single-ended side. Due to the simplicity of this interface, it was possible to integrate the isolator function into the RS-485 transceiver circuit as shown in Figure 7b, thus providing an application-specific isolator device featuring low cost and a low component count.

To simplify the selection of an appropriate isolator for a specific application, Table 1 provides a comprehensive overview of TI digital isolators. Of the five different speed grades for isolators—A, B, C, CF, and M—all but the M version possess internal low-pass noise filters at the data inputs and are therefore recommended for use in noisy environments. The high-speed version, M, requires external input filtering when used in noisy environments. This is accomplished by connecting a filter capacitor from an

Figure 7. Isolated RS-485 interface

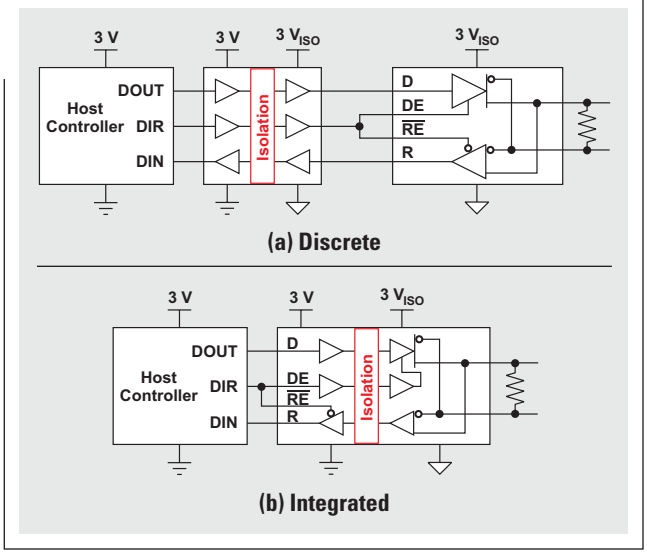


Table 1. Overview of TI stand-alone and application-specific isolators

ISOLATOR TYPE	DEVICE	SPEED GRADE	INPUT THRESHOLD	MAX. DATA RATE* (Mbps)	MAX. PROP. DELAY* (ns)	MAX. CH/CH OUTPUT SKEW* (ns)	TYPICAL OUTPUT RISE TIME* (ns)
Single	ISO721/722		TTL	100	24	—	1
		M	CMOS	150	16	—	1
Dual	ISO7220/7221	A	TTL	1	475	15	1
		B		5	70	3	1
		C		25	42	1	1
		M	CMOS	150	16	1	1
Triple	ISO7230/7231	A	TTL	1	95	2	2
		C		25	42	2	2
		M	CMOS	150	23	1	2
Quad	ISO7240/7241/7242	A	TTL	1	95	2	2
		C		25	42	2	2
		M	CMOS	150	23	1	2
	ISO7240	CF	TTL	25	42	2	2
RS-485 Half-Duplex	ISO3082		TTL	0.2	1.3 (XTR) 125 (RCV)	—	900 (XTR) 1 (RCV)
	ISO15		TTL	1	340 (XTR) 100 (RCV)	—	185 (XTR) 2 (RCV)
	ISO3088		TTL	20	45 (XTR) 125 (RCV)	—	7 (XTR) 1 (RCV)
RS-485 Full-Duplex	ISO3080		TTL	0.2	1.3 (XTR) 125 (RCV)	—	900 (XTR) 1 (RCV)
	ISO35		TTL	1	340 (XTR) 100 (RCV)	—	185 (XTR) 2 (RCV)
	ISO3086		TTL	20	45 (XTR) 125 (RCV)	—	7 (XTR) 1 (RCV)
PROFIBUS Half-Duplex	ISO1176		—	40	40 (XTR) 55 (RCV)	1	3 (XTR) 2 (RCV)

*Switching characteristics with $V_{CC1} = V_{CC2} = 5$ V.

input to the respective device ground. The capacitor value is calculated as

$$C_F = \frac{1}{2\pi \times f_{max} \times R_{SS}},$$

where f_{max} is the maximum signal frequency and R_{SS} is the output impedance of the signal source.

PCB design guidelines

PCB material

Standard Flame Retardant 4 (FR-4) epoxy glass should be used as PCB material for digital circuit boards operating below 150 Mbps (or with rise and fall times longer than 1 ns) and with trace lengths of up to 10 inches. FR-4 meets the requirements of Underwriters Laboratories UL 94 V-0 and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies; low moisture absorption; greater strength and stiffness; and self-extinguishing burning characteristics.

Layer stack

A minimum of four layers is required to accomplish a PCB design with low electromagnetic interference (EMI) (see Figure 8). Layers should be stacked in the following order, from top to bottom:

- *High-speed traces*—Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator, transmitter, and receiver circuits of the data link.
- *Ground plane*—Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission-line interconnects and provides an excellent low-inductance path for the return current flow.
- *Power plane*—Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- *Low-speed traces*—Routing the slower-speed control signals on the bottom layer allows for greater flexibility, as these signal links usually have a margin to tolerate discontinuities such as vias.

If an additional supply-voltage plane or signal layer is needed, a second power/ground-plane system can be added to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground planes of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Creepage distance

Creepage distance is the shortest path between two conductive parts, measured along the surface of the insulation. An adequate creepage distance protects against tracking, a process that produces a partially conducting path of localized deterioration on the surface of an insulating material as a result of the electric discharges on or close to that surface. Tracking damage to the insulating material normally occurs because of one or more of the following reasons: humidity in the atmosphere, the presence of contamination such as that from corrosive chemicals, and the altitude at which equipment is operated.

The degree of tracking that occurs depends on the comparative tracking index (CTI) of the material and the degree of pollution in the environment. Used for electrical insulating materials, the CTI provides a numerical value of the voltage that will cause failure due to tracking during standard testing. Reference 1 provides a fuller explanation of tracking and CTI.

With higher isolation-voltage levels, it is more important than ever to have a robust PCB design that not only reduces EMI emissions but also reduces creepage problems. In addition to wide isolator packaging, techniques such as cutting grooves can be used to attain a desired creepage distance (see Figure 9).

For a groove wider than 1 mm, the only depth requirement is that the existing creepage distance plus the width of the groove and twice the depth of the groove must equal or exceed the required creepage distance. The groove should not weaken the substrate to a point that it fails to meet mechanical test requirements.

Also, on all layers, the space under the isolator should be kept free of traces, vias, and pads to maintain maximum creepage distance (see Figure 8).

Figure 8. Recommended layer stack

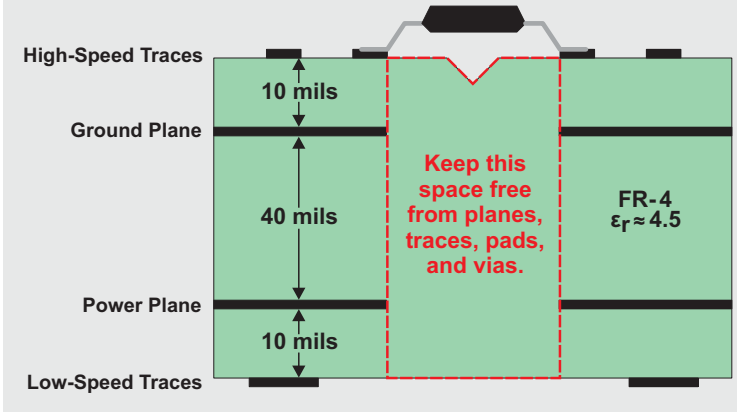


Figure 9. Groove cutting extends effective creepage distance

Controlled-impedance transmission lines

A controlled-impedance transmission line is a trace whose characteristic impedance, Z_0, is tightly controlled by the trace geometries. In general, these traces match the differential impedance of the transmission medium, such as cables and line terminators, to minimize signal reflections. Around digital isolators, controlled-impedance traces must match the isolator's output impedance, $Z_0 \approx r_O$, which is known as source-impedance matching (see Figure 10).

To determine Z_0, the dynamic output impedance of the isolator, $r_O = \Delta V_{OUT}/\Delta I_{OUT}$, needs to be established. For that purpose, the output characteristic in Figure 11 (based on the ISO7240 data sheet) is approximated by two linear segments. One indicates that $r_O \approx 260\ \Omega$ at low voltages; the other indicates that $r_O \approx 70\ \Omega$ for the majority of the curve—and thus for the transition region of the output.

The required trace geometries, such as trace thickness (t) and width (w), the height of the trace (h) above an adjacent ground layer, and the PCB dielectric (ε_r), are partially dictated by the copper-plating capabilities of the board manufacturing process and the dielectric of the chosen board material. Typical values are 1 and 2 oz of copper plating, resulting in trace thicknesses (t) of 1.37 and 2.74 mils, respectively. The dielectric value (ε_r) for FR-4 epoxy glass varies between 2.8 and 4.5 for microstrips and is 4.5 for stripline traces.

With t and ε_r given, the designer has the freedom to define Z_0 through the trace width (w) and height (h). For PCB designs, however, the most critical dimensions are not the absolute values of w and h but their ratio, w/h. Easing the designer's task, Figure 12 plots the characteristic trace impedance as a function of the width-to-height ratio (w/h) for a trace thickness of 2.74 mils (2-oz copper plating), an FR-4 dielectric of 4.5, and a trace height (h) of 10 mils above the ground plane.

From Figure 12 we see that a 70-Ω design requires a w/h ratio of about 0.8. As described later under "Reference planes," designing a low-EMI board requires close electric coupling between the signal trace and ground plane, which is accomplished by ensuring that h = 10 mils. The corresponding trace width would therefore be 8 mils. This width must be maintained across the entire trace length; otherwise, variations in trace width will cause discontinuities in the characteristic impedance, leading to increased reflections and EMI.

Figure 10. Source-impedance matching: $Z_0 \approx r_O$

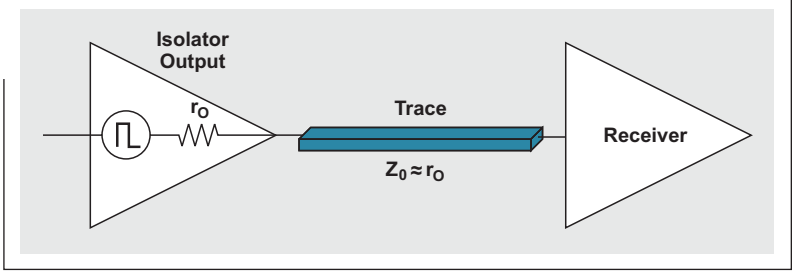


Figure 11. Isolator output characteristic

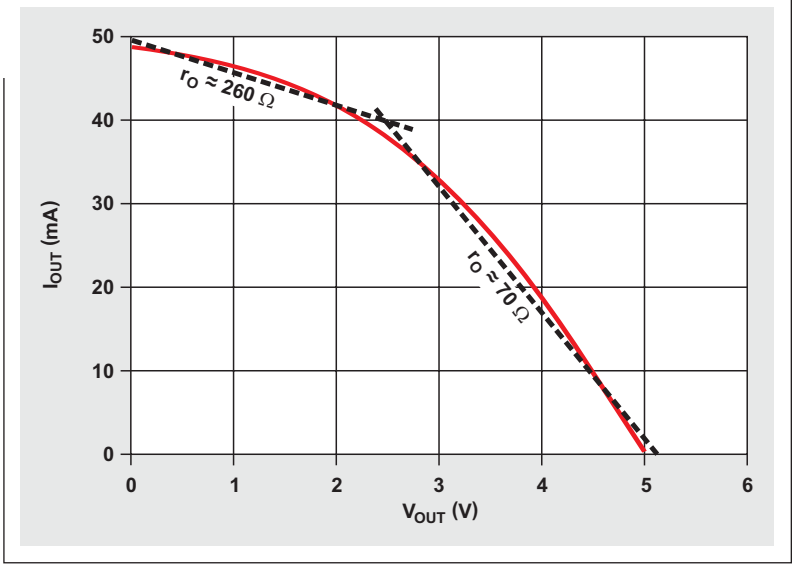


Figure 12. Characteristic impedance as a function of w/h

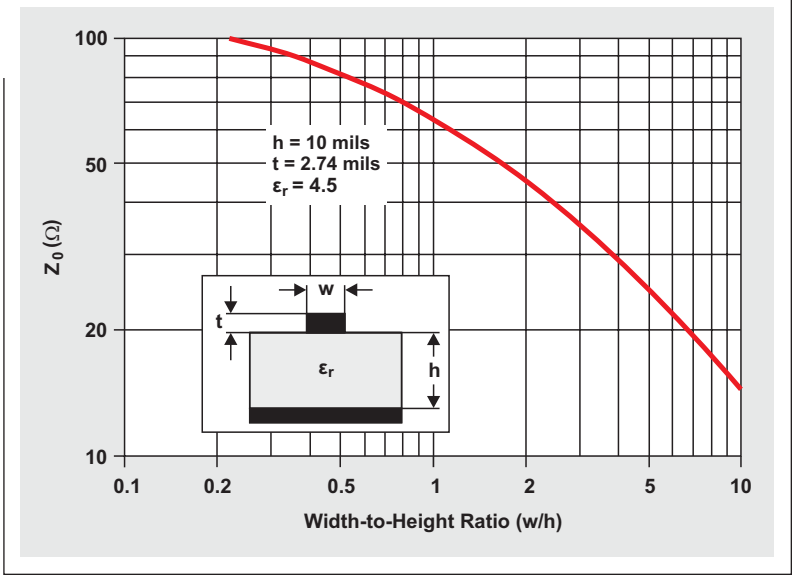
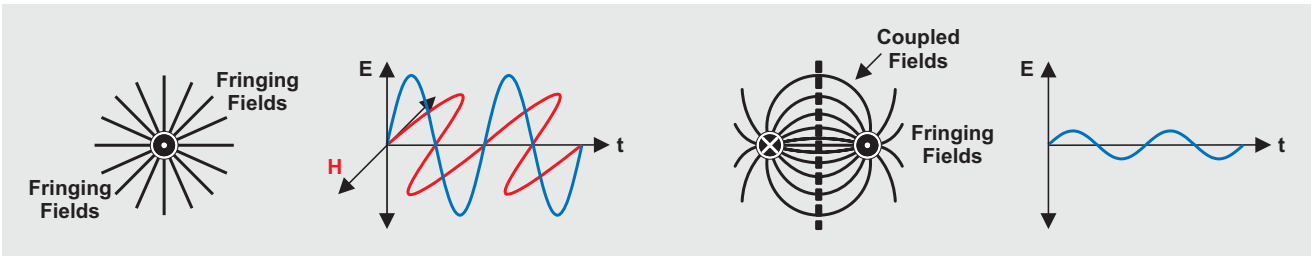


Table 2. Microstrip equations* for when 0.2 < w/h < 1

$\varepsilon_{Eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \times \left[\frac{1}{\sqrt{1 + \frac{12h}{w}}} + 0.04 \times \left(1 - \frac{w}{h}\right)^2 \right] - \frac{t}{2.3 \times \sqrt{wh}}$	ε_{Eff} = effective dielectric, taking into account: • dielectric of air • dielectric of PCB material • height above ground • nominal trace width
$w_{Eff} = w + \frac{1.25t}{\pi} \times \left[1 + \ln\left(\frac{2h}{t}\right)\right]$	w_{Eff} = effective trace width, taking into account: • nominal trace width • trace thickness • height above ground
$Z_0 = \frac{60 \times \ln\left(\frac{8h}{w_{Eff}} + \frac{w_{Eff}}{4h}\right)}{\sqrt{\varepsilon_{Eff}}}$	Z_0 = characteristic impedance, taking into account: • effective trace width • height above ground • effective dielectric

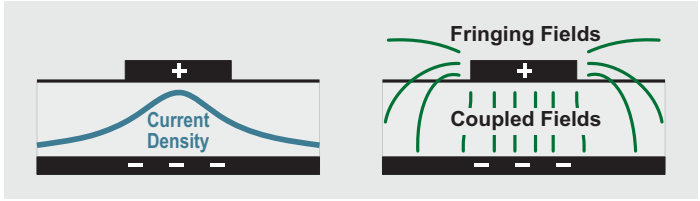
*Keep all dimensions in inches, mils (1 inch = 1000 mils), or millimeters (1 inch = 25.4 mm).

Figure 13. Reducing field fringing through close electric coupling between conductors



Note that this design example is only one of many possible ways to achieve the desired Z_0. Different trace thicknesses due to higher or lower copper plating can be used, as can a different PCB material, but these will require the w/h ratio to change. The rather complex mathematical equations for calculating the characteristic impedance, Z_0, while taking into account the trace thickness, width, and dielectric, are presented in Table 2.

Figure 14. Ground plane acting as a single return trace



Reference planes

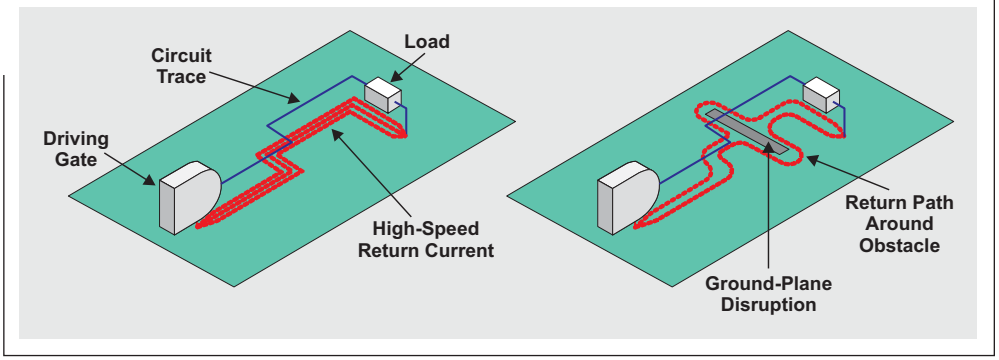
The power and ground planes of a high-speed PCB design usually must satisfy a variety of requirements. At DC and low frequencies, they must deliver stable reference voltages, such as V_{CC} and ground, to the supply terminals of integrated circuits. At high frequencies, reference planes, and ground planes in particular, serve numerous purposes. For the design of controlled-impedance transmission systems, the ground plane must provide strong electric coupling with the signal traces of an adjacent signal layer.

Consider a single, AC-carrying conductor with its associated electric and magnetic fields, shown in Figure 13. Loose or no electric coupling allows the transversal electromagnetic (TEM) wave, created by the current flow, to freely radiate into the outside environment, causing severe EMI. Now imagine a second conductor in close proximity, carrying a current of equal amplitude but opposite polarity. In this case the conductors' opposing magnetic fields cancel, while their electric fields tightly couple. The TEM waves of the two conductors, now being robbed of their magnetic fields, cannot radiate into the environment. Only the far smaller fringing fields might be able to couple outside, thus yielding significantly lower EMI.

Figure 14 shows the same effect occurring between a ground plane and a closely coupled signal trace. High-frequency currents follow the path of least inductance, not the path of least impedance. Because the return path of least inductance lies directly under a signal trace, returning signal currents tend to follow this path. The confined flow of return current creates a region of high current density in the ground plane, right below the signal trace. This ground-plane region then acts as a single return trace, allowing the magnetic fields to cancel while providing tight electric coupling to the signal trace above.

To provide a continuous, low-impedance path for return currents, reference planes (power and ground planes) must be solid copper sheets and free of voids and crevices (see Figure 15). For reference planes, it is important that the clearance sections of vias do not interfere with the path of the return current. In the case of an obstacle, the return current will find its way around it. However, when this happens, the current's electromagnetic fields will most likely interfere with the fields of other signal traces, introducing crosstalk. Moreover, this obstacle will adversely affect the impedance of the traces passing over it, leading to discontinuities and increased EMI.

Figure 15. Return-current paths in solid versus slotted ground planes



Routing

Guidelines for routing PCB traces and placing components are necessary to maintain signal integrity, avoid noise pickup, and lower EMI. Although there seem to be an endless number of precautions to be taken, only a few main layout recommendations are provided here:

1. Separate signal traces by three times the trace-to-ground height (d = 3h) to reduce crosstalk to 10% (see Figure 16). Because the return-current density under a signal trace diminishes via the function $1/[1 + (d/h)^2]$, it will be sufficiently small at a point where d > 3h to avoid causing significant crosstalk in an adjacent trace.
2. Use 45° bends (chamfered corners) instead of right-angle (90°) bends (see Figure 17). Right-angle bends increase the effective trace width and thus the trace impedance. This creates additional impedance mismatch, which might lead to higher reflections.
3. For permanent operation in a noisy environment, connect the Enable inputs of an isolator through a via to the appropriate reference plane; that is, connect high-Enable inputs to the V_{CC} plane and low-Enable inputs to the ground plane.
4. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below (see Figure 18). If a via clearance section lies in the return path, the return current will find a path of least inductance around it. By doing so, it might cross below other signal traces, thus generating crosstalk and increasing EMI.
5. Avoid routing signal traces over different layers, as this causes the inductance of the signal path to increase.
6. If, however, such routing is unavoidable, accompany each signal-trace via with a return-trace via. In this case, use the smallest via size possible to minimize the increase in inductance.

Figure 16. Separate traces to minimize crosstalk

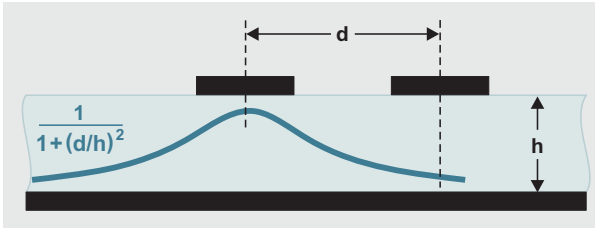
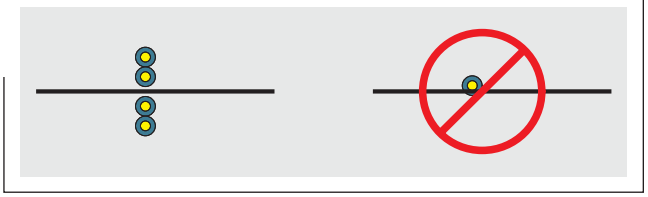


Figure 17. Use 45° bends instead of 90° bends

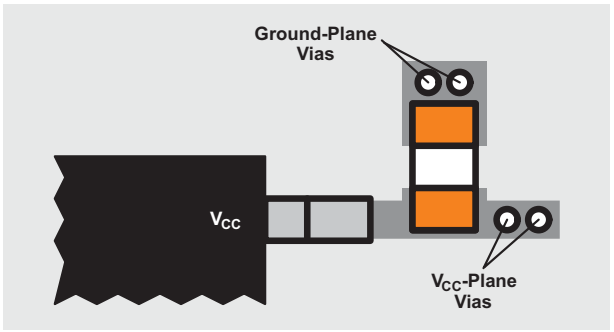
Figure 18. Avoiding via clearance sections



7. Use solid power and ground planes for impedance control and minimum power noise.
8. Use short trace lengths between the isolator and surrounding circuits to avoid noise pickup. Digital isolators are usually accompanied by isolated DC-to-DC converters that supply power across the isolation barrier. Because single-ended transmission signaling is sensitive to noise pickup, the switching frequencies of nearby DC-to-DC converters can easily be picked up by long signal traces.

9. Place bulk (i.e., 10-µF) capacitors close to power sources such as voltage regulators or where the power is supplied to the PCB.
10. Place smaller (0.1-µF or 0.01-µF) bypass capacitors close to the device to be bypassed. This can be accomplished by connecting the power side of the capacitor directly to the device's supply terminal and through two vias to the V_{CC} plane (see Figure 19). Connect the ground side of the capacitor through two vias to the ground plane.

Figure 19. Connect bypass capacitor directly to V_{CC} terminal



Vias

The term "via" commonly refers to a plated hole in a PCB. While some applications require through-hole vias to be wide enough to accommodate the leads of through-hole components, designs for high-speed boards mainly use vias to route signal traces to different layers, connect SMT components to the required reference plane, and connect reference planes of the same potential to each other.

Layers connecting to a via do so by making direct contact with a pad surrounding the via (the "via pad"). Layers that must not connect are separated by a clearance ring. Every via has a capacitance to ground that can be approximated with the following equation:

$$C = \frac{1.41 \times \varepsilon_r \times T \times D_1}{D_2 - D_1},$$

where D_2 is the diameter of a clearance hole in a ground plane (in inches), D_1 is the diameter of a pad-surround via (in inches), T is the thickness of the PCB (in inches), ε_r is the dielectric constant of the PCB, and C is the parasitic via capacitance (in picofarads). Because the capacitance increases proportionally with size, trace vias in high-speed boards should be as small as possible to avoid signal degradation caused by heavy capacitive loading.

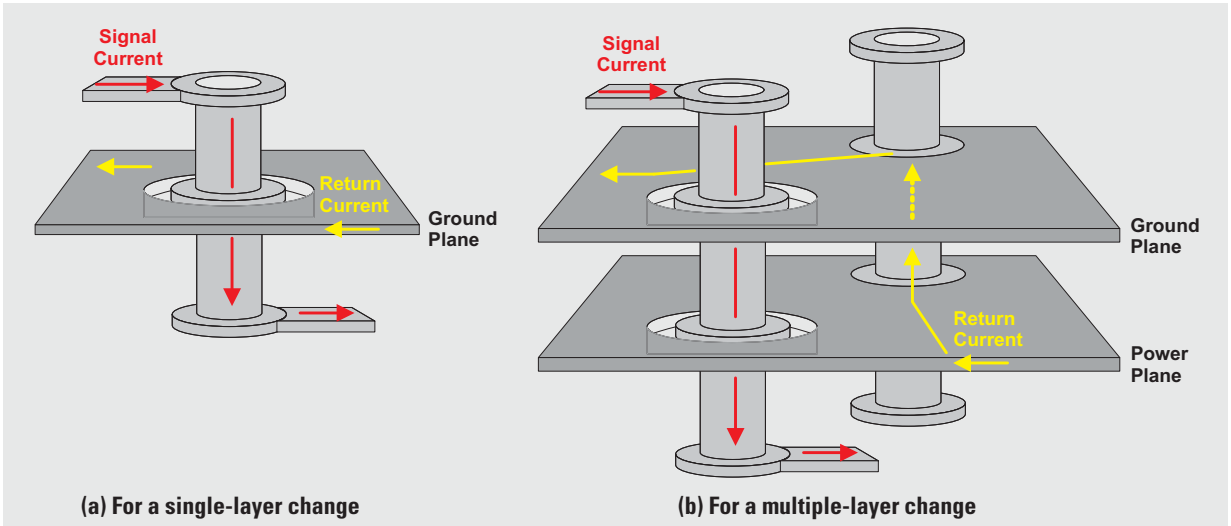
When decoupling capacitors are connected to a ground plane, or when ground planes are connected to each other, the via's inductance becomes more important than its capacitance. The magnitude of this inductance is approximated by

$$L = 5.08h \times \left[\ln\left(\frac{4h}{d}\right) + 1 \right],$$

where L is the via inductance (in nanohenries), h is the via length (in inches), and d is the via diameter (in inches). Because this equation involves a logarithm, changing the via diameter does little to influence the inductance. A big change may be effected by changing the via length or by using multiple vias in parallel. Therefore, the designer should connect decoupling capacitors to ground by using two paralleled vias per device terminal. For low-inductance connections between ground planes, multiple vias should be used in regular intervals across the board.

It is highly recommended that high-speed traces not change layers; but, if they must, the designer should ensure a continuous return-current path. Figure 20 shows the flow of the return current for a single-layer change and a multiple-layer change.

Figure 20. Continuous return-current paths

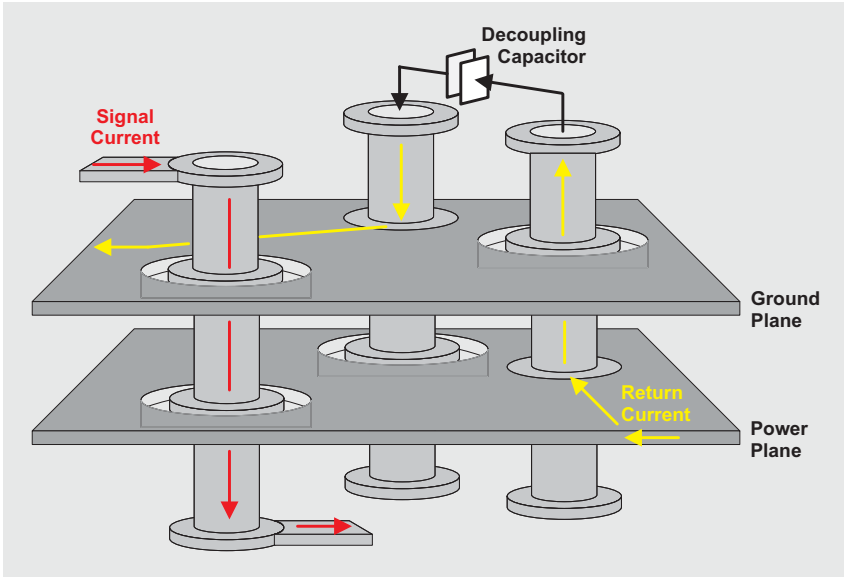


The ability for the current flow to change from the bottom to the top of the ground plane is provided by a metallic laminate of the inner clearance ring. Thus, when a signal passes through a via and continues on the opposite side of the same plane, a return-current discontinuity does not exist.

A signal trace that changes from one layer to another by crossing multiple reference planes complicates the design of the return-current path. In the case of two ground planes, a ground-to-ground via must be placed near the signal via to ensure a continuous return-current path (see Figure 20b).

If the reference planes are of different voltage potentials, such as the power and ground planes in Figure 21, the design of the return path becomes messy, requiring a third via and a decoupling capacitor. The return-current flow begins at the bottom of the power plane, where it is closest to the signal current. It then flows through the power via, across the decoupling capacitor into the ground via, and returns on top of the ground plane.

Figure 21. Return-current path for reference planes with different voltage potentials



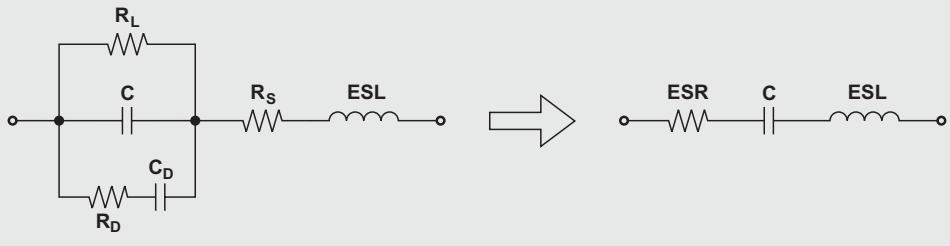
Return-current paths comprising multiple vias and decoupling capacitors possess high inductance, thus compromising signal integrity and increasing EMI. If possible, the designer should avoid changing layers during high-speed trace routing, as it usually worsens board performance, complicates design, and increases manufacturing cost.

Decoupling capacitors

Decoupling capacitors provide a local source of charge for ICs requiring a significant amount of supply current in response to internal switching. Insufficient decoupling causes a lack of supply current, resulting in signal-integrity problems and data errors. The capacitors must provide low impedance for a specific frequency range. To accomplish that, a common approach is to distribute an array of decoupling capacitors evenly across the board. In addition to maintaining signal integrity, decoupling capacitors serve as EMI filters, preventing high-frequency RF signals from propagating throughout the PCB.

Connecting a capacitor between the power and ground planes actually loads the power supply with a series resonant circuit whose frequency-dependent R-L-C components represent the equivalent circuit of a real capacitor. Figure 22 shows the parasitic components of an initial equivalent circuit and their conversion into a series resonant circuit. The leakage resistance, R_L, represents the loss through leakage current at low frequencies. R_D and C_D respectively indicate the losses due to molecular polarization and dielectric absorption. R_S depicts the resistance in the leads and plates of the capacitor. The three resistive losses are combined into one equivalent series resistance (ESR). The equivalent series inductance (ESL) combines the inductance of the capacitor plates and internal leads.

Figure 22. Capacitor losses modeled by a series resonant circuit



Note that the capacitor-connecting vias, although low in impedance, contribute a significant amount to the series inductance. Therefore, via inductance should be reduced by using two vias per capacitor terminal.

Figure 23 shows the progression of capacitor impedance, Z, versus frequency for a 10-nF capacitor. At frequencies far below the self-resonant frequency (SRF), the capacitive reactance is dominant. Closer to the SRF, the inductive reactance gains influence, trying to neutralize the capacitive component. At the SRF the capacitive and inductive reactance cancel each other, and only the ESR is effective. Note that the ESR is frequency-dependent and, in contrast to popular belief, does not reach its minimum at the SRF. However, the impedance, Z, does.

Paralleling capacitors in a distributed decoupling network works because the total capacitance increases to $C_{TOT} = C \times n$, where n is the number of decoupling capacitors used. With $X_C = 1/\omega C$, the capacitor impedance is reduced to $X_{C_{TOT}} = 1/n\omega C$ for frequencies below SRF. The same holds true for the inductance. Here $L_{TOT} = L/n$; and, because $X_L = \omega L$, the impedance decreases to $X_{L_{TOT}} = \omega L/n$ for n capacitors at frequencies above SRF.

Designing a solid decoupling network must include lower frequencies down to DC, which requires the implementation of large bypass capacitors. Therefore, to provide sufficient low impedance at low frequencies, 1-µF to 10-µF tantalums should be placed at the output of voltage regulators and at the point where power is supplied to the PCB. For the higher-frequency range, several 0.1-µF or 0.01-µF ceramics should be placed next to every high-speed switching IC.

Conclusion

Without claiming to be complete, this article covers the main aspects of PCB design with digital isolators. Following the recommendations presented will help designers accomplish an electromagnetic-compatible board design in the shortest time possible. Further information is available in the ISO72xx data sheets and EVM manuals.

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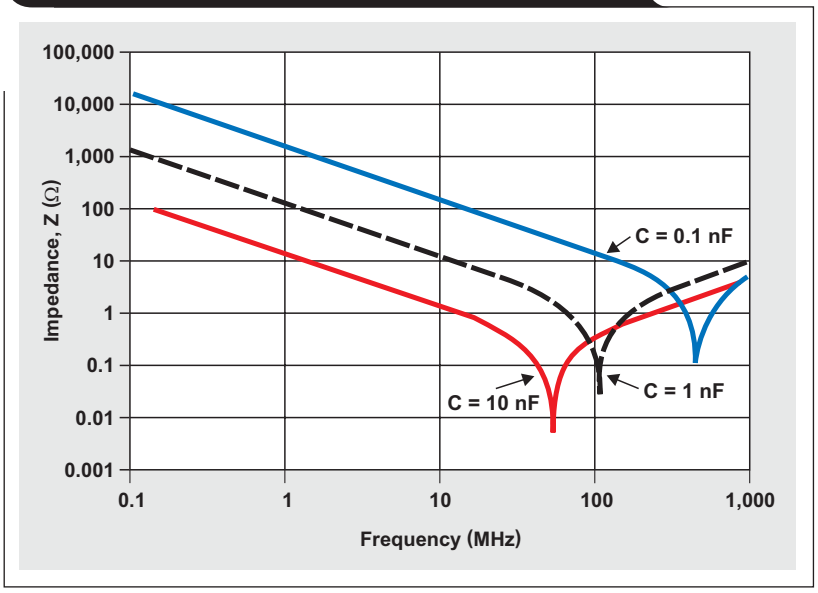
Figure 23. Capacitor impedance versus frequency



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