Designing an isolated I²C Bus® interface by using digital isolators

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The continuing changes in legislation concerning both the design and use of machinery and equipment require the isolation of almost any type of industrial system or interface. The inter-integrated circuit bus (I²C Bus®) is a single-ended, multi-master, two-wire bus; and, while designed only for short-distance I²C communication, it is no exception to isolation requirements.

The particular challenge in designing an isolated I²C interface by using standard digital isolators lies in the different operation modes between the two. The I²C Bus operates in bidirectional, half-duplex mode, while standard digital isolators are unidirectional devices. To make efficient use of one technology supporting the other, external circuitry is required that separates the bidirectional bus into two unidirectional signal paths without introducing significant propagation delay.

This article provides a short introduction to I²C Bus operation and then describes how to design an isolated I²C interface by adding only a few external components to a digital capacitive isolator.

I²C Bus operation

The I²C uses open-drain technology, thus requiring the serial data line (SDA) and serial clock line (SCL) to be connected to V_{DD} by resistors (see Figure 1). Pulling the line to ground is considered a logic "0," and letting the line float is a logic "1." This logic configuration is used as a channel-access method. Transitions of logic states must occur while SCL is low, because transitions while SCL is high indicate START and STOP conditions. Typical supply voltages are 3.3 V and 5 V, although systems with higher or lower voltages are permitted.

I²C communication uses a 7-bit address space with 16 reserved addresses, so a theoretical maximum of 112 nodes can communicate on the same bus. In praxis, however, the number of nodes is limited by the specified total bus capacitance of 400 pF, which restricts communication distances to a few meters. The specified signaling rates are 100 kbps (standard mode), 400 kbps (fast mode), 1 Mbps (fast mode plus), and 3.4 Mbps (high-speed mode).

Figure 1. The I²C Bus®

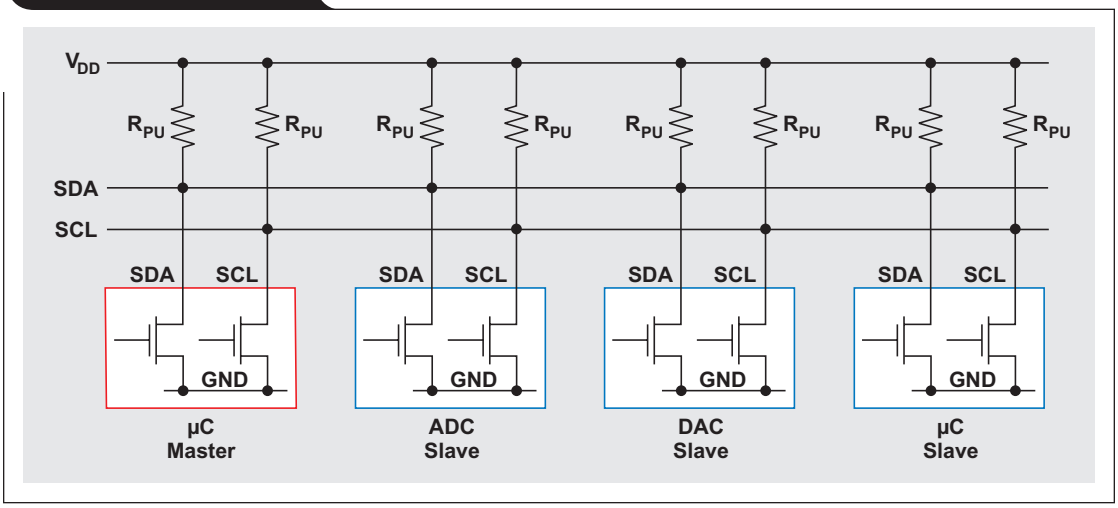
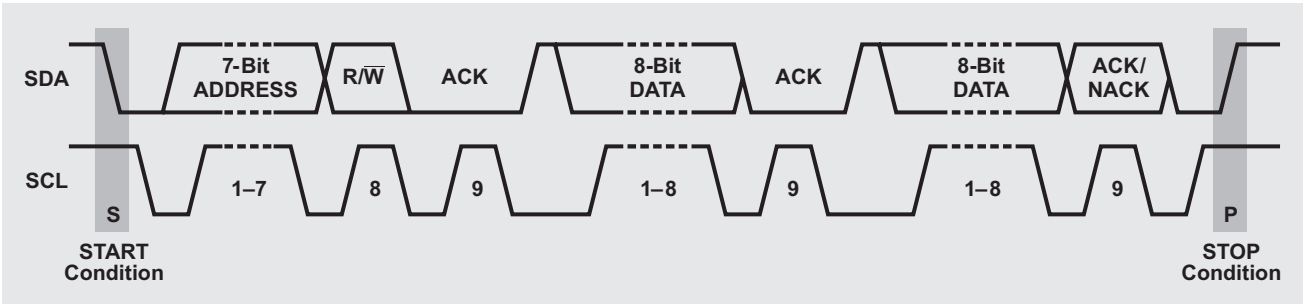


Figure 2. Timing diagram of a complete data transfer



The bus has two roles for nodes: master and slave. A master issues the clock and slave addresses and also initiates and ends data transactions. A slave receives the clock and addresses and responds to requests from the master. Figure 2 shows a typical data transfer between master and slave.

The master initiates a transaction by creating a START condition, then transmits the 7-bit address of the slave it wishes to communicate with. This is followed by a single READ/WRITE (R/W) bit, representing whether the master wishes to write to "0" or to read from "1," the slave. The master then releases the SDA line to allow the slave to acknowledge the receipt of data.

The slave responds with an acknowledge (ACK) bit by pulling SDA low during the entire high time of the ninth clock pulse on SCL. Then the master continues in either transmit or receive mode (according to the R/W bit sent), while the slave continues in the complementary mode (receive or transmit, respectively).

The address and 8-bit data bytes are sent with the most significant bit (MSB) first. The START bit is indicated by a high-to-low transition of SDA while SCL is high. The STOP condition is created by a low-to-high transition of SDA while SCL is high.

If the master writes to a slave, it repeatedly sends a byte to the slave, which sends an ACK bit for each byte received. In this case, the master is in master-transmit mode and the slave is in slave-receive mode.

If the master reads from a slave, it repeatedly receives a byte from the slave while sending an ACK bit to acknowledge the receipt of every byte but the last one (see Figure 3). In this situation the master is in master-receive mode and the slave is in slave-transmit mode.

The master ends the transmission with a STOP bit or may send another START bit to maintain bus control for further transfers.

When writing to a slave, a master mainly operates in transmit mode and changes to receive mode only when receiving acknowledgment from the slave.

When reading from a slave, the master starts in transmit mode and then changes to receive mode after sending a READ request (R/W bit = 1) to the slave. The slave continues in the complementary mode until the end of a transaction.

Note that the master ends a reading sequence by not acknowledging the last byte received—i.e., by sending a NACK bit. This procedure resets the slave state machine and allows the master to send the STOP command.

Figure 3. Changes in transmit/receive modes during a data transfer

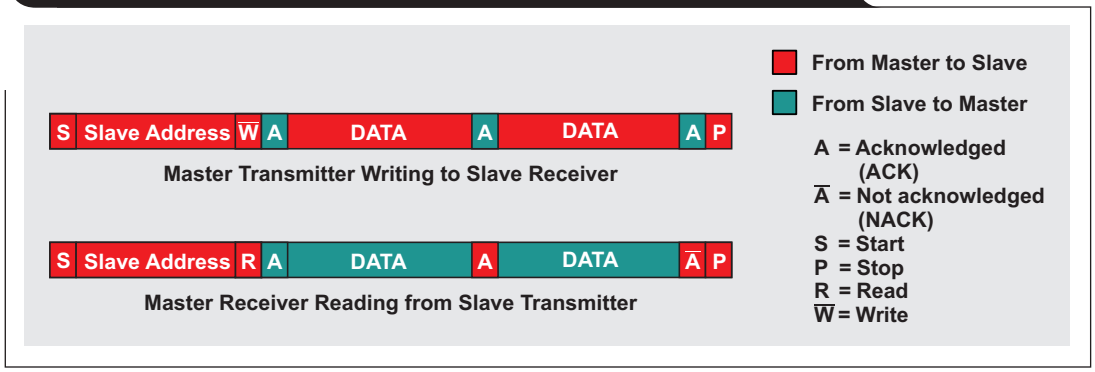
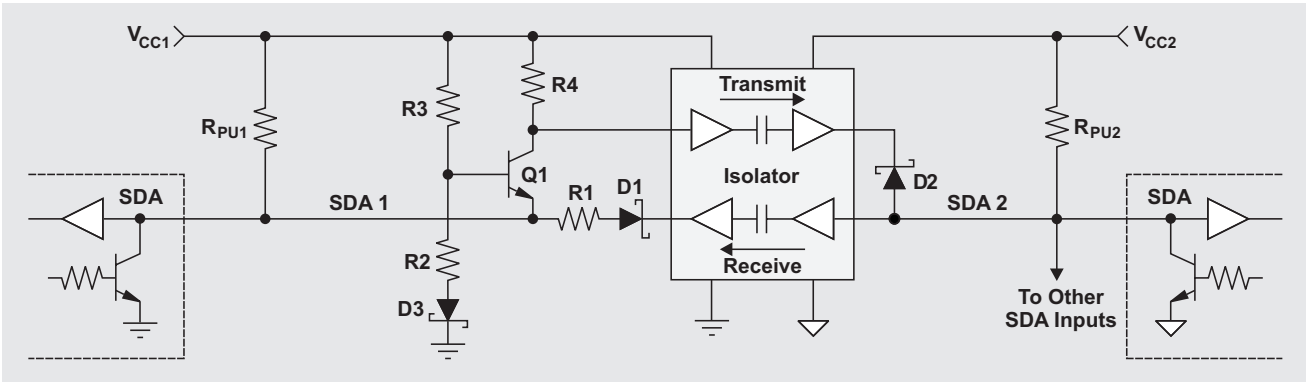


Figure 4. Isolating an I²C line by using a digital isolator



Isolator design

Isolating an I²C signal path by using standard digital isolators requires splitting the half-duplex line into separate transmit and receive paths and converting the isolator's push-pull outputs into open-collector outputs via Schottky diodes (Figure 4). To prevent a transmitted signal from feeding back to its source, a comparator function is implemented that detects the direction of the signal flow and switches the signal paths accordingly.

Transistor Q1 and its surrounding resistor network provide the comparator function. Since the dominant switching level in I²C is logic low, the base of Q1 is so biased that a low level applied to SDA1 turns the transistor on, and a low level sent from SDA2 keeps Q1 at high impedance. While the R3/R2 voltage divider primarily determines the biasing, diode D3 provides temperature compensation. To prevent SDA2 from turning Q1 on, the low-level output at D1 is raised by a voltage drop across R1, which raises Q1's emitter potential, V_E, and decreases the base-emitter voltage below the minimum turn-on level. However, care must be taken to maintain V_E below the minimum input high-level threshold of SDA1, which the I²C specification lists as $V_{IHmin} = 0.3 \times V_{CC}$.

So, when the I²C Bus at SDA2 is pulled low, the low state passing in receive direction causes a voltage increase at SDA1 that is just enough to block Q1 but well below V_{IHmin}, thus presenting a valid low for an I²C input. At the same time, R4 provides a logic high to the isolator input in transmit direction, preventing diode D2 from conducting. Once SDA2 is released and returns to the level of V_{CC2}, SDA1 follows after one propagation delay through the isolator. When the isolator is driven from the bus side (SDA2), the added signal delays for both the falling and the rising edges mainly consist of only one propagation delay through the isolator.

In the opposite direction, when SDA1 is pulled low, its maximum low-level output, V_{OLmax}, is significantly lower than V_E and causes Q1 to conduct. The low-state signal passing through the isolator in transmit direction forward biases D2, and SDA2 goes low. However, when SDA1 is released, its voltage cannot return to the level of V_{CC1} immediately due to the remaining low-level signal at SDA2. Instead, SDA1 rises to the necessary V_E potential that blocks Q1, and it will stay at this level until a high-impedance Q1 allows R4 to provide a logic high to the isolator input, thus releasing SDA2 and D1. Only then will SDA1 be able to return to the level of V_{CC1}.

When the isolator is driven from the device side (SDA1), the added signal delays for both edges increase due to the involvement of the comparator function.

Figure 5. Final isolator circuit

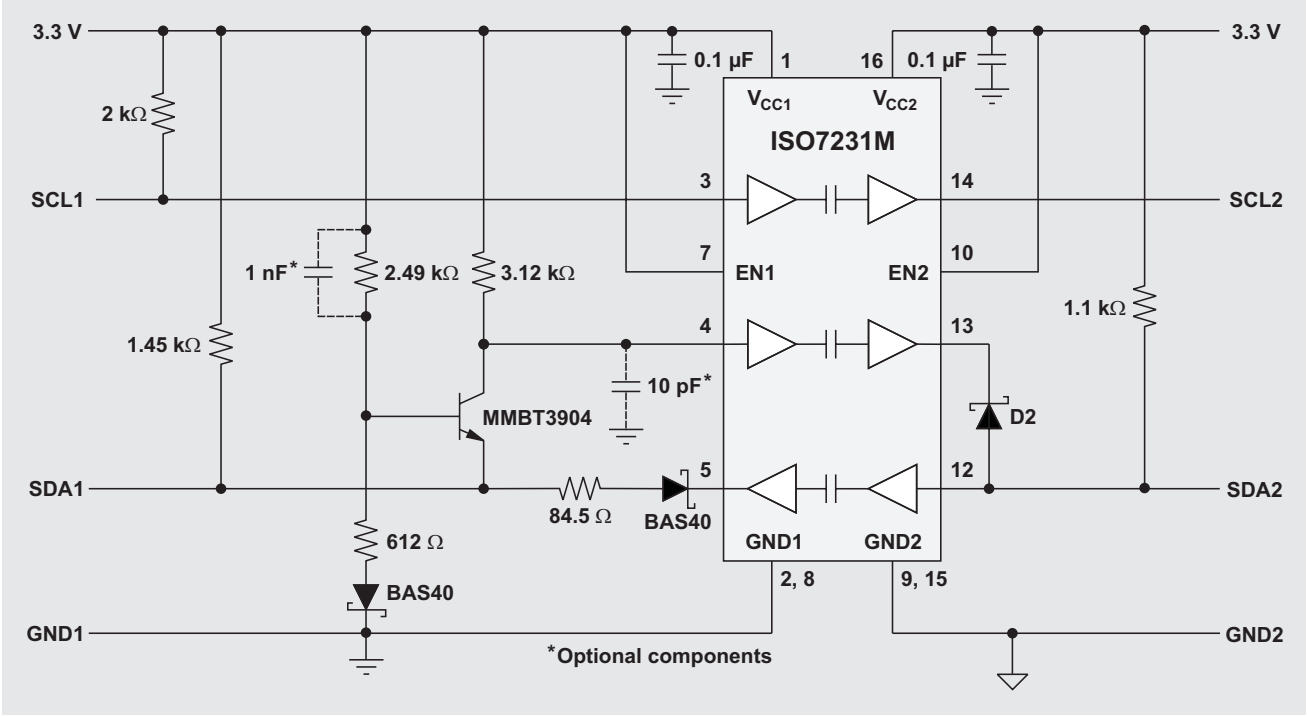


Figure 5 shows the final isolator circuit for the majority of I²C applications where the master is isolated from a slave bus. In this case, only the SDA line is bidirectional, while the SCL is unidirectional. For a multi-master system in which both lines must be bidirectional, the SDA circuit design can also be applied to the SCL when an ISO7242M isolator is used.

The typical propagation delays listed in Table 1 were measured under light capacitive loading at SDA1 and SDA2. Note that at low supply voltages, switching transients at Q1's collector might require a 10-pF filter capacitor to avoid false triggering of the internal isolator logic. Also, propagation delays can be reduced by switching a capacitor parallel to the upper base resistor to increase the charge injection into Q1's base.

Table 1. Propagation delays

SDA1 TO SDA2		SDA2 TO SDA1		CONDITION
RISING EDGE (ns)	FALLING EDGE (ns)	RISING EDGE (ns)	FALLING EDGE (ns)	
121	124	113	82	No caps
136	140	113	82	10 pF
103	136	113	82	10 pF + 1 nF
86	140	113	82	1 nF

Related Web sites

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