The IBIS model, Part 3: Using IBIS models to investigate signal-integrity issues

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This article is the third of a three-part series on using a digital input/output buffer information specification (IBIS) simulation model during the development phase of a printed circuit board (PCB). Part 1 discussed the fundamental elements of IBIS simulation models and how they are generated in the SPICE environment. Part 2 discussed IBIS model validation. The IBIS model brings a simple solution to many of the signal-integrity problems that may be encountered during the design phase. This article, Part 3, shows how to use an IBIS model to extract important variables for signal-integrity calculations and PCB design solutions. Please note that the extracted values are an integral part of the IBIS model.

**Signal-integrity problems**
When looking at a digital signal at both ends of a transmission line, the designer may be surprised at the result of driving the signal into a PCB trace. Over relatively long distances, electric signals act more like traveling waves than instantaneous, changing signals. A good analogy that describes electric-wave behavior on a circuit board is waves in a pool. A ripple travels smoothly across the pool because one volume of water has the same “impedance” as the next. However, the pool wall presents a very different impedance and reflects the wave in the opposite direction. Electric signals injected into a PCB trace experience the same phenomena, reflecting in a similar manner when impedances are mismatched. Figure 1 shows a PCB setup with mismatched termination impedances. A microcontroller,
the Texas Instruments (TI) MSP430™, transmits a clock signal to the TI ADS8326 ADC, which sends the conversion data back to the MSP430. Figure 2 shows the reflections created by the impedance mismatches in this setup. These reflections cause signal-integrity problems on the transmission lines. Matching the electrical impedance of the PCB trace at one or both ends can reduce reflections dramatically.

To tackle the issue of matching a system’s electrical impedances, the designer needs to understand the impedance characteristics of the integrated circuits (ICs) and the PCB traces that function as a transmission line. Knowing these characteristics allows the designer to model the connecting elements as distributed transmission lines.

Transmission lines service a variety of circuits, from single-ended and differential-ended to open-drain output devices, etc. This article focuses on a single-ended transmission line where the driver has a totem-pole design. Figure 3 shows the elements to use to design this example transmission line.

The following IC pin specifications are also needed:

- Transmitter’s output resistance, $Z_T$ ($\Omega$)
- Transmitter’s rise time, $t_{\text{Rise}}$, and fall time, $t_{\text{Fall}}$ (seconds)
- Receiver’s input resistance, $Z_R$ ($\Omega$)
- Receiver pin’s capacitive value, $C_{R_{\text{Pin}}}$ (F)

These specifications are usually not available in the IC manufacturer’s product datasheets. As this article will demonstrate, all of these values can be pulled from the IC’s IBIS model in the process of designing the PCB and using the model to simulate the PCB’s transmission lines.

The transmission lines are defined with the following parameters:

- Characteristic impedance, $Z_0$ ($\Omega$)
- Propagation delay, $D$ (ps/inch)
- Line propagation delay, $t_D$ (ps)
- Trace length, $\text{LENGTH}$ (inches)

This list of variables can expand, depending on the PCB design. For instance, a PCB design can have a backplane with multiple transmission/receiver points. All of the transmission-line values depend on the particular PCB. Typically, an FR-4 board’s $Z_0$ ranges from 50 to 75 $\Omega$, and $D$ ranges from 140 to 180 ps/inch. The actual values of $Z_0$ and $D$ depend on the actual transmission line’s material.

![Figure 2. Induced reflections from mismatched termination impedances in Figure 1](Image)

![Figure 3. Example single-ended transmission-line circuit](Image)
and physical dimensions. The line propagation delay on a particular board is calculated as:

\[ t_D = D \times \text{LENGTH}. \]  

(1)

For FR-4 boards, a reasonable propagation delay for a stripline (see Figure 4) is 178 ps/inch, with a characteristic impedance of 50 Ω. This can be verified on the board by measuring the line inductance and capacitance of the trace and inserting those values into the following equations:

\[ D = 10^{12} \times \sqrt{C_{TR} \times L_{TR}} \]  

(2)

or

\[ D = 85 \, \text{ps/inch} \times \sqrt{e_r}, \]  

(3)

and

\[ Z_0 = \frac{L_{TR}}{C_{TR}}. \]  

(4)

\[ C_{TR} \] is the trace line capacitance in farads/inch; \( L_{TR} \) is the trace line inductance in henrys/inch; 85 ps/inch is the dielectric constant for air; and \( e_r \) is the material dielectric constant. For instance, if the microstrip-board line capacitance is 2.6 pF/inch, and the line inductance is 6.4 nH/inch, then \( D = 129 \, \text{ps/inch} \) and \( Z_0 = 49.4 \, \Omega \).

**Lumped versus distributed circuits**

Once the transmission lines have been defined, the next step is to determine whether the circuit layout represents a lumped or a distributed system. Generally, a lumped circuit is small, and a distributed circuit requires much more space on the board. A small circuit is one that has an effective length (LENGTH) that is smaller than the fastest electrical feature in the signal. To qualify as a lumped system, the circuit on the PCB must meet the following requirement:

\[ \text{LENGTH} < \frac{t_{\text{Rise}}}{6 \times \sqrt{L_{TR} \times C_{TR}}}, \]  

(5)

where \( t_{\text{Rise}} \) is the rise time in seconds.

With a lumped-circuit implementation on the PCB, termination strategies become a non-issue. Fundamentally, it is assumed that the driver signals transmitted into the transmission lines arrive at the receiver instantaneously.

**Data organization in an IBIS model**

An IBIS model includes data for three, six, or nine corners, depending on the IC’s power-supply voltage range. The variables governing these corners are the silicon process, the power-supply voltage, and the junction temperature. The specific process/voltage/temperature (PVT) SPICE corners of a device’s models are critical for creating an accurate IBIS model. The silicon process varies from nominal to weak to strong models. The designer defines the voltage settings from the component’s power-supply requirements and varies them between nominal, minimum, and maximum values. Finally, the temperature settings at the component’s silicon junction are determined from the component’s specified temperature range, the nominal power dissipation, and the package’s junction-to-ambient thermal resistance, or \( \theta_{JA} \).

Table 1 shows an example of the three PVT variables and their relationships for a CMOS process with TI’s ADS129x family of 24-bit biopotential-measurement ADCs. These variables are used to perform the SPICE simulation six times. The first and fourth simulations use the nominal process models, the nominal power-supply voltage, and the junction at room temperature. The second and fifth simulations use the weak process models, a low power-supply voltage, and a high junction temperature. The third and sixth simulations use the strong process models, a higher power-supply voltage, and a lower junction temperature. The relationships between the PVT values map the optimum corners for a CMOS process.

**Table 1. PVT simulation corners for ADS1296 IBIS model**

<table>
<thead>
<tr>
<th>CORNER NUMBER</th>
<th>SILICON PROCESS*</th>
<th>POWER-SUPPLY VOLTAGE (V)</th>
<th>TEMPERATURE (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Nominal</td>
<td>1.8</td>
<td>27</td>
</tr>
<tr>
<td>2</td>
<td>Weak</td>
<td>1.85</td>
<td>85</td>
</tr>
<tr>
<td>3</td>
<td>Strong</td>
<td>2.0</td>
<td>–40</td>
</tr>
<tr>
<td>4</td>
<td>Nominal</td>
<td>3.3</td>
<td>27</td>
</tr>
<tr>
<td>5</td>
<td>Weak</td>
<td>3.0</td>
<td>85</td>
</tr>
<tr>
<td>6</td>
<td>Strong</td>
<td>3.6</td>
<td>–40</td>
</tr>
</tbody>
</table>

*The standard for TI’s IBIS models is nominal = typical, weak = minimum, and strong = maximum.
Finding and/or calculating transmitter specifications

The required transmitter specifications for a signal-integrity evaluation are the output impedance ($Z_T$) and the rise and fall times ($t_{\text{rise}}$ and $t_{\text{fall}}$, respectively). Figure 5 shows the package listing from the IBIS model file, ads129x.ibs, for TI's ADS1296. The values that are used to produce the impedance are shown under the “[Pin]” keyword and are also within the buffer models (not shown). The rise and fall times are located in the transient portions of the IBIS model's data listing.

Impedances of input and output pins

The pin impedance of any signal consists of the package inductance and capacitance added to the model's impedance. In Figure 5, the keywords “[Component],” “[Manufacturer],” and “[Package]” describe a specific package, a 64-pin PBGA (ZXG). The package inductance and capacitance for specific pins can be found under the “[Pin]” keyword. For instance, at pin 5E for the signal GPIO4, the $L_{\text{pin}}$ and $C_{\text{pin}}$ values are given. The $L_{\text{pin}}$ (pin inductance) and $C_{\text{pin}}$ (pin capacitance) values for this signal and package are 1.4891 nH and 0.28001 pF, inclusive.

The second capacitance value of interest is the silicon capacitance, $C_{\text{comp}}$. The $C_{\text{comp}}$ values can be found under the “[Model]” keyword in the model DIO_33 listing from the ads129x.ibs file (see Figure 6). $C_{\text{comp}}$ in this model is the capacitance of the DIO buffer with 3.3 V applied to the power-supply pin. The “|” symbol indicates a comment; so the active $C_{\text{comp}}$ values in this listing are 3.0727220e-12 F (typical), 2.3187130e-12 F (minimum), and 3.8529520e-12 F (maximum), from which the PCB designer can choose. During the design stage of the PCB transmission lines, the typical value of 3.072722 pF is an appropriate choice.
The input and output impedances can be critical to signal transmission. The following equation defines the characteristic impedance of the IBIS model pins:

\[ Z_T = Z_R = \sqrt{\frac{L_{\text{pin}}}{C_{\text{pin}} + C_{\text{comp}}}} \]  

(6)

**Output rise and fall times**

Across the industry, the convention for rise- and fall-time specifications is to use the time needed for the output signal to swing between 10% and 90% of the rail-to-rail signal, which is usually 0 to \( V_{\text{DD}} \). The IBIS Open Forum’s definition for rise time is the same and was adopted because of the long tails on CMOS switching waveforms.

Output, I/O, and three-state models within the IBIS model have specifications embedded under the “[Ramp]” keyword for \( R_{\text{load}} \) (test load), \( \frac{dV}{dt}_{r} \) (rise time), and \( \frac{dV}{dt}_{f} \) (fall time). The range of the rise- and fall-time data is from 20 to 80% of the voltage-output signal. If the denominator of the typical \( \frac{dV}{dt}_{r} \) values is multiplied by 0.8/0.6, the rise-time value will change from a 20-to-80% swing to a 10-to-90% swing. Please note that the data represents a buffer with the resistive load, \( R_{\text{load}} \).

In the ads129x.ibs file, \( R_{\text{load}} \) is the load, so the data does not extend to \( V_{\text{DD}} \). The resulting number from this calculation will provide an appropriate value for \( t_{\text{rise}} \) for the various transmission-line calculations such as \( f_{\text{rise}}, f_{3 \text{dB}} \), and rising-edge lengths.

**Using IBIS to design transmission lines**

This article started out by discussing a PCB with mismatched termination impedances. The IBIS model was then used to understand and find the critical elements for this transmission problem. At this point, it is only fair to show that there is a solution to this problem. Figure 7 shows the termination-correction strategy, and Figure 8 shows the corrected waveforms.
To design PCB transmission lines, the first step is to gather information from the product datasheet. The second step is to examine the IBIS model to find the parameters that cannot be gleaned from the datasheet—input/output impedance, rise time, and input/output capacitance. It makes sense to use the IBIS model to find key product specifications and to simulate the final design before going to the hardware stage.

References
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