How to Design an Inexpensive HART Transmitter

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ABSTRACT
This application report provides details for designing an inexpensive HART transmitter.

Process measurement and control devices can communicate via the conventional 4- to 20-mA current loop by utilizing the highway addressable remote transducer (HART) protocol. This protocol uses frequency-shift keying (FSK) with the frequencies of 1200 Hz and 2200 Hz. Here one 1200-Hz cycle represents a logic 1, while two 2200-Hz cycles represent a logic 0. Because the average value of the FSK waveform is always zero, the analog 4- to 20-mA signal is not affected.

Ideally, the FSK signal consists of sine waves of the two frequencies superimposed onto the DC measurement signal. However, generating phase-continuous FSK sine waves is a rather complex matter. Therefore, in order to simplify the generation of HART signal waveforms, the physical layer of the HART specification defines parametric limits into which the amplitude, shape, and slew rate of a more generalized waveform must fall. In this case, a trapezoidal waveform, with the limiting values detailed in Figure 1, suits this application well.

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<tr>
<th>PARAMETER</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
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<tbody>
<tr>
<td>( V_{pp} )</td>
<td>0.4 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>( I_{pp} )</td>
<td>0.8 mA</td>
<td>1.2 mA</td>
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<tr>
<td>Slew Rate at 1200 Hz</td>
<td>1 V/ms</td>
<td>4 V/ms</td>
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<tr>
<td></td>
<td>2 mA/ms</td>
<td>8 mA/ms</td>
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<tr>
<td>Slew Rate at 2200 Hz</td>
<td>2 V/ms</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4 mA/ms</td>
<td></td>
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Figure 1. Minimum and Maximum Values of Trapezoidal HART Current Waveform
The HART transmitter in Figure 2 provides a simple and inexpensive solution that generates a trapezoidal HART waveform, superimposes it onto a variable DC level, and subsequently converts the resulting output voltage into the loop current.

![Figure 2. Low-Cost HART Transmitter](image)

The HART FSK signal, commonly generated by a local microcontroller unit (MCU), is applied to the input of a first NAND gate, G1. A second output of the MCU’s general purpose I/O port serves as an active-high ENABLE signal. G1 controls two further NAND gates, G2 and G3, whose outputs connect together via high-impedance voltage dividers, \( R_1 \) and \( R_2 \).

A second voltage divider, consisting of \( R_4 \) and \( R_5 \), splits the 5-V supply into a reference voltage of \( V_{REF} = VCC/2 \), or 2.5 V. As long as ENABLE is low, G2’s output is low and G3’s output is high. Due to high-impedance loading, the NAND outputs provide rail-to-rail capability; and, with \( R_1 = R_2 \), the input voltage at A1’s non-inverting input, \( V_{IN} \), is also 2.5 V.

When ENABLE is taken high, the outputs of G2 and G3 toggle in phase with each other, thus creating a small square wave at \( V_{IN} \) that swings symmetrically about \( V_{REF} \). The peak-to-peak amplitude of \( V_{IN} \) is given in Equation 1:

\[
V_{IN(PP)} = V_S \times \frac{R_3}{R_3 + R_1||R_2}
\]

where \( V_S \) is the positive 5-V supply, and \( R_1 || R_2 \) is the parallel combination of \( R_1 \) and \( R_2 \).

Inserting the resistor values from Figure 2 into the preceding equation yields an input-voltage swing of \( V_{IN(PP)} = 200 \) mV, making \( V_{IN} \) swing between 2.4 and 2.6 V. When \( V_{IN} \) rises to 2.6 V, A1’s output goes immediately into positive saturation and charges \( C_3 \) via \( R_6 \) and \( R_7 \). The actual HART voltage on \( C_3 \) (\( V_{HART} \)) rises linearly until it reaches 2.6 V. At this point, amplifier A1 rapidly exits saturation and acts as a voltage follower, thus holding \( V_{HART} \) at 2.6 V. When \( V_{IN} \) decreases to 2.4 V, A1’s output goes into negative saturation and discharges \( C_3 \) via \( R_6 \) and \( R_7 \). \( V_{HART} \) then ramps down linearly until it reaches 2.4 V, at which point A1 comes out of saturation and again acts as a voltage follower, holding \( V_{HART} \) at 2.4 V.

The resulting trapezoidal waveform is equal in amplitude to \( V_{IN} \) and swings symmetrically about \( V_{REF} \). Its slew rate is determined by:

\[
\frac{dV}{dt} = \frac{V_{SAT} - V_{HART}}{C_3} = \frac{R_6 + R_7}{C_3}
\]

where \( V_{SAT} \) is the positive or negative output-saturation voltage of A1.
Because the AC content of $V_{\text{HART}}$ is small compared to $V_{\text{SAT}}$, $V_{\text{HART}}$ can be approximated by its quiescent level, $V_{\text{REF}}$. Also, A1’s rail-to-rail output capability in combination with the high-impedance loading through $R_6$ yields output saturation levels of 5 V and 0 V. Given that $R_7$ is much smaller than $R_6$, the preceding expression simplifies to:

$$\frac{dV}{dt} = \frac{\pm V_{\text{REF}}}{R_6 \times C_3}$$

(3)

If the component values for $R_6$ and $C_3$ from Figure 2 are inserted, the trapezoid’s slew rate results in ±1.25 V/ms.

Scaling the peak-to-peak amplitude of $V_{\text{HART}}$ (200 mV) to a HART peak-to-peak current signal of 1 mA makes the voltage slew rate of 1.25-V/ms equivalent to a current slew rate of 6.25 mA/ms in the HART current signal, which perfectly fits within the given limits of Figure 1.

$R_7$ is required to isolate A1’s output from the large capacitive load, $C_3$, in order to maintain closed-loop stability. The required value depends on A1’s unity-gain bandwidth, $f_T$, and the values of $R_6$ and $C_3$. A good approximation for $R_7$ is accomplished with:

$$R_7 \approx \frac{1 + \frac{8}{\pi} \times f_T \times R_6 \times C_3}{2 \pi \times f_T \times C_3}$$

(4)

$A_1$ must have a reasonably wide frequency response and be able to slew significantly faster than the HART trapezoid. The OPA2374, a low-cost dual operational amplifier from Texas Instruments (TI), provides a sufficiently fast slew rate of 5 V/$\mu$s and a unity-gain bandwidth of $f_T = 6.5$ MHz. In addition, the amplifier outputs have rail-to-rail drive capability with a typical quiescent current of 585 $\mu$A per amplifier.

The second amplifier, $A_2$, superimposes the HART signal onto a variable DC voltage, $V_{\text{DC}}$. The voltage at $A_2$’s output, $V_{\text{OUT}}$, becomes:

$$V_{\text{OUT}} = \left( V_{\text{REF}} \times \frac{R_{10}}{R_9 + R_{10}} + V_{\text{DC}} \times \frac{R_9}{R_9 + R_{10}} \right) \times \left( 1 + \frac{R_{11}}{R_8} \right) - V_{\text{HART}} \times \frac{R_{11}}{R_8}$$

(5)

Making $R_8$ to $R_{11}$ equal in value simplifies this equation to:

$$V_{\text{OUT}} = V_{\text{REF}} + V_{\text{DC}} - V_{\text{HART}}.$$  

(6)

Because $V_{\text{HART}}$ consists of a 200-mV trapezoid swinging symmetrically about $V_{\text{REF}}$, the output of $A_2$ contains only the small HART waveform riding on the variable DC level. Feeding $V_{\text{OUT}}$ into TI’s XTR115 voltage-to-current converter makes each 200 mV of $V_{\text{DC}}$ equivalent to 1 mA of current. Thus, varying $V_{\text{DC}}$ from 0.8 V to 4.0 V is equivalent to a 4- to 20-mA current range.

Resistors $R_8$ to $R_{11}$ should be large enough to minimize the loading effects on $C_3$’s charging current but not so large as to introduce errors through $A_2$’s input-offset current. Well-matched resistor values remove $V_{\text{REF}}$ entirely from $V_{\text{OUT}}$ so that $V_{\text{OUT}} = V_{\text{DC}} \pm 100$ mV. Therefore, a mismatch in $R_4$ and $R_6$ or variations in the voltage supply have little effect on $V_{\text{OUT}}$’s DC content.

The XTR115 is a two-wire, precision, current-output converter that transmits analog 4- to 20-mA signals over an industry-standard current loop. The device provides accurate current scaling as well as functions for limiting output current. Its on-chip 5-V voltage regulator is used to power the external circuitry. To ensure control of the output current, $I_{\text{OUT}}$, the current-return pin, $I_{\text{RET}}$, serves as a local ground and senses any current used in the external circuitry. Its input stage has a current gain of 100, which is set by the two laser-trimmed gain resistors, $R_{G1}$ and $R_{G2}$:

$$\text{Gain} = 1 + \frac{R_{G1}}{R_{G2}}$$

(7)
Therefore, an input current, $I_{IN}$, produces an output current, $I_{OUT}$, equal to $I_{IN} \times 100$. With the voltage potential at $I_{IN}$ being 0 (referenced to $I_{RET}$), the resistor value required to convert an input voltage into a defined output current is calculated with:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{V_{IN}}{I_{OUT}} \times \text{Gain}$$

(8)

Converting the 200-mVpp HART voltage into a 1-mA current thus requires an input resistance of:

$$R_{IN} = \frac{200 \text{ mV}}{1 \text{ mA}} \times 100 = 20 \text{ k}\Omega$$

(9)

In addition, $R_{IN}$ defines the input-voltage range for a 4- to 20-mA current range with:

$$V_{DC_{\text{min}}} = \frac{R_{IN} \times I_{OUT_{\text{min}}}}{\text{Gain}} = \frac{20 \text{ k}\Omega \times 4 \text{ mA}}{100} = 0.8 \text{ V}$$

(10)

and

$$V_{DC_{\text{max}}} = \frac{R_{IN} \times I_{OUT_{\text{max}}}}{\text{Gain}} = \frac{20 \text{ k}\Omega \times 20 \text{ mA}}{100} = 4 \text{ V}$$

(11)
Conclusion

Simple operational-amplifier circuits can be used to design a low-cost HART transmitter for the conventional 4- to 20-mA current loop.

Figure 3 shows the signal voltages at various test points during a HART transmission for a DC input of 2 V. Resistor matching in the difference amplifier, A2, removes the $V_{\text{REF}}$ component in the output signal. Thus, deviations in the reference voltage have no impact on $V_{\text{OUT}}$. The output signal therefore swings symmetrically around the 2-V DC input.

![Figure 3. Signal Voltages of the HART Transmitter’s Signal Path](image-url)
References

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Related Web sites


Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2012) to A Revision

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Changed document format to current application reports standard.</td>
</tr>
</tbody>
</table>
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