

Power MOSFET failures in mobile PMUs: Causes and design precautions

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Introduction

Power MOSFETs in automotive systems and in mobile devices being charged or operated in automobiles may be subjected to harsh operating environments and intense transients from power equipment and transmitters.

Moreover, caustic contaminants in the atmosphere and on exposed conductive surfaces of circuit boards can induce low-impedance paths. Over time, these low-impedance paths and transient events like overloading, electromagnetic coupling, and inductively induced spikes from the operating environment can cause destructive electrical overstress (EOS) conditions. Such conditions may cause a large current to flow across a MOSFET power switch in a very short time.

This article addresses special design considerations and failure analysis of high-frequency switchers and regulators employing external feedback components for mobile and automotive applications. The goal is to help familiarize designers with various mechanisms and circumstances that may lead to destruction of on-chip power switches. Techniques for averting and eliminating the effects of EOS conditions are discussed to help improve end-user products and PCB designs. This article also presents tips for conducting lab tests and suggests good engineering practices to obviate potential problems from occurring in high-density/ultracompact mobile designs.^{1, 2}

Case studies

In 2011, a designer reported a shorted NMOS switch in the step-down DC/DC converter of the Texas Instruments (TI) LM26484 PMU during in-house testing. This regulator was designed into a new instrumentation panel. The banks of LEDs powered by a buck converter were operating in light-load conditions. TI asked the designers to monitor the voltage at the supply pins around the clock for transients above 6 V. They confirmed that transient spikes were peaking at over 8 V for hundreds of nanoseconds, which occurred frequently. The device's absolute maximum limit on the supply pin is $V_{IN} = 6\text{ V}$!

It was suspected that a parasitic NPN (formed by n+ (S), p- (well), and n+ (D) as shown in Figure 1) may have turned on hard when the p- (well) base biased up the emitter from n+ (S), a classic EOS scenario in power devices. Figure 2 shows an equivalent-circuit model of a MOSFET device with parasitic components.

Figure 1. Cross-section of a typical MOSFET structure and relevant parasitic elements

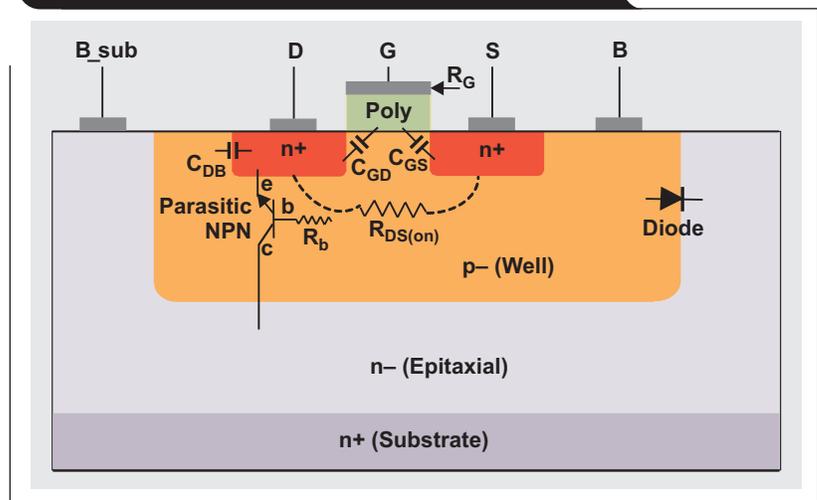
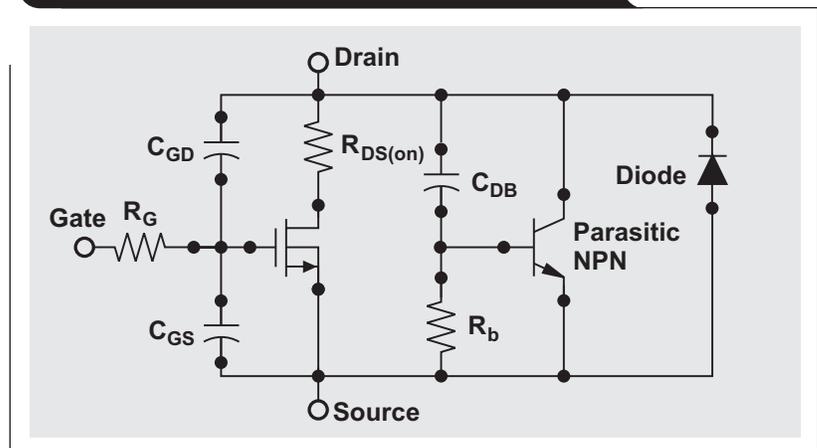


Figure 2. Model of a typical MOSFET with associated parasitic elements



Examining the PCB layout (Figure 3) revealed that the top traces of the power pins had a single via tapped into the power plane, and their longer tracks made the bypass capacitors ineffective. To prevent this situation from arising again, TI has suggested improved design guidelines. For example, adequately large bulk capacitors need to be added between the V_{IN} and ground planes. Also, local bypassing needs to be augmented with additional capacitors covering broader frequency bands. These precautions, shown implemented in Figure 4, will keep large transients from stressing the PMU's integrated circuit.

A more involved solution for eliminating EOS is to place the bypass capacitors closer to the power and ground pins, as shown in Figure 5. Note that the power-ground tracks have been widened and include liberal use of larger vias. This recommendation became a viable solution for the customer.

In 2012, another customer reported experiencing some failures with another PMU of the same family that had dual buck converters and dual LDOs. The buck-converter switches either shorted out or opened soon after the system left the factory. This PMU was powered from a stepped-down supply in an automotive application. With many infotainment and safety systems becoming standard equipment in cars starting in 2014, the PMU production rate is projected to increase by approximately tenfold, creating a concern for all parties involved. Although no anomalies have been discovered in the customer's rigorous testing for device- and board-level stress, some infrequent failures have occurred. In general, there are many known mechanisms and opportunities involved in vehicular applications that potentially could induce abnormal input-voltage transients, leading to device damage.

Common causes of EOS

Many EOS conditions on PMUs arise from inadequate design considerations or overlooking subtle parasitics in some systems. This is especially true in industrial/automotive applications, wherein unusual ambient conditions or differences in the electromechanical layout can manifest reliability issues. EOS can also be related to the manufacturing process, testing, and component aging.

The following discussion presents some of the most common EOS culprits. Appropriate design tips and suggestions are included to help designers eliminate EOS problems. A typical means of identifying failure mechanisms is well-documented. It is strongly suggested that readers seeking more information also study the physics of failure via failure-mode mechanisms and effects analysis (FMMEA).

Figure 3. PCB with two LM26484s provides four buck converters and two LDOs

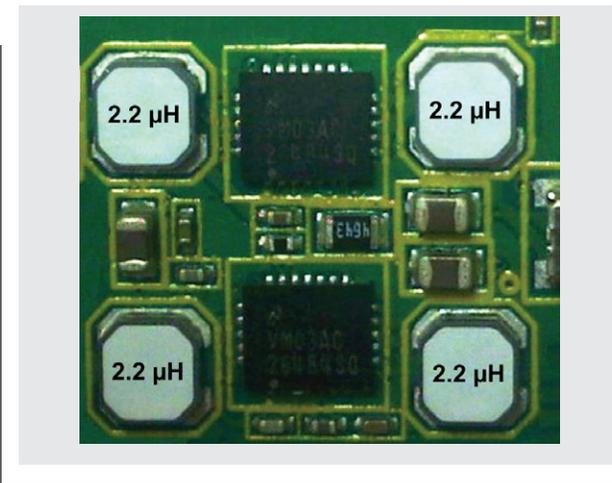


Figure 4. Example of a more robust line filter and bypass

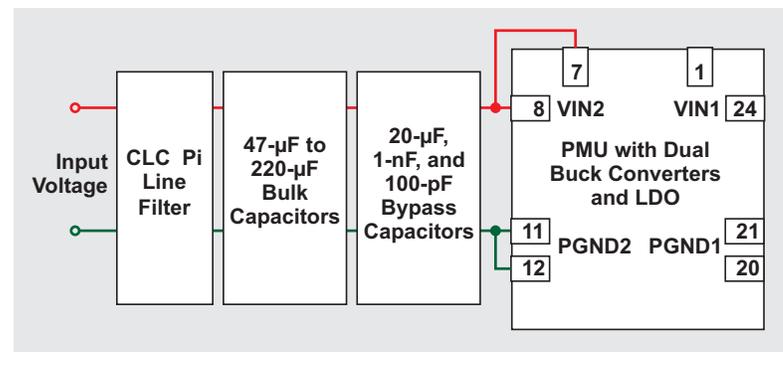
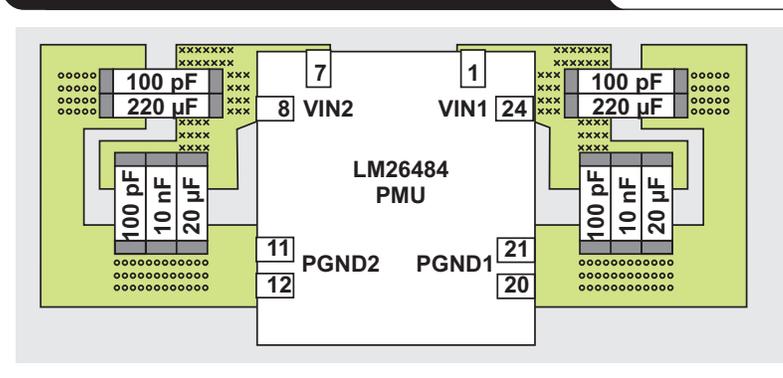


Figure 5. Improved layout with bypass capacitors closer to power and ground pins



EOS caused by battery and wiring in automotive applications

Whenever a vehicle's 12-V battery voltage falls too low, as in cold weather and cranking operations, the onboard PMU's control, timing, and decision-making circuits may malfunction before undervoltage lockout (UVLO) comes to its rescue. As a result, undesirable effects such as shoot-through and disengaged clamping can stress the MOS switches and cause permanent damage over time.

High-voltage, fast edge-rate transients are another commonly encountered cause of instantaneous device damage. Another example, load dumping, is when the 12-V battery is momentarily removed from the alternator connection. Due to the inductive effect from the long wirings involved, the loads can experience a sudden increase in potential at over 100 V, which may last for hundreds of milliseconds before it decays to normal levels.

High-voltage spikes in fast transients can propagate from the MOSFET's drain terminal to the gate via terminal capacitance. This can rapidly bias up the gate, potentially leading to runaway conditions. Normally, slightly exceeding the recommended maximum operating supply voltage might not be a destructive event. However, when the supply voltage exceeds the maximum level and sustains sufficient energy, it can cause the device to short-circuit in a few nanoseconds or lead to an avalanche breakdown. Moreover, loose or poorly secured battery-cable connections can manifest similar high-voltage transients if subjected to strong and abrupt mechanical vibrations.

Inadequate or poor power-supply bypassing

Inadequate supply bypassing can cause abnormal operation that may lead to shoot-through stress from timing issues. A proper bypass capacitor must have a voltage rating that adequately covers peak voltage transients. Leakage and parasitic inductance from traces are among the sources that cause the largest, most severe $L(di/dt)$ overstress pulses created at the pulsing terminal of a switcher. These high-energy pulses can lead to device breakdown as previously described. Hence, taking proper precautions to eliminate unwanted inductive paths is imperative. For example, bypass capacitors should be placed as close as possible to the device rail pins. A thick metal trace should be used as much as is allowable on all high-transient paths to further cut down parasitic inductance. Finally, transient-suppressing elements or similar techniques should be used as appropriate to attenuate potentially destructive high-voltage spikes.

Shorted output from overloading and/or a defective load capacitor

When a switcher's output current (I_{OUT} load) exceeds the rated limit, built-in protection circuits usually prevent any immediate damage to the device. However, frequent over-current events can lead to accumulated EOS conditions, which over time may cause permanent device damage. Such damage is associated with the finite delay time, typically in the range of microseconds, required before the protection circuit kicks into action. Other than true loading

shorts, a defective output capacitor can effect a low-impedance path that creates a dynamic short-circuit current in parallel with the maximum loading—thus producing another continuous EOS condition.

Temporary high-overcurrent operation with synchronous switches

The MOSFET body diode generally has a long reverse recovery time compared to that of the MOSFET switch itself. If the body diode of one MOSFET is still conducting when the opposing complementary device has switched on, then a short-circuit condition similar to shoot-through occurs. This can happen due to timing issues from parasitics or from the circuit or device design (see Figures 1 and 2). Furthermore, internal parasitic inductance and capacitance can store energy that, under certain conditions, additional current may freewheel through the body diodes of the FET switches as one turns off and the other turns on. This is the classic parasitic-capacitance mechanism, $C(dv/dt)$, with high-speed switching that can lead to continuous high-peak-current transients with no dependence on load conditions.

This type of EOS increases dramatically when coupled with power-rail integrity issues as discussed before. The circumstance can be improved or eliminated with more accurate design and simulation of the power-train circuitry and/or by augmenting protective devices, such as a Schottky diode across the drain and source of the MOSFET. Using a Schottky diode is a proven technique to prevent the body diode from being turned on by the freewheeling current. Eliminating excessive undershooting below ground that could cause noise and turning on parasitic pn junctions also lends another benefit—the Schottky diodes may moderately increase switcher efficiency.

Device-failure verification and analysis

Failure analysis (FA) utilizes visual inspection, impedance measurements, X-rays, SAT.Sam, emission hot-spot OBIRCH analysis, SEM, and SCM tools and techniques, etc., to identify failure-mode mechanisms and root causes of device failure. Failure analysis also examines whether general oversights in a customer's design or manufacturing process may be the cause. When the cause is identified, TI issues relevant advisory and containment actions to internal and external customers to help prevent failure from reoccurring.

Failure-mode mechanisms

1. Electrostatic-discharge (ESD) destruction or gate surge:

Device-junction or oxide-rupture damage (a short or leakage) can occur as a result of improper handling during assembly and testing of the device and system. These mechanisms introduce electrostatic charges onto the device and/or create external high-voltage surge events that reach the switch circuit.

For example, an ESD event between a fingertip and the communication-port connectors of a cell phone or tablet may cause permanent system damage. As process-technology nodes continue to shrink, device-level ESD

protection becomes inadequate on a system level. A transorb, or a transient-voltage suppressor such as TI's TPD1E10B06 protection diode, is a good remedy.

2. Wear-and-tear mechanisms:

- A die fracture may occur in extreme temperature cycling
- Over time, high-voltage stress may induce dielectric breakdown that will become a gate-oxide short circuit
- Wire bond and metal routes can open due to EOS from current overload, etc.
- A voltage transient on the supply lines can cause damage to passive and active devices on the die

3. PCB elements and environment:

- A circuit failure may occur due to humidity, presence of a contaminant, or filaments becoming conductive
- A die fracture may occur due to shock, vibration, material fatigue, etc.
- Loss of polymer strength, known as glass transition failure, may occur under high-temperature stress
- Bypass and load capacitors may be leaky or shorted
- Inductor windings may short-circuit due to wear and tear of insulation under high-temperature stress or mechanical vibration

4. Component aging and inadequacy:

Because aging components may contribute to MOSFET failures even if they initially meet datasheet specifications,¹ manufacturing and product-engineering departments are encouraged to perform testing and burn-in of parts at ratings slightly above datasheet limits. This ensures that marginal devices with inherent wafer-defect density and random process-related issues are weeded out. It may be better to lose some yield at production than to be accountable for and spend valuable resources on field failures later on.

Failure-analysis results

In the 2012 case study mentioned earlier, where the switch's drain and source channels were fused together in an automotive application, the customer could not determine that the PMU IC, the circuit board, or the subsystem had a reliability problem. Each was rigorously tested and stressed beyond specification limits, and no failure ever surfaced. The culprit might have been the layout; the electrical plumbing; the system installation; and/or the operating conditions, such as cold cranking, a weak battery, or intermittent connection of long/loose power cabling.

Because the customer and its subcontractors were unable to reproduce the initial failure in their lab, they needed confirmation and sought assistance from TI. Examples of in-house failure-analysis results are depicted in Figures 6 and 7.

Figure 6. High-side pFET shorted to the VIN rails

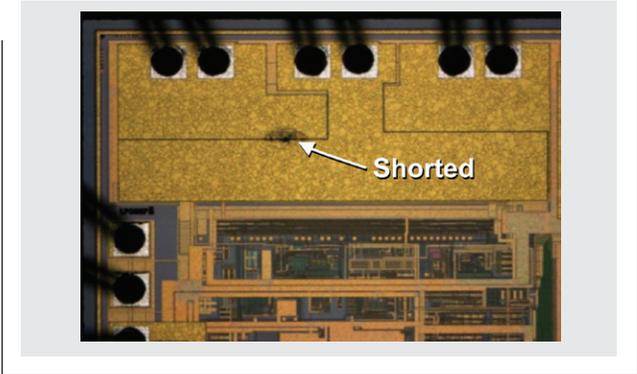
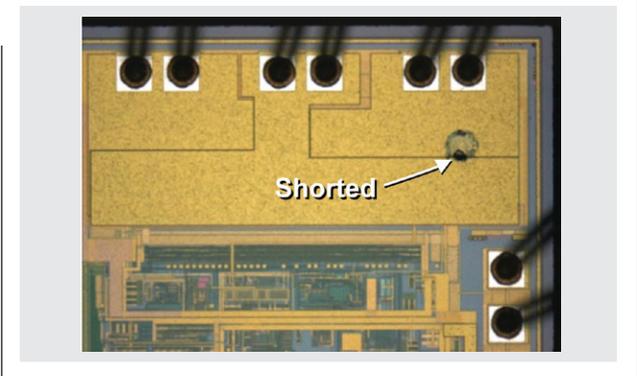


Figure 7. Low-side nFET shorted to ground



Failure analysis suggested that the burn marks reflected in the deprocessed dies were likely the consequence of EOS conditions. To validate this assumption, it was demonstrated that the failures could be induced in lab setups for (1) 5-V operation and (2) start-up conditions. By using a Keithley 2420 3-A source meter—a versatile power supply whose amplitude, frequency, and on/off times can be programmed— V_{IN} was programmed at 5 V and injected with a 50-ms pulse that repeated at 100-ms intervals. With loading at 200 mA and above, the pulse amplitude was increased at 0.5-V increments at 5-minute intervals until abnormal current was observed. The part was then decapped to visually confirm EOS. The results revealed that when the peak-to-peak pulse voltage reached approximately 7.5 V or more, the switches shorted out. Moreover, if pulses were to peak further to 9 V, the ESD structure might also be damaged.

Reproducing a short circuit from the switches during start-up was more challenging, however. With a bench supply cycling the buck converters on and off, V_{IN} issued relatively slow and smooth start-up transients and settled in at about 6 ms (Figure 8). Even with the supply set to slightly over 7 V, the switchers did not fail over days of stress testing.

In order to make the operation mimic in-vehicular conditions more closely, the cable length between the supply and the device was increased from about 30 cm to about 1.5 m. These longer wires, typically routed from the 12-V battery to the device, created more inductance. Furthermore, the soft power cycling from the power supply was replaced with a mechanical toggle switch such that the mechanical bounce and chatter behaved more like transients introduced by mechanical relay contacts (Figure 9).

The tests were conducted with the power-supply output set at 5.0 V, then the toggle switch was flip-flopped 20 times. If no overcurrent failure was detected, the supply voltage was increased by 0.2 V, the switch was again toggled on and off 20 times, and the process repeated until the part failed. The result was a stunning success! The buck converter's high- or low-side switch became shorted with the power-supply output at about 7.5 VDC. The V_{IN} pins monitored with a 10-pF probe exhibited faster turn-on transients, which caused an overshoot above 11 V in 20 μ s. The actual $L(di/dt)$ could have been a lot higher, creating a repeatable destructive EOS condition. The customer was elated that this bench setup replicated the same failures as in the field.

Conclusion

This article has discussed common device-failure mechanisms related to MOSFET transistors in integrated power-management and voltage-regulator circuits. General precautions, specific PCB layout techniques, and component-selection tips have been presented to help mitigate and eliminate EOS concerns. It is hoped that this article will help system and PCB designers be aware of the EOS effects of seemingly benign parasitic elements that can be subjected to transients in the PMU operating environment. Product and field support personnel may also find this article useful for understanding the cause and effect of EOS to facilitate their interface with customers.

Acknowledgments

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References

- 1 Kern Wong. (2012, April 27). "PCB and ESR subtleties in switching regulator and LDO designs." EDN [Online]. Available: www.edn.com

Figure 8. Power supply off/on ramping in ~6 ms

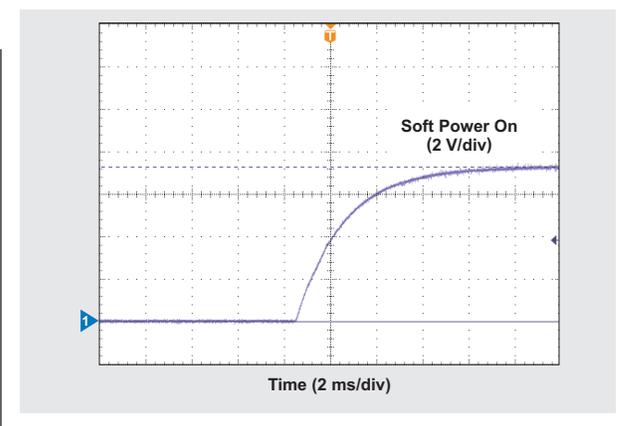
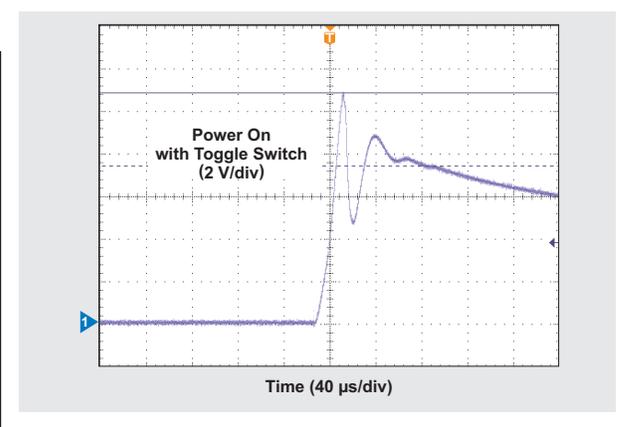


Figure 9. An 80- μ s transient induced by switch and longer wire



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- 4 "Analysis of MOSFET failure modes in LLC resonant converter," Fairchild Semiconductor, AN-9067, Nov. 5, 2009 [Online]. Available: www.fairchildsemi.com/an/AN/AN-9067.pdf

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