

Correcting cross-wire faults in modern e-metering networks

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Electricity metering (e-metering) for commercial and residential applications relies heavily on long-haul, differential data-transmission networks based on the TIA/EIA-485 standard, commonly referred to as RS-485. In order to overcome the large ground-potential differences often encountered between remotely located bus nodes, each node is galvanically isolated, with regards to signal and supply lines, from the local e-metering circuitry.

The e-metering network is a typical master/slave system in which a host processor in the master node (located in a control center) sequentially addresses multiple slave nodes (located in the individual end customer's premises) along the bus.

With a single network comprising up to 60 nodes typically, the potential for unintentionally cross-wiring the two conductors of the twisted-pair bus cable can be rather high, if neither preventive measures during network installation nor corrective measures during network operation are applied.

The e-metering companies in the United States and Europe rely heavily on trained installation personnel and visually distinctive, color-coded cabling as preventive measures. This approach allows for the use of standard transceivers and cabling, such as isolated RS-485 transceivers and CAT-5 cable.

To further reduce the risk of wiring faults, recent network designs have been implementing a so-called training

sequence that causes the slave nodes to adjust to the signal polarity of the master. During this sequence, the master broadcasts a unique bit pattern to all slaves. The same bit pattern, initially stored in each slave processor during power-up, is then compared with the pattern sent by the master. If the patterns match, the slave maintains its signal polarity. In the case of a mismatch, the slave processor inverts the signal polarity of both the incoming receive data and the outgoing transmit data. This inverting process is typically accomplished through an Exclusive-OR function within the slave processor and does not require any changes in hardware design. Thus, the proper operation of standard transceivers is still maintained.

In contrast to this approach, Asian e-metering companies push for more cost savings in network designs by using:

- Personnel inexperienced in network installation
- Low-cost, non-color-coded lamp wire instead of twisted-pair cable
- Dedicated transceivers with integrated signal-polarity correction

Figure 1 shows a typical e-metering network with SN65HVD888 polarity-correction (POLCOR) transceivers from Texas Instruments (TI). The master node contains a failsafe-biasing resistor network (R_{FS} and R_T) that determines the signal polarity on the bus. Both master and slave nodes require integrated polarity-correction logic in

Figure 1. Typical e-metering bus with POLCOR transceivers

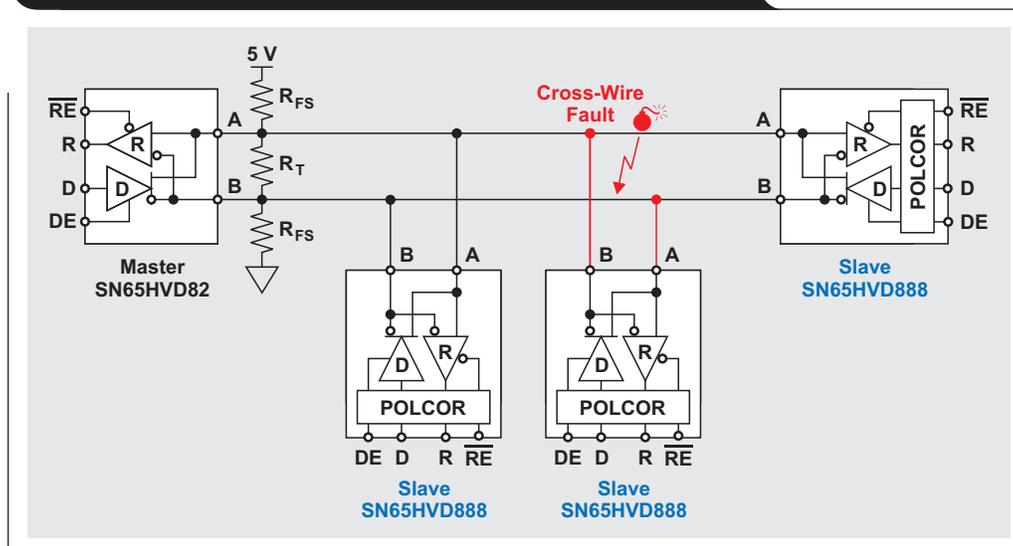
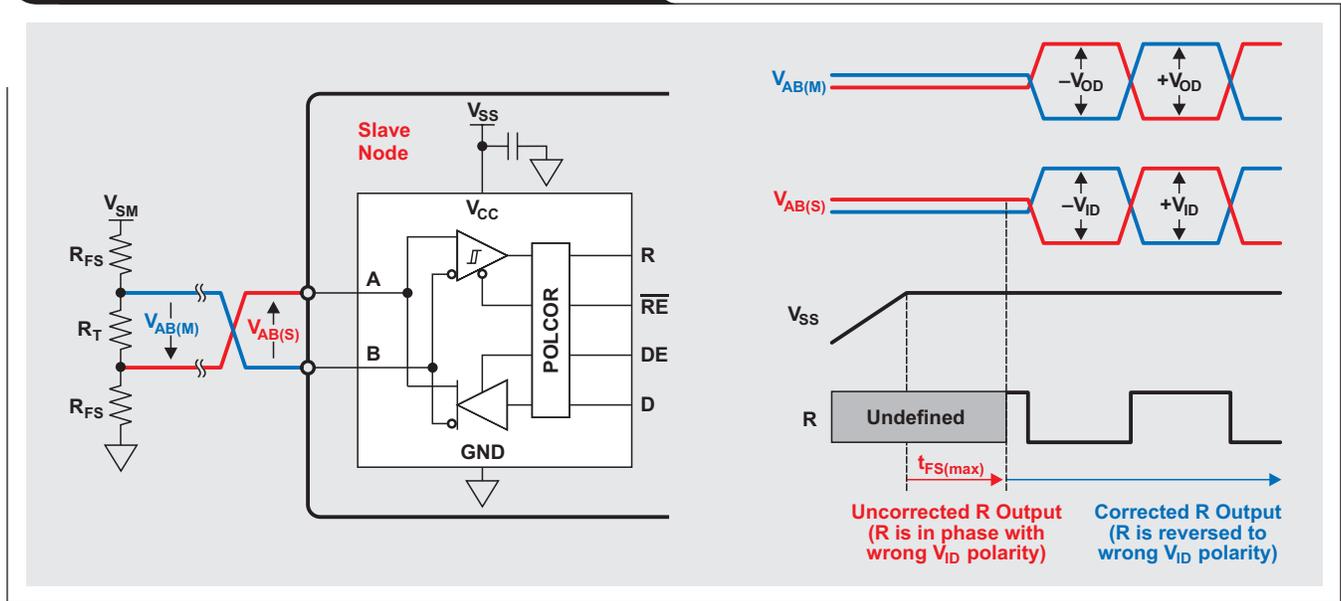


Figure 2. Polarity-correction timing after power-up



order to match the bus's signal polarity during bus idling. This correction logic consists of a debounce filter whose debounce time distinguishes between long data strings of the same signal polarity and actual bus-idle time. Due to the wide temperature range, across which the SN65HVD888 must be able to operate, the debounce time can vary between a lower limit of $t_{FS(min)} = 44$ ms and an upper limit of $t_{FS(max)} = 78$ ms.

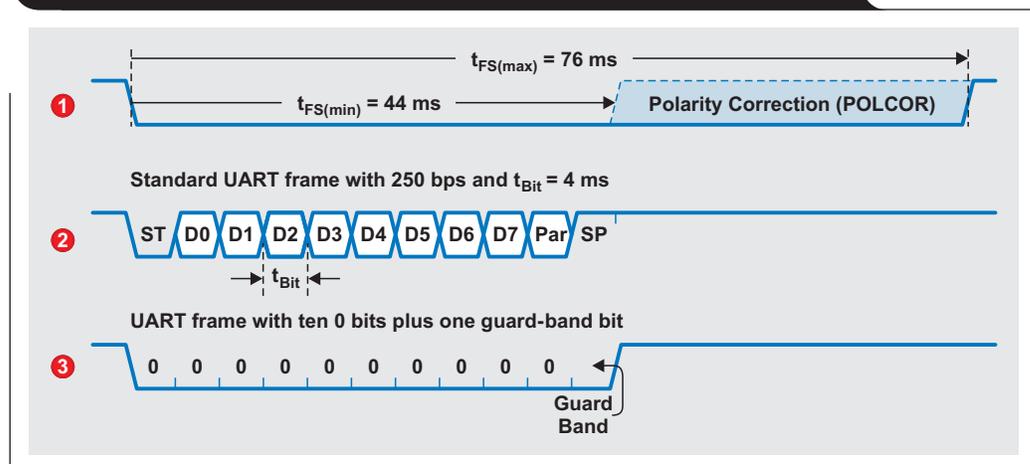
This means that a polarity correction might be initiated by a constant bus voltage that is present for as little as 44 ms. Therefore, a data string of consecutive 0 bits must be shorter than 44 ms to avoid causing polarity correction. Alternatively, an intended polarity correction, typically required after powering up the network or after the installation of a new bus node, requires a bus-idle voltage to be present for longer than 78 ms to ensure that the polarity correction is completed.

Hence, constant bus signals shorter than 44 ms are considered valid data. Those exceeding 78 ms are considered bus-idle states. Only idle states with differential voltages more negative than the negative receiver input threshold (V_{IT-}) cause the correction logic to invert signal polarity. Otherwise, a transceiver maintains its polarity status. Figure 2 gives an example of the polarity correction after a power-up sequence.

During power-up, the receiver output (R) is undefined. Once the slave-node supply (V_{SS}) is stable, the bus must idle for at least $t_{FS(max)}$ to ensure that the polarity correction is completed. Because of the cross-wire fault, the positive bus voltage at the master's failsafe network ($V_{AB(M)}$) appears negative at the transceiver input. Thus, after completion of $t_{FS(max)}$, the transceiver's internal polarity is switched to invert receive and transmit data. Hence, the negative input voltage ($V_{AB(S)}$) is converted into a positive output voltage.

The minimum debounce time of $t_{FS(min)} = 44$ ms allows for the transmission of a 250-bps UART frame with eleven 0 bits without triggering the POLCOR logic. The bit rate of 250 bps was chosen to be lower than the minimum 300 bps used in e-metering. The structure of the UART frame with its start, data, parity, and stop bits is shown in Figure 3.

Figure 3. Standard UART frame will not trigger a polarity correction



Polarity correction with DL/T645 protocol

The e-metering protocol standard DL/T645 has further provisions to distinguish between long data strings of the same polarity and bus-idle states. Figure 4 shows how an example power value of 340078.56 W is processed within slave and master nodes.

The DL/T645 protocol calls for the measured decimal value in the driving slave node to be divided into groups of two digits. Each two-digit pair is converted into hexadecimal format (indicated by “h”). When these hex values arrive at the driver input, a 33h value is added. The resulting sum pattern is then transmitted through the driver output across the bus towards the master.

At the receiving master input, 33h is subtracted from the incoming sum pattern, thus yielding the original raw transmit data. Further, data processing converts the hex values back into decimal format.

Figure 5 shows a DL/T645-compliant data frame operating at the minimum rate of 300 bps and compares it to the minimum debounce time of 44 ms. Here the DL/T645 protocol requires a string of ten 0 bits (eight data bits plus the start and parity bits) to be converted into a bit sequence with a maximum of two consecutive 1 or 0 bits. However, because the start bit is always 0, a maximum of three consecutive 0 bits can occur at the beginning of a frame. Their combined duration of 10 ms, however, is far too short to cause an unintentional polarity correction.

Based on the three 0 bits at the frame start, it can be determined how far the data rate can be safely reduced when one bit is added as a guard band. If the four bits are spread across the 44-ms time window, the bit interval becomes 11 ms. This results in a minimum data rate of 1/11 ms ~ 91 bps. Therefore it is safe to say that the SN65HVD888 transceiver supports DL/T645-compliant data rates down to 100 bps.

Figure 4. Adding 33h to raw transmit data ensures short bit strings of the same polarity

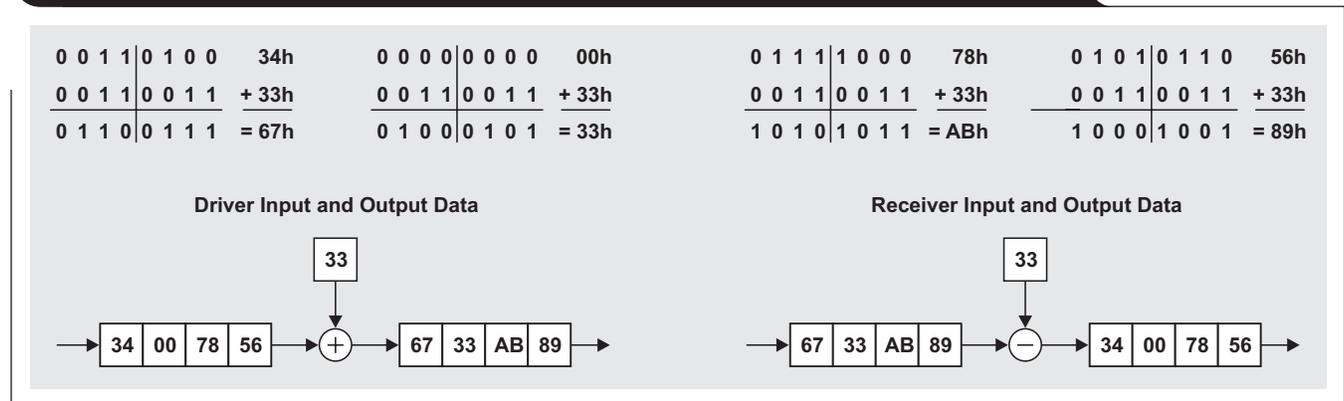


Figure 5. DL/T645-compliant data frame does not falsely trigger polarity correction

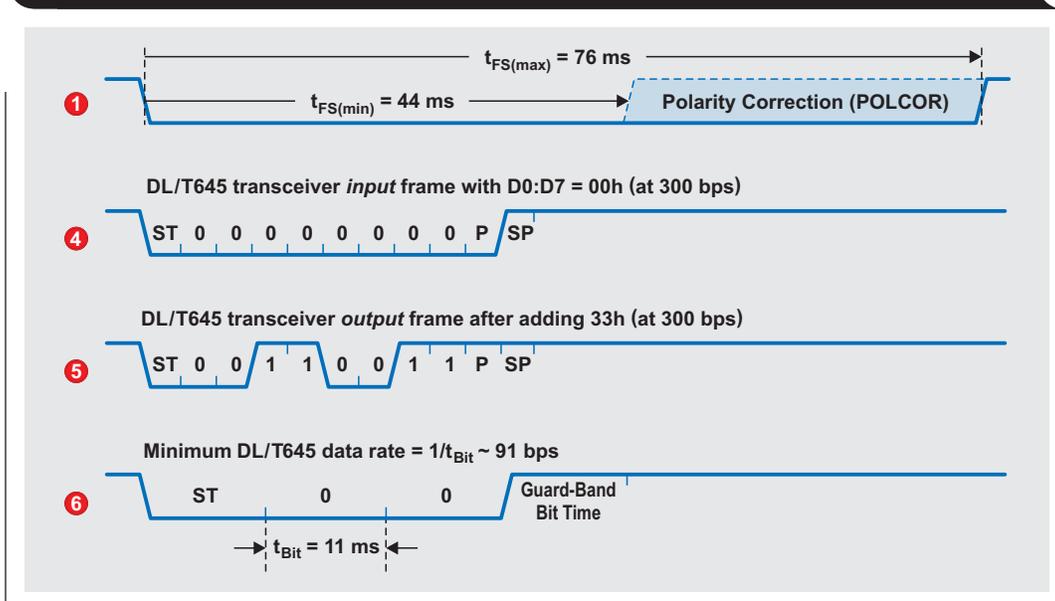
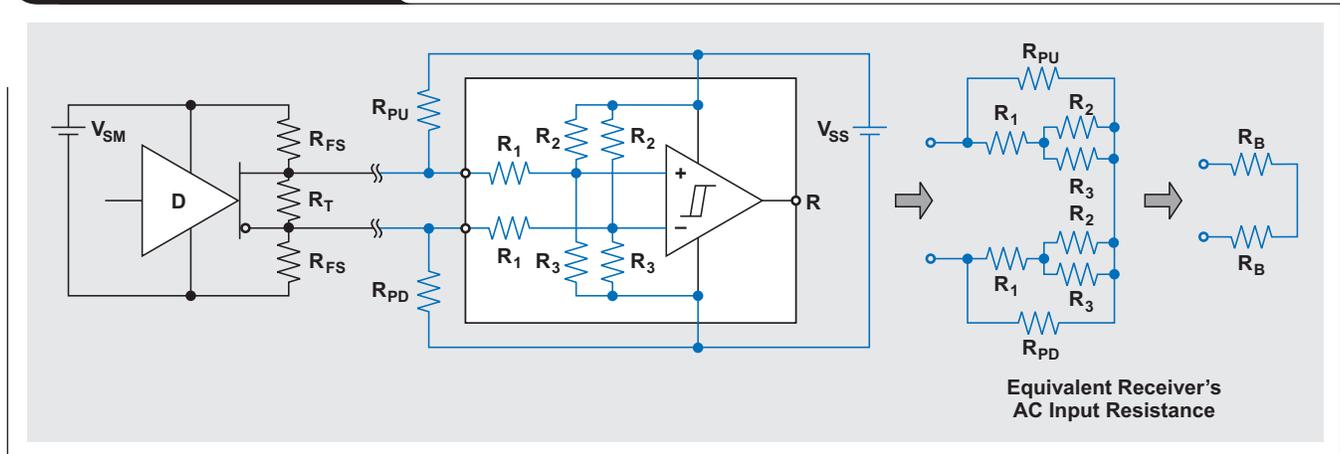


Figure 6. Simplified data link



Bus loading

To determine the maximum number of slave nodes the master can drive, two load conditions are evaluated—dynamic or AC loading, and static or DC loading.

AC loading

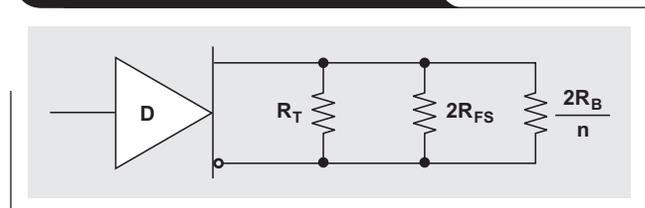
AC loading exists during data transmission when the master commands a slave to send data and the slave responds to this request. During this normal operation, signal transients occur on the bus that are affected by the capacitances of the bus cable, node connectors, transceiver inputs, and power supplies. To minimize the effect of capacitive reactance on the signal, e-metering networks operate at low data rates of 300 bps to 20 kbps. Therefore, the following discussion considers only resistive loads.

Figure 6 shows a simplified data link between a master, its failsafe-biasing network, and a remotely located slave receiver. Due to their large capacitance, the voltage supplies of the master (V_{SM}) and the slave (V_{SS}) can be seen as short circuits for AC signals. Hence, for the master node, the two failsafe resistors (R_{FS}) are connected in series and lie parallel to the termination resistor (R_T). The slave nodes are connected in a similar way. Here the internal DC-bias resistors (R_2 and R_3) are in parallel to one another, and their combined resistance is in series to a typical high-impedance R_1 . Occasionally external pull-up/pull-down resistors (R_{PU} and R_{PD} , respectively) are used to further bias the node input. These resistors do nothing but load the bus because they lie in parallel to the internal resistance network of the receiver.

Note that when R_{FS} is kept between 1 and 2 k Ω , it is sufficient to bias the entire bus with a low-impedance biasing network at the master without further biasing at the slave nodes.

The resulting equivalent AC circuit is shown in Figure 7. Here $2R_B/n$ represents the input resistance of multiple (n) transceivers. Because the EIA-485 standard specifies a maximum differential driver load of $R_L = 54 \Omega$, the parallel

Figure 7. Equivalent AC network



combination of all resistances on the bus must not exceed this value. This requirement is expressed in Equation 1:

$$\frac{1}{R_L} = \frac{1}{R_T} + \frac{1}{2R_{FS}} + \frac{n}{2R_B} \quad (1)$$

Solving for n yields Equation 2, which gives the maximum number of bus nodes that should be used under an AC-loading condition:

$$n = 2R_B \times \left(\frac{1}{R_L} - \frac{1}{R_T} - \frac{1}{2R_{FS}} \right) \quad (2)$$

Two commonly applied network designs are as follows:

1. The master uses a failsafe network with $R_T = 120 \Omega$ and $R_{FS} = 1 \text{ k}\Omega$, while each slave is biased with external pull-up/pull-down resistors of $R_{PU} = R_{PD} = 20 \text{ k}\Omega$, so that $R_B \sim 18 \text{ k}\Omega$. Under these conditions, the maximum number of potential nodes on the bus is limited to

$$n = 2 \times 18 \text{ k}\Omega \times \left(\frac{1}{54 \Omega} - \frac{1}{120 \Omega} - \frac{1}{2 \text{ k}\Omega} \right) = 348 \text{ nodes.} \quad (3)$$

2. The other scenario uses no termination resistor and rather high-impedance failsafe resistors of 10 k Ω . Also, the slave nodes operate without external biasing ($R_{PU} = R_{PD} = \infty$). In this case, R_B consists of only the receiver's internal resistance, which for the SN65HVD888 is 184 k Ω

per input. Due to this high-impedance loading, the theoretical number of bus nodes increases drastically to

$$n = 2 \times 184 \text{ k}\Omega \times \left(\frac{1}{54 \text{ }\Omega} - \frac{1}{40 \text{ k}\Omega} \right) = 6805 \text{ nodes.} \quad (4)$$

These two examples yield rather high numbers of bus nodes in comparison to the average e-metering network comprising only 40 to 60 nodes. The next section, “DC loading,” shows that the AC-loading evaluation is misleading, as it does not consider the bus’s leakage currents caused by the bus-node supplies.

DC loading

DC loading occurs during bus idling when no transceiver is actively driving the bus. In this state, the supply of the master (V_{SM}) drives current through the nearby failsafe network to establish a positive bus failsafe voltage (V_{FS}). This voltage determines the signal polarity for all slave nodes. Like the master supply, the slave supply (V_{SS}) drives current through its internal resistor network. Part of this current leaks through the input resistance (R_1) into the bus. The remaining current then flows through R_T and returns through R_1 of the opposite terminal (Figure 6).

Correctly wired nodes drive currents through R_T in the same direction as the master supply. However, cross-wired nodes drive current in the opposite direction through R_T . This reduces the combined current through R_T , and with it the failsafe voltage (V_{FS}). At a certain number of cross-wired nodes, V_{FS} can become so small that it falls within the receiver’s input sensitivity, causing all bus nodes to assume indeterminate output states. To avoid this condition, the failsafe network at the master must be dimensioned so that even if all slaves are cross-wired, a positive V_{FS} is still maintained.

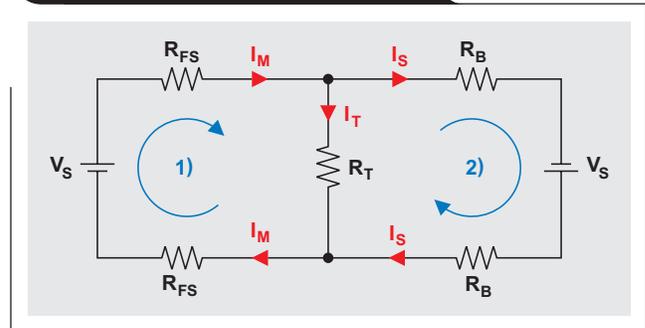
Figure 8 illustrates this scenario for only one slave node in order to simplify the mathematical derivations of the voltage and current relations within the network. Because V_{SM} equals V_{SS} , both supplies are simplified to V_S .

Equations 5 and 6 describe the two existing voltage loops, while Equation 7 expresses the current in the upper summing node:

$$-V_S + I_M \times 2R_{FS} + I_T \times R_T = 0 \quad (5)$$

$$-V_S + I_S \times 2R_B - I_T \times R_T = 0 \quad (6)$$

Figure 8. Equivalent DC network



$$I_T = I_M - n \times I_S \quad (7)$$

Note that in Equation 7, the slave current (I_S) is multiplied by a factor n , indicating multiple slave nodes.

The master and slave currents are determined by solving Equation 5 for I_M and Equation 6 for I_S , yielding Equations 8 and 9, respectively:

$$I_M = \frac{V_S - I_T \times R_T}{2R_{FS}} \quad (8)$$

$$I_S = \frac{V_S + I_T \times R_T}{2R_B} \quad (9)$$

Inserting the equations for I_M and I_S into Equation 7 and substituting I_T with V_{FS}/R_T gives

$$\frac{V_{FS}}{R_T} = \frac{V_S \times (R_B - R_{FS} \times n)}{R_B \times (2R_{FS} + R_T) + R_{FS} \times R_T \times n}. \quad (10)$$

Solving Equation 10 for R_{FS} provides the failsafe resistor value necessary to keep V_{FS} positive:

$$R_{FS} = \frac{V_S - V_{FS}}{2V_{FS}/R_T + n \times (V_S + V_{FS})/R_B}. \quad (11)$$

For applications without a termination resistor ($R_T = \infty$), Equation 11 simplifies to

$$R_{FS} = \frac{R_B \times (V_S - V_{FS})}{n \times (V_S + V_{FS})}. \quad (12)$$

Figure 9 shows the values of R_{FS} and the master supply current (I_M) as functions of bus-node count. Figure 9a was created by using Equation 11, assuming a termination resistor of $120\ \Omega$. Figure 9b was created by using Equation 12, assuming no termination. Both figures were created for a failsafe voltage of $110\ \text{mV}$.

Figure 9c shows the master supply current (I_M) for both cases. Despite the low-impedance load of $120\ \Omega$, I_M in the failsafe network with termination is merely $1\ \text{mA}$ larger than I_M in the network without termination.

Conclusion

The SN65HVD888 POLCOR transceiver provides polarity correction for cross-wired bus cables by means of debounce filtering. The filter's minimum debounce time ($t_{FS(\min)}$) determines the maximum duration of consecutive bits of equal polarity, while its maximum debounce time ($t_{FS(\max)}$) determines the minimum bus-idle time for a complete signal-polarity correction.

The SN65HVD888 requires polarity correction only after a power-up sequence. Once completed, the polarity status is stored within the transceiver and consistently applied to both receive and transmit data. Switching the transceiver between transmit and receive mode does not alter the polarity status.

The transceiver supports DL/T645 data rates well below $300\ \text{bps}$. The recommended failsafe-biasing network uses a $120\text{-}\Omega$ termination resistor and two $1.1\text{-k}\Omega$ failsafe-biasing resistors.

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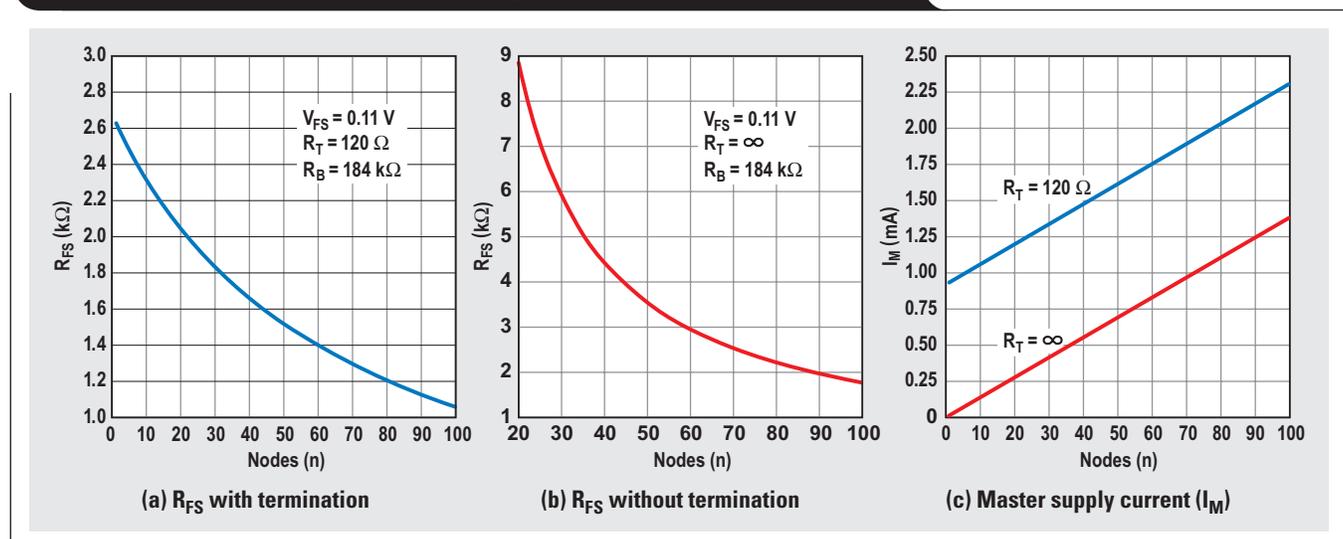
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Figure 9. Effects of failsafe resistance (R_{FS}) with and without termination



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