Distortion and source impedance in JFET-input op amps

By John Caldwell
Analog Applications Engineer

Designers of low-distortion analog circuits in industrial data acquisition, seismic measurement, and high-fidelity audio are aware that many operational amplifiers (op amps) produce greater distortion when configured as non-inverting amplifiers. In the non-inverting configuration, the input signal appears as a common-mode signal at both inputs. The subtraction performed by the op amp on the two inputs is finite and slightly non-linear, producing a small amount of additional distortion at the op amp output. This effect is often referred to as common-mode distortion.[1]

It is less widely known that some op amps show more severe common-mode distortion when the input-signal source has a high output impedance. Using the TL072, a JFET-input general-purpose op amp, let’s compare the output distortion for two source impedances. Figure 1 shows the TL072’s output distortion when the source impedance is 20 Ω and 10 kΩ. The total harmonic distortion and noise (THD+N) is substantially increased in the 10-kΩ case – more than could be attributed to the additional source resistor.

This behavior is typical of older JFET-input op amps like the TL072 and limits their usability in many circuits such as Sallen-Key active filters.[2]

At the time, JFETs offered some advantages over bipolar transistors when used as the input devices of an op amp. For example, the reduced current noise allowed JFET-input op amps to be used in high-impedance applications. Furthermore, JFETs could be fabricated with the existing bipolar semiconductor processes, giving them a major advantage over MOSFETs.

Figure 2 shows the cross section of a p-channel JFET fabricated using ion implantation on a p-type substrate in a junction-isolation process.[3] The channel was formed by implanting p-type impurities into an n-type region. An n-type region is then implanted on top of the channel (n-type top gate) and connected to the region below the channel to form the gate.

The junction between the p-type substrate and n-type gate acts as a reverse-biased diode. This allows the JFET to have extremely low input current, while creating a parasitic capacitance (C_GSS) from the gate to the substrate.

At the interface of p-type and n-type semiconductor material, a process of diffusion occurs where electrons and holes migrate across the interface leaving behind charged ions on their respective sides. The migrating charge carriers recombine with the opposing charge carriers from the opposite side and are eliminated, which produces an area with no mobile charge carriers. This area is called the depletion region because the mobile charge carriers have been depleted. In this region, the semiconductor material behaves as an insulator. The resulting structure resembles a capacitor with n- and p-type regions being the conductive electrodes, and the depletion region acts as the dielectric. Due to the large contact area between the gate...
and the substrate, the gate-to-substrate capacitance, \( C_{GSS} \), is typically much larger than the gate-to-source and gate-to-drain capacitances.\(^3\) Therefore, the \( C_{GSS} \) of the input JFETs is the dominant contributor to the input common-mode capacitance of these op amps.

Like all capacitors, the capacitance of the p-n junction is dependent on the area of its electrodes and the distance they are separated. Although the area of the junction is fixed, the width of the depletion region is not. It depends on the direction and intensity of the electric field across the depletion region.

During the initial diffusion, the ions left behind by the diffusing charge carriers produce an electric field which opposes further diffusion. This is called the built-in voltage of the junction. The application of an external voltage to the junction has the effect of growing or shrinking the width of the depletion region and changing the capacitance of the junction. The gate-to-substrate capacitance of a JFET varies as a function of gate-to-substrate voltage according to the equation:

\[
C_{GSS} = \frac{C_{GSS0}}{1 + \frac{V_{GSS}}{\psi_0}}
\]

In Equation 1, \( C_{GSS0} \) is the junction capacitance at 0 V, \( V_{GSS} \) is the gate-to-substrate voltage. Further, \( \psi_0 \) is the built-in voltage of the junction, which typically is about 0.7 V. In most op amps, the substrate is held at the negative supply voltage (\( V_{EE} \)). Therefore, as the common-mode voltage changes, the \( V_{GSS} \) term in Equation 1 changes, which increases or decreases the gate-to-substrate capacitance, \( C_{GSS} \).

In Figure 3, input common-mode capacitances, \( C_{CM1} \) and \( C_{CM2} \), were added to represent \( C_{GSS} \) of the input JFETs.

The input common-mode capacitance of the non-inverting input, \( C_{CM1} \), must be charged and discharged by a small current, \( I_S \), from the input source, \( V_S \). If the input capacitance is not a constant, but depends on the input voltage, the charging current drawn from the source is no longer linearly related to the rate-of-change of the input voltage signal:

\[
I_S \neq C_{CM1} \frac{dV_S}{dt} \rightarrow I_S = \frac{C_{GSS0}}{1 + \frac{V_{IN} - V_{EE}}{\psi_0}} \times \frac{dV_S}{dt}
\]

This behavior is similar to the voltage coefficient of discrete ceramic capacitors.\(^4,5\) The change in capacitance with applied voltage distorts the current in the capacitor. This distorted current drawn from the source produces a distorted signal at the op-amp input due to the voltage drop across \( R_S \):

\[
V_{IN} = V_S - I_S R_S
\]

It is possible to cancel this distortion by placing a resistance equal to the source impedance in the op amp’s feedback loop. This produces an identical distortion signal at the op amp’s inverting input. Because the distortion is now common to both inputs, it is removed by the op amp’s common-mode rejection. Unfortunately, the resistance in the feedback path introduces additional noise and also can cause stability issues if it is very large.\(^6\)

Ideally, to preserve low distortion when operating with high source impedances, the input common-mode capacitance needs to be stabilized to a constant value. One method to accomplish this is to fabricate the op amp with a dielectrically isolated (DI) process. As shown in Figure 4, DI processes use a layer of dielectric material, such as silicon dioxide (\( \text{SiO}_2 \)), to isolate devices from the substrate and other adjacent structures. These processes were originally introduced to improve the speed of on-chip transistors by reducing the capacitance at their collectors.\(^3\)

An additional benefit of dielectric isolation is that the JFET’s gate-to-substrate capacitance no longer varies with the input common-mode voltage. The value of the gate-to-substrate capacitance is determined by the size of the device and width of the isolation layer, which is completely unaffected by an applied electric field. Furthermore, the isolation layer prevents the diffusion of charge carriers across the p-n interface that would form a depletion
region. There is still an electric field across the barrier, but its effect on the mobile charge carriers in the silicon is not large enough to affect the total capacitance.

In Figure 5, the common-mode capacitance of two op amps was measured very precisely with a network analyzer. The TL072 op amp was fabricated with a standard junction-isolated process. Over the measurement range, the input common-mode capacitance varies from 4.87 pF at +10 V to 7.10 pF at –10 V, a total change of 2.23 pF. As expected, the input common-mode capacitance increases with negative common-mode voltages because the gate-to-substrate voltage is decreasing.

Alternatively, the OPA1642 was fabricated with a DI process. The input common-mode capacitance is greatly stabilized and shows a variation of only 30 fF over the entire measurement range.

The improved stability of the input common-mode capacitance is immediately apparent in distortion measurements. Figure 6 shows the measured THD+N of the OPA1642 configured in a gain of +1 for source impedances of 20 Ω and 10 kΩ. Unlike the TL072, the distortion of the OPA1642 is unaffected by an increase in source impedance.

The need for JFET-input op amps is still prevalent today because they continue to offer a unique combination of low noise, low bias current, and excellent AC/DC performance. The introduction of DI processes in their fabrication and the resulting stabilization of the input capacitance allow modern JFET-input op amps to achieve extremely low distortion regardless of source impedance.

References

Related Web sites
www.ti.com/4q14-opa824
www.ti.com/4q14-opa1642
www.ti.com/4q14-opa141
www.ti.com/4q14-opa140
Subscribe to the AAJ: www.ti.com/subscribe-aaj
**TI Worldwide Technical Support**

### Internet

**TI Semiconductor Product Information Center**

**Home Page**

support.ti.com

**TI E2E™ Community Home Page**

e2e.ti.com

### Product Information Centers

#### Americas

<table>
<thead>
<tr>
<th>Country</th>
<th>Phone</th>
</tr>
</thead>
<tbody>
<tr>
<td>Brazil</td>
<td>0800-891-2616</td>
</tr>
<tr>
<td>Mexico</td>
<td>0800-670-7544</td>
</tr>
</tbody>
</table>

#### Europe, Middle East, and Africa

**Phone**

- **European Free Call**: 00800-ASK-TEXAS (00800 275 83927)
- **International**: +49 (0) 8161 80 2121
- **Russian Support**: +7 (4) 95 98 10 701

**Note:** The European Free Call (Toll Free) number is not active in all countries. If you have technical difficulty calling the free call number, please use the international number above.

**Fax**

+49 (0) 8161 80 2045

**Internet/Email**

support.ti.com/sc/pic/america.htm

**Direct Email**

asktexas@ti.com

#### Asia

**Phone**

<table>
<thead>
<tr>
<th>Country</th>
<th>Toll-Free Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Australia</td>
<td>1-800-999-084</td>
</tr>
<tr>
<td>China</td>
<td>800-820-8682</td>
</tr>
<tr>
<td>Hong Kong</td>
<td>800-96-5941</td>
</tr>
<tr>
<td>India</td>
<td>000-800-100-8888</td>
</tr>
<tr>
<td>Indonesia</td>
<td>001-803-8861-1006</td>
</tr>
<tr>
<td>Korea</td>
<td>080-551-2804</td>
</tr>
<tr>
<td>Malaysia</td>
<td>1-800-80-3973</td>
</tr>
<tr>
<td>New Zealand</td>
<td>0800-446-934</td>
</tr>
<tr>
<td>Philippines</td>
<td>1-800-765-7404</td>
</tr>
<tr>
<td>Singapore</td>
<td>800-886-1028</td>
</tr>
<tr>
<td>Taiwan</td>
<td>0800-006800</td>
</tr>
<tr>
<td>Thailand</td>
<td>011-800-886-0010</td>
</tr>
</tbody>
</table>

**International**

+86-21-23073444

**Fax**

+86-21-23073686

**Email**

tiasia@ti.com or ti-china@ti.com

**Internet**

support.ti.com/sc/pic/asia.htm

**Important Notice:** The products and services of Texas Instruments Incorporated and its subsidiaries described herein are sold subject to TI's standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer's applications or product designs, software performance, or infringement of patents. The publication of information regarding any other company’s products or services does not constitute TI’s approval, warranty or endorsement thereof.

© 2014 Texas Instruments Incorporated. All rights reserved.

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio
Amplifiers
Data Converters
DLP® Products
DSP
Clocks and Timers
Interface
Logic
Power Mgmt
Microcontrollers
RFID
OMAP Applications
Wireless Connectivity

Applications
Automotive and Transportation
Communications and Telecom
Computers and Peripherals
Consumer Electronics
Energy and Lighting
Industrial
Medical
Security
Space, Avionics and Defense
Video and Imaging

www.ti.com/audio
www.ti.com/amplifier.ti.com
www.dataconverter.ti.com
www.dlp.com
www.dsp.ti.com
www.ti.com/wirelessconnectivity
www.ti.com/omap
www.ti.com/audio
www.ti.com/automotive
www.ti.com/communications
www.ti.com/computers
www.ti.com/consumer-apps
www.ti.com/energy
www.ti.com/industrial
www.ti.com/medical
www.ti.com/security
www.ti.com/space-avionics-defense
www.ti.com/video

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2014, Texas Instruments Incorporated