

Using interleaving with SAR ADCs for lower power, smaller size and lower cost

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Introduction

Recent advancements in successive-approximation-register analog-to-digital converters (SAR ADCs) have enabled much lower power consumption. These ADCs also maintain the resolution and sampling-rate performance that they are known for in the market. In general, SAR ADCs are faster than delta-sigma ADCs but often slower than pipeline ADCs. However, the resolution ranges of SAR ADCs are wider than the pipeline ADCs. In the current market, the resolution spectrum is fairly well covered, but there is a gap between the sampling speed of SAR ADCs and pipeline ADCs. The interleaving of SAR ADCs is a method of bridging this gap.

Interleaving is a technique that enables a system to maintain the resolution of the SAR ADC while increasing the effective sample rate, helping bridge the speed gap. In an equivalent system, interleaved SAR ADCs can help reduce the overall power consumption, cost and size of the end system compared to pipeline ADCs. This article highlights some key considerations when designing an interleaved SAR ADC system and provides test results from an example system.

Interleaving technique

Interleaving is a technique where multiple data converters sample a common signal and the sampling period for each converter is phase-shifted to effectively increase the system sampling rate. This allows the overall measurement system to maintain the resolution of the individual ADCs while increasing the overall throughput in order to more quickly measure input signals.

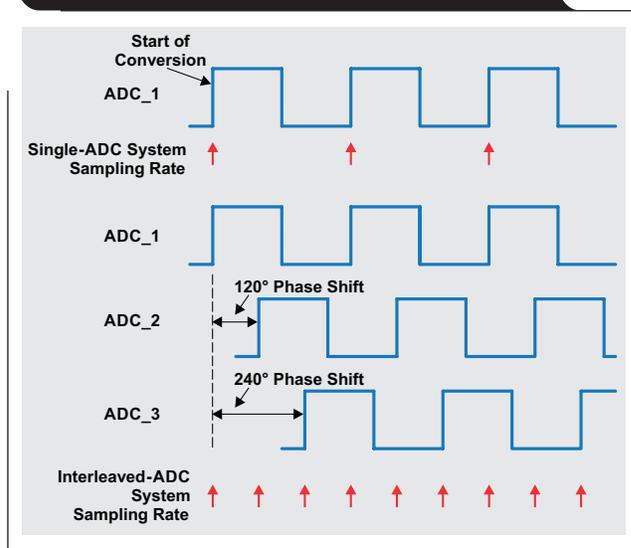
Keep in mind that the ADCs must be synchronized for this system architecture to work. The same clock can be used to generate the conversion signal for the ADCs, shifting only the phase of the clock using the relationship shown in Equation 1:

$$\text{Phase}_{\text{ADC}_k} = 360^\circ \times \frac{(k-1)}{n} \quad (1)$$

where $k = 1, 2, 3, \dots, n$ and $n =$ the number of ADCs used in the system.

Figure 1 illustrates the concept of the phase offset and increased sampling rate for an interleaved system with three ADCs.

Figure 1. Sampling rate of an interleaved system with three ADCs



System-level design considerations

In theory, an infinite number of ADCs can be interleaved to achieve an infinite sampling rate; however, there are some realistic limitations to consider:

- The ADC has a minimum acquisition and conversion time in order to function as expected. The acquisition time should not overlap for interleaved ADCs if the ADCs are sampling the same input signal. The acquisition and conversion time impose a limitation on the maximum sampling rate for a single ADC; the minimum acquisition time itself imposes a limitation on the maximum sampling rate for an interleaved system, and therefore the maximum number of interleaved ADCs.
- The bandwidth of the individual ADCs needs to be at least twice the frequency of the input signal to adhere to the Nyquist sampling theory. As the input signal frequency approaches the bandwidth of the individual ADCs, the system will no longer be able to properly measure it.
- Other factors like area and power consumption also scale with the number of ADCs used and thereby impose a practical limitation on the total number of ADCs in the system.

In addition to the practical limitations just described, there are also measurement errors introduced in interleaved data-acquisition systems that are not present in single-ADC systems. These errors fall into two categories: system-level and ADC-specific. At a system level, SAR ADCs require a voltage reference with which to compare the input voltage and a front-end driver amplifier to buffer the input signal. The mismatch between references and buffer amplifiers can introduce errors due to manufacturing process deviations. To eliminate these errors, the solution shown in Figure 2 has a single voltage reference and front-end driver amplifier with multiple ADCs.

With the circuit in Figure 2, a single-input drive buffer eliminates the offset variations of the input signal. Using a single driver amplifier ensures that the ADCs receive the same offset instead of different offsets due to the multiple drive amplifiers. A single amplifier can be used if the input signal has time to stabilize before the ADC starts its conversion process so that it converts a fully settled signal. This stabilization is possible if the amplifier has a wide-enough bandwidth, or if the internal sampling capacitor of the ADCs is small enough to allow enough time for the signal to settle.

A single voltage reference connected to all three ADCs eliminates variations in the gain of the input signal. A single voltage reference must also provide the necessary current and bandwidth required to power the reference of multiple ADCs. In some low-power ADCs, the supply also acts as the reference voltage for the conversion. In such circuits, it is similarly important to ensure that the voltage reference can provide enough current to power the ADCs.

Figure 3 illustrates how a single drive buffer and voltage reference in an interleaved system with ideal ADCs can help minimize offset and gain errors due to device-to-device variations between multiple buffers and references. Ideal ADCs are used to highlight the effect that the variations in the buffers and references have on the measurement gain and offset. The next section will address the offset and gain error in the system with a single drive buffer and voltage reference by looking at the mismatches that exist between the multiple nonideal ADCs in the system.

Other system-level errors exist but will not be discussed in this article extensively. Proper layout techniques can mitigate (but not completely eliminate) errors caused by additional noise in the system such as clock jitter and clock skew.

ADC-specific design considerations

The ADC-specific errors are caused by device-to-device variations inherent in the device manufacturing process and consequently are not present in single-ADC systems. While it would be ideal if all ADCs were identical, in reality they exhibit differences in integral nonlinearity (INL), bandwidth, offset, and gain. INL is not easily correctable, and should be taken into account when designing the system. The bandwidth of the individual ADCs may

Figure 2. Simplified system design with ADC, drive buffer and voltage reference

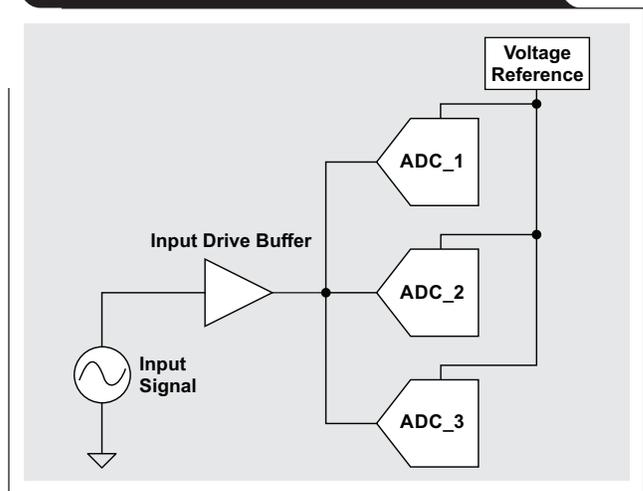
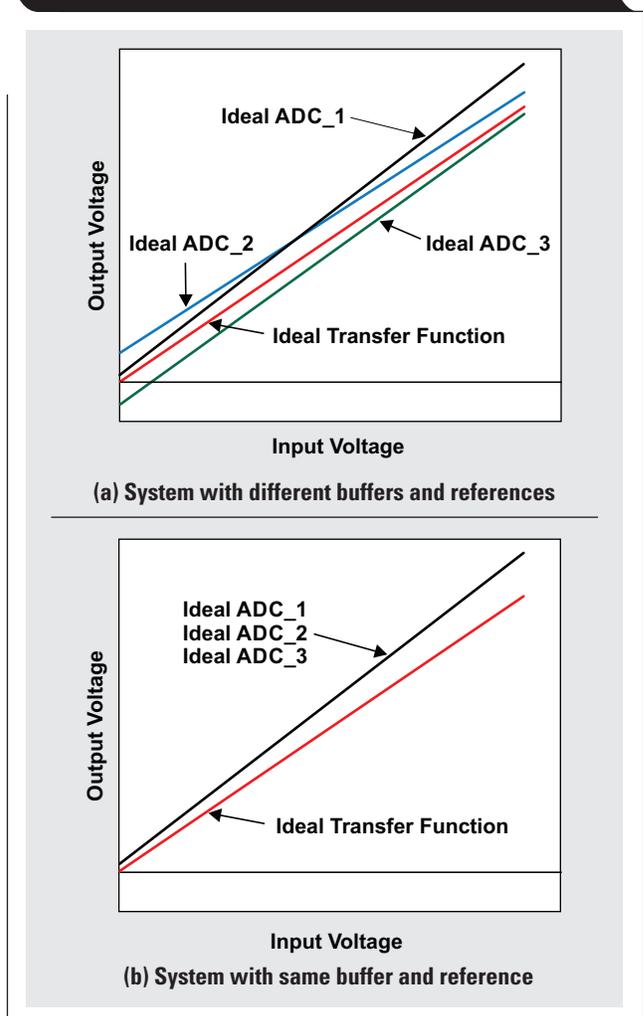


Figure 3. Minimizing offset and gain errors with a single drive buffer and voltage reference



become a consideration if it is less than the Nyquist rate of the input signal. However, modern ADCs have high-enough bandwidth specifications such that this is often not an issue. In contrast, offset and gain mismatches between ADCs can be calibrated out at the system level. This calibration process can be further optimized with the use of auto-calibration circuits integrated into some ADCs.

Offset and gain calibration

It is important to calibrate mismatches in offset and gain errors between multiple ADCs in an interleaved system in order to achieve the highest possible performance from the ADCs. These errors in the digital domain can be calibrated out with post-processing, but this causes additional complexity for the host processor. To eliminate this additional complexity, some SAR ADCs are now designed with extremely-low gain error and integrated offset-calibration circuitry. TI's ADS7056 is an example of a SAR ADC with an integrated offset-calibration feature and a typical gain error of only $\pm 0.01\%$ (or 3.2 LSBs at 14 bits). Therefore, this ADC does not generally require gain-error calibration.

If unaccounted for, the offset error will appear as a noise spur at the sampling frequency of the ADC, while the gain error will appear as a noise spur at the sampling frequency, plus or minus the input signal frequency. This will degrade the overall performance of the ADC, including the signal-to-noise-ratio (SNR). Figure 4 illustrates the effect of offset calibration on the noise spur generated at the sampling frequency, both before and after calibration.

Test results

An analog front-end circuit was used to measure performance of time-interleaved SAR ADCs (See Reference 1 and Related Web sites). This design interleaves three 14-bit ADS7056 SAR ADCs with a sampling rate of 2.5 MSPS each to achieve an effective system sampling rate of 7.5 MSPS.

Table 1 illustrates the interleaved system performance compared to that of an individual ADC. The overall performance metrics of the ADC—including resolution, SNR and total harmonic distortion (THD)—remain relatively the same, but the sampling rate increases to three times the sampling rate of an individual ADC.

Table 1. SAR ADC performance in a single ADC versus an interleaved ADC system

	1x ADS7056	3x ADS7056
Resolution	14-bit	14-bit
Sampling rate	2.5 MSPS	7.5 MSPS
SNR (dB)	74.9	73
THD (dB)	-85	-83.8

Figure 4. Reduction of noise spur at the sampling frequency after offset calibration

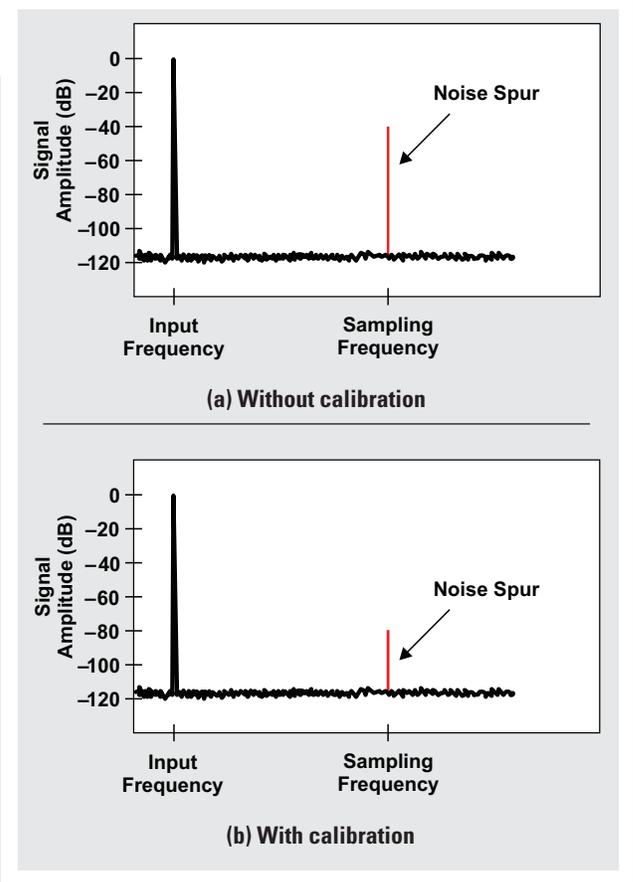


Table 2 compares the ADC performance of three interleaved SAR ADCs with a pipeline ADC. The performance specifications of resolution, sampling rate and SNR are comparable, while the power, package size and price are greatly reduced.

Table 2. SAR ADC specifications compared to a pipeline ADC

	3x ADS7056	THS1408
Resolution	14-bit	14-bit
Sampling rate	7.5 MSPS	8 MSPS
SNR (dB)	73	72
Power consumption (mW)	17.5	270
Package area (mm ²)	6.75	81
Price (1 ku)	\$6.00	\$20.05

The package area in Table 2 does not account for the overall system-level board area required to lay out the circuits. However, there is considerable margin between the size of the ADS7056 design compared to the other, so it is highly likely that this design will still be smaller.

Conclusion

There are some system-level considerations to be aware of when designing an interleaved ADC system. However, this article shows that interleaved SAR ADCs can help bridge the sampling-rate gap between SAR and pipeline ADCs. In addition, SAR ADCs also enable a lower-power, smaller-size, and lower-cost solution.

References

1. Abhijeet Godbole and Lokesh Ghulyani, “Low-Cost, Low-Power, Small Size, 14-bit AFE: Interleaved ADCs Scalable up to 7.5 MSPS Sampling With 73-dB SNR,” TI Application Report (SBAA231), 2017.
2. N. Kurosawa, H.Kobayashi, K.Maruyama, H. Sugawara and K. Kobayashi, “Explicit Analysis of Channel Mismatch Effects in Time-Interleaved ADC Systems,” IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Vol. 48, Issue: 3, 2001.

Related Web sites

Reference design tool:

Analog front end with time-interleaved SAR ADCs

Product information:

ADS7056

THS1408

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