

Comparing internally-compensated advanced current mode (ACM) with D-CAP3™ control

By Rich Nowakowski, Product Marketing Manager, Converter and Controller Products

Ryan Manack, Applications Manager, Power Design Services

Introduction

Vendors of switching regulators are very active in the development of leading-edge control circuits to help engineers address specific design challenges. No control mode is optimal for every application, and the various control modes for non-isolated step-down DC/DC controllers and converters each have unique advantages.

Linear control modes such as voltage mode and peak-current mode have been used for decades, and many designers are familiar with their implementation. However, over the past few years, nonlinear control modes such as constant on-time and its derivatives have become more popular due to their simplicity and better load-transient performance.

This article provides a comparison of the load-transient performance and jitter of DC/DC converters operating in two distinct modes. One is TI's D-CAP3™ control mode (a derivative of constant on-time), and the other a new internally-compensated, emulated-peak-current control mode called advanced current mode (ACM). The D-CAP3 and ACM control modes were both developed for enterprise rack-server and hardware-accelerator applications that require fast response times to load transients, but ACM provides a fixed synchronizable frequency that is suitable for medical ultrasound scanners and active-antenna communication systems. Neither of the control modes require loop compensation, making the design simpler than devices employing externally compensated voltage or current mode.

Selecting and bounding the application

Two different power supplies were designed and built to demonstrate the performance of each control mode under similar operating conditions. For both designs, the input voltage is 12 V, the output voltage is 1 V and the output current for each device is capable of 40 A. These requirements are typical for powering a high-performance processor such as a high-current field-programmable gate array (FPGA) or application-specific integrated circuit (ASIC) processor.

To bound the filter design and performance expectations, the allowable ripple voltage is $\pm 3\%$, or ± 30 mV (60 mV_{PP}) of the output voltage, and the allowable voltage overshoots and undershoots during a load transient are bound to $\pm 5\%$, or ± 50 mV (100 mV_{PP}). The comparison features two TI DC/DC converters: a 40-A D-CAP3 synchronous-buck converter^[1] switching at 650 kHz (TPS548D22); and an internally-compensated, ACM

synchronous-buck converter^[2] switching at 700 kHz (TPS543C20). Operating frequencies were selected as close as possible to one another within the converter's capability, allowing each design to use the same output filter. Although component selection is beyond the scope of this article, the inductor chosen for both designs was the Würth 744309025, which is a 47.5-A, 0.165-m Ω , 250-nH coil. Table 1 summarizes both device configurations.

Table 1. Converter frequency and output jitter

Part Number	Control	f _{sw}	Inductor	Output Capacitance
TPS543C20	ACM	700 kHz	250 nH	4 x 470 μ F + 2 x 100 μ F
TPS548D22	D-CAP3™	650 kHz	250 nH	4 x 470 μ F + 2 x 100 μ F

An overview of the D-CAP3™ control mode

The D-CAP3 control mode is a variation of a constant-on-time control mode where the loop comparator monitors its inputs from the feedback voltage, reference voltage and emulated current ramp voltage to simulate ripple to generate on-pulses.^[3] Whenever the ramp voltage and feedback voltage are lower than the reference voltage, the comparator output goes high to initiate an on-pulse. The control logic and driver block calculate the width of the on-pulse, based on the input-voltage, output-voltage and switching-frequency settings. During the on-pulse, the high-side power transistor turns on, the switch node is pulled-up to the input voltage and the inductor current increases to charge the output voltage.

The D-CAP3 control mode is different from earlier D-CAP™ generations because it uses an internal sample-and-hold circuit to eliminate the effects of the offset voltage of the integrated ripple-injection circuit. A benefit of the sample-and-hold circuit is improved output-voltage regulation accuracy. The D-CAP3 control mode has an ability to fine-tune the internal ramp amplitude by selecting one of four values through pin-strapping. The recommended value shown in the data sheet was used based on the device's duty cycle. The D-CAP3 control mode does not integrate an oscillator or clock, so the switching frequency is not synchronizable to an external clock signal.

An overview of the internally-compensated ACM

An internally-compensated ACM is an emulated peak-current-control topology. Like the D-CAP3 control mode, ACM supports stable static and fast load-transient operation without a complicated external compensation design.^[4] ACM does allow fixed-frequency modulation with

frequency synchronization to overcome electromagnetic interference (EMI) issues in noise-sensitive applications. This control architecture includes an internal ramp-generation network that emulates inductor current information, enabling the use of output capacitors with low equivalent series resistance (ESR), which the D-CAP3 control mode supports.

An internal ramp in the ACM creates a high signal-to-noise ratio for good noise immunity. ACM also has several ramp options requiring a single resistor to ground to optimize the internal loop for various inductor and output-capacitor combinations. The recommended resistor value specified in the data sheet was used for comparison purposes. WEBENCH® Power Designer will also recommend a resistor value to set the internal ramp amplitude.

A transient-response comparison

The D-CAP3 control mode is nonlinear, so the Bode plot is difficult to measure because the feedback loop is not fully disconnectable internally. Figure 1 shows the Bode plot for the ACM design. Measurements were taken with an output current of 15 A, which is the maximum current supported by the electronic load used for the comparison. The ACM design has a crossover frequency of 45 kHz and 58° of phase margin, which represents a stable power supply exhibiting traditional current-mode behavior. So when comparing with the D-CAP3 adaptive on-time control mode, it is better to inspect the load-transient waveforms.

A load-transient test was performed with a 20% to 80% load step (a 40-A full-load condition), or 8 A to 32 A, then 32 A to 8 A. The rising load step had a very fast slew rate of 240 A/μs, to better show the ACM pulse groupings, and a falling slew rate of 50 A/μs. When comparing the transient response waveforms shown in Figures 2 and 3, the ACM design has a slight advantage over the D-CAP3 solution, with faster response times and smaller voltage overshoots and undershoots. Table 2 shows the results.

Figure 1. Internally-compensated ACM Bode plot

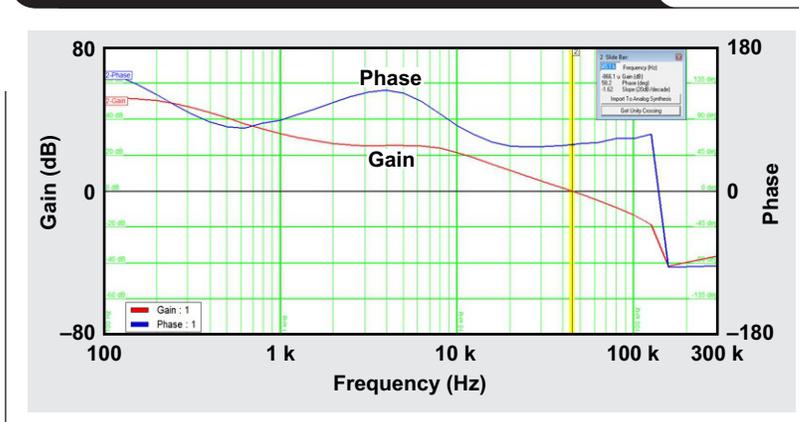


Figure 2. ACM transient response

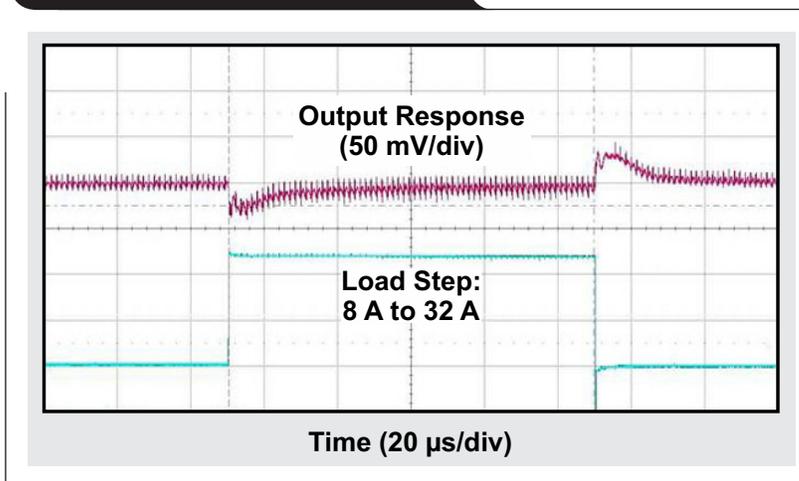


Figure 3. D-CAP3™ transient response

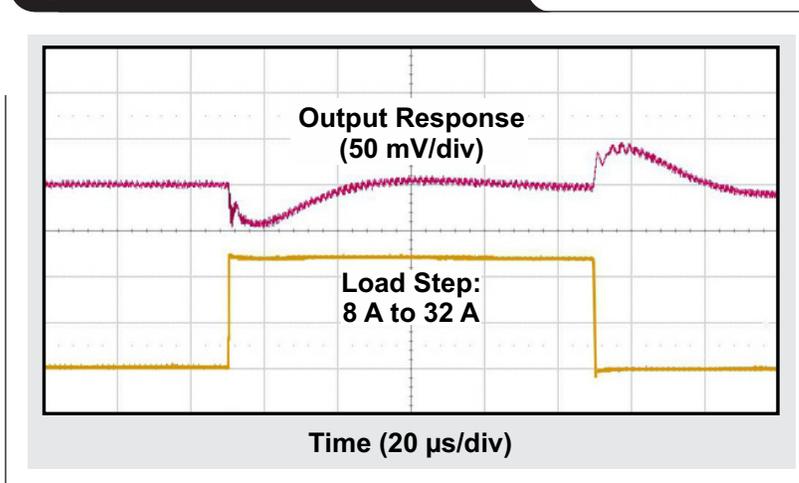


Table 2. Transient response summary at 240 A/μs with 8-A to 32-A load step

Control Mode	Undershoot	Undershoot Response	Overshoot	Overshoot Response
ACM	40 mV	20 μs	40 mV	20 μs
D-CAP3	50 mV	30 μs	45 mV	25 μs

Asynchronous pulse injection and body braking

ACM is a true fixed-frequency control mode, and a major limitation for any fixed-frequency converter is that during a transient load step, the converter must wait for the next clock cycle to respond to the load change. Depending on the loop bandwidth design and the timing of the load transient, this time delay could cause an additional output voltage drop. In our comparison, the ACM device implements asynchronous pulse-injection (API) circuitry to improve transient performance, which was employed for comparison with the D-CAP3 control mode. During the load step, the ACM converter senses both the speed and amplitude of the output voltage change. If the output voltage change is fast and large enough, the converter will generate an additional pulse-width modulation (PWM) pulse before the next available clock cycle to prohibit the output voltage from dropping further, which reduces the undershoot voltage. However, the switching frequency is no longer fixed during this transient event.

Figure 4 shows the switch-node waveform during an 8-A to 32-A load step with the additional asynchronous pulse injected by the DC/DC converter. As shown in Figure 5, the ACM pulse train actually has a similar appearance to the D-CAP3 control mode, where the PWM frequency changes to provide a faster response to the quickly changing load.

During load-step recovery, the ACM device implements a body-brake function, which turns off both the high- and low-side, metal-oxide-semiconductor field-effect transistors (MOSFETs) and allows power to dissipate through the low-side body diode, thus reducing the output voltage overshoot. This approach is effective in reducing voltage overshoot to help minimize the required output capacitance to meet the output voltage-tolerance requirement. However, it does have a minor impact on efficiency during a transient event due to additional power dissipated in the low-side MOSFET body diode. The API and body-braking features for the ACM DC/DC converter can be disabled by pin-strapping the mode pin accordingly, allowing the device to maintain fixed-frequency operation and frequency synchronization during a load-step transient.

Jitter

Jitter comes from many sources, but it typically comes from noise injected on the feedback or compensation pins of DC/DC converters. Jitter can also be a sign of instability. In D-CAP type converters, jitter is a well-known side effect of frequency modulation during a transient event, which greatly improves the load-transient response by quickly increasing the switching frequency. In applications that do not have noise-sensitive analog circuitry, frequency jitter is easily tolerated.

Figure 6 shows the frequency jitter for the D-CAP3 converter under a 15-A load condition. Note the frequency modulation on the right-hand pulse waveform.

Figure 4. ACM switch-node waveform during an 8-A to 32-A load step

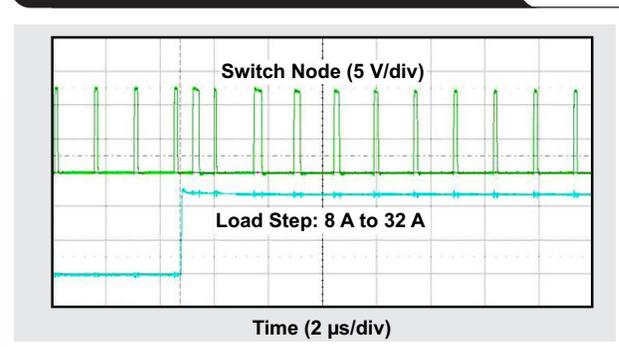


Figure 5. D-CAP3 switch-node waveform during an 8-A to 32-A load step

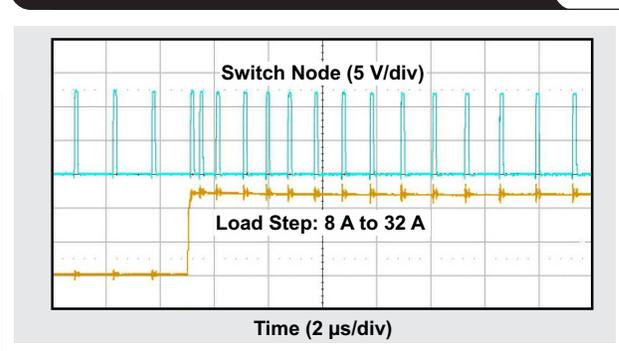
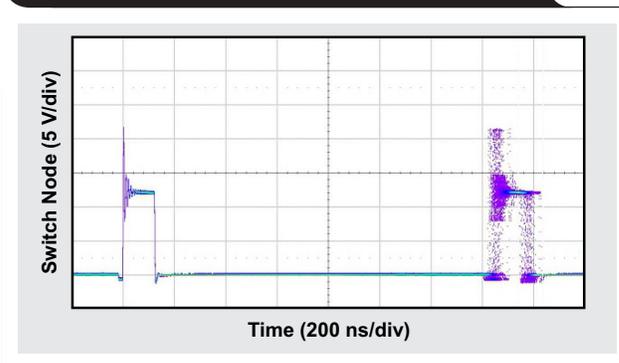


Figure 6. D-CAP3 frequency jitter at 15 A



ACM uses a fixed-frequency scheme that improves the frequency jitter performance over the D-CAP3 control mode, as shown in Figure 7. For applications that need more predictable switching-frequency behavior, ACM is the better choice.

Conclusion

There is no perfect control mode for every situation. When designing a wireless access point or a remote radio unit using data converters and other noise-sensitive circuitry, a fixed, predictable switching frequency that is synchronizable to an external clock may be the preferred design. On the other hand, many designers are looking for easy-to-use DC/DC converters that do not require tedious compensation calculations. They may also wish to reduce the required output capacitance to meet the processor's demanding load-transient and voltage-tolerance requirements. Table 3 summarizes the comparison between both control modes.

Table 3. Control-mode comparison summary

Control Mode	Transient Response	Compensation Required	Ramp Adjustment	Frequency Synchronization	API/Body Braking	Jitter
ACM	Fast (with API)	No	Yes	Yes	Yes	Lower
D-CAP3	Fast	No	Yes	No	N/A	Higher

Both control modes complement one another and each has its own merits. ACM provides a fast transient response and has the ability to tune performance with an adjustable ramp, API and body braking. When fixed-frequency operation and reduced external components are required, ACM may offer a better alternative to the D-CAP3 control mode.

References

1. “TPS543C20 4- V_{IN} to 16- V_{IN} , 40-A Stackable, Synchronous Step-Down SWIFT™ Converter with Adaptive Internal Compensation,” Texas Instruments data sheet (SLUSCD4), September 2017.
2. “TPS548D22 1.5-V to 16-V V_{IN} , 4.5-V to 22-V V_{DD} , 40-A SWIFT™ Synchronous Step-Down Converter with Full Differential Sense,” Texas Instruments data sheet (SLUSC70D), July 2017.
3. Song Guo, “Accuracy-Enhanced Ramp Generation Design for D-CAP3 Modulation,” Texas Instruments Application Report (SLVA762A), April 2016.
4. Mingyue Zhao, Jiwei Fan, and Nguyen Huy, “Internally Compensated Advanced Current Mode (ACM),” Texas Instruments Report (SLYY118), August 2017.

Related Web sites

Design tool:

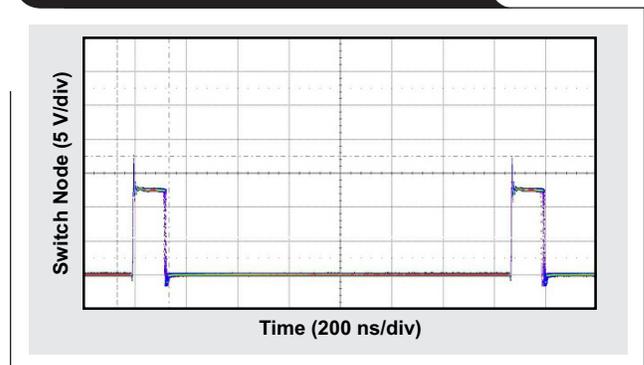
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Product information:

TPS548D22

TPS543C20

Figure 7. ACM on-time jitter at 15 A



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