

Designing for high common-mode rejection in balanced audio inputs

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Introduction

Balanced audio-signal transmission is useful in many environments, such as concert venues, sports arenas and professional recording studios. In a balanced transmission system, the audio signal transmits over two signal lines differentially (180 degrees out of phase). Electrical interference tends to be introduced into both signal lines with equal magnitude and equal phase. Therefore, subtracting the signal on one conductor from the other will recover the audio signal and remove unwanted interference common to both signal lines. The job of a line-receiver circuit is to perform this subtraction while adding the least possible amount of noise and distortion to the audio signal.

The figure of merit that quantifies the ability of a line-receiver circuit to reject noise that is common to both signal lines is the common-mode rejection ratio (CMRR) and is typically expressed in decibels. See Equation 1.

$$\text{CMRR(dB)} = 20 \times \log \left(\frac{A_{\text{CM}}}{A_{\text{DM}}} \right) \quad (1)$$

where A_{CM} is the line-receiver's gain for common-mode signals and A_{DM} is the gain for differential signals.

Figure 1 represents a typical balanced audio-transmission system with a line-driver circuit that transmits two complementary audio signals (V_S and $-V_S$) over a shielded twisted-pair cable to a line receiver. R_{S1} and R_{S2} represent the output impedances of the line driver. Figure 1 also shows a line receiver where $R_{\text{IN}1}$ and $R_{\text{IN}2}$ represent the input impedances.

Two sources of external interference are present in Figure 1. $V_{\text{N}1}$ represents interference that is capacitively

coupled into the signal lines through inadequate shielding of the cable, or unshielded cable runs inside of equipment enclosures. $V_{\text{N}2}$ illustrates common-mode interference that may arise from ground-potential differences between connected pieces of equipment, or circulating ground currents that magnetically couple interference into the signal lines.

For an ideal line-receiver circuit with a differential gain of 1 and a common-mode gain of 0 (infinite CMRR), Equation 2 shows the transfer function of the circuit.

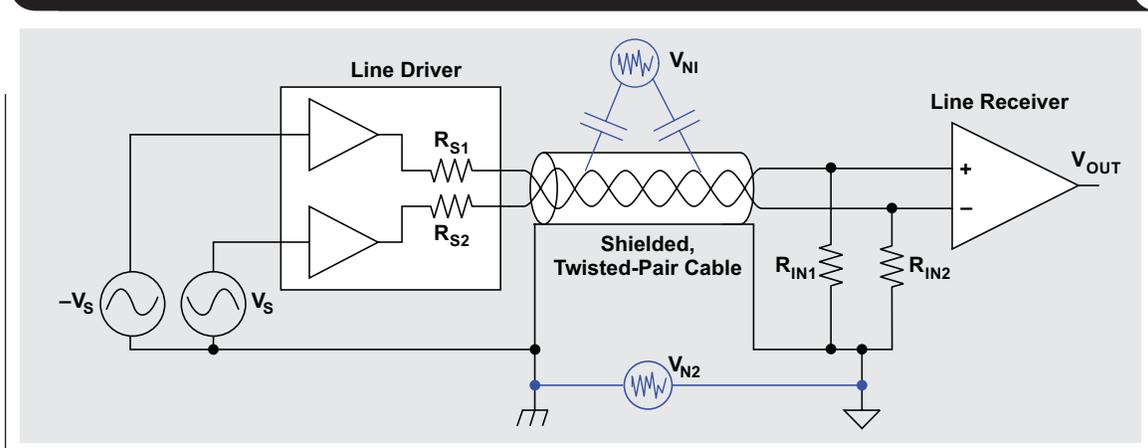
$$\begin{aligned} V_{\text{OUT}} &= (V_S + V_{\text{N}1} + V_{\text{N}2}) - (-V_S + V_{\text{N}1} + V_{\text{N}2}) \\ &= 2 \times V_S \end{aligned} \quad (2)$$

Achieving this idealized transfer function requires more than using an ideal component for the line receiver and is a difficult design challenge in the real world. To ensure that the external interference couples into both signal transmission lines with equal magnitude and phase requires meeting several conditions:

- Matching the output impedances of the line-driver circuit (R_{S1} and R_{S2}).
- Matching the input impedances of the line-receiver circuit ($R_{\text{IN}1}$ and $R_{\text{IN}2}$).
- Matching all parasitic impedances from the cable, printed circuit board (PCB) and connectors.

While achievement of the conditions in this list may seem impossible, careful design of the line-receiver circuit can make great strides toward improving the noise immunity of an audio system.

Figure 1. Typical balanced audio-transmission system with common-mode noise sources



A typical line-receiver circuit

Professional audio equipment with XLR-connector or screw-terminal inputs might use the type of line-receiver circuit shown in Figure 2. It consists of an audio operational amplifier (op amp) configured as a four-resistor difference amplifier with input AC-coupling capacitors. While additional components for filtering radio frequency interference (RFI)/electromagnetic interference (EMI) or electrostatic discharge (ESD) protection may also be necessary, they are not shown in the figure.

The differential gain of the circuit in Figure 2 is one, and theoretically the common-mode gain of the circuit is zero if constructed with perfectly matched resistors and capacitors and an ideal op amp. But designers often choose this topology for its simplicity, not its high performance in the application. For example, the input impedance on each signal line (pins 2 and 3 of the XLR input) is not matched in a difference amplifier, which violates the second condition in the earlier bullet list.^[1]

Figure 3 shows the simulated CMRR performance versus frequency of the circuit and consists of three regions.

Region 1

CMRR degradation in region 1 is caused by a mismatch in the values of the input AC-coupling capacitors. This mismatch causes the individual high-pass corner frequencies at each of the inputs to the line-receiver circuit to be different. This mismatch will also convert some portion of a common-mode signal to a differential signal. Because the impedance of the input capacitors decreases as the frequency increases, the overall impact to the circuit performance is limited at high frequencies. For debugging purposes, a CMRR that improves as frequency increases (with a slope of 20 dB per decade) is an indicator that the AC-coupling capacitors are limiting the overall circuit performance.

The 10- μ F AC-coupling capacitors in the circuit were mismatched by 10% to produce the CMRR plot in Figure 3. This is not an unreasonable amount when considering the large tolerances of electrolytic or high-k ceramic capacitors (such as the X7R type) that might be used in AC-coupling applications. Improving CMRR performance in region 1 requires either improving the matching of the AC capacitors or lowering the high-pass corner frequency of the circuit. Both of these approaches have engineering trade-offs. For example, capacitors with tight tolerances may be prohibitively expensive or simply unavailable.

Lowering the high-pass corner frequency requires larger-value capacitors or larger resistances in the difference-amplifier circuit. Increasing the resistor values used in the difference amplifier will introduce additional noise into the signal path and degrade the system's signal-to-noise ratio

Figure 2. A common line-receiver circuit using an op amp with discrete resistors and capacitors

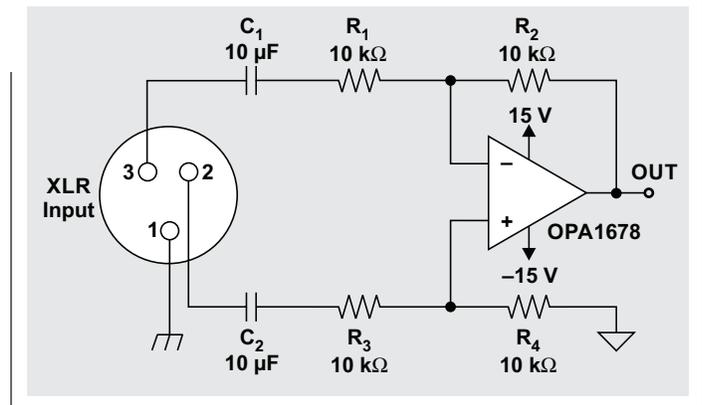
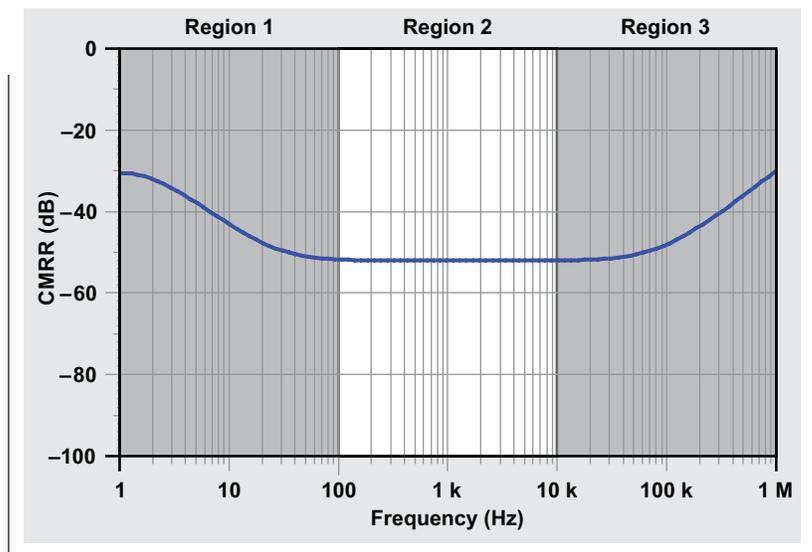


Figure 3. CMRR performance of the line-receiver circuit shown in Figure 2



(SNR). Therefore, using larger capacitors may be the best option in this circuit.

Region 2

CMRR degradation in region 2 is caused by a mismatch of the resistances in the difference-amplifier circuit. In region 2, the CMRR remains constant over frequency, indicating that the performance-limiting factor is an imbalance from resistances rather than impedances. The tolerance of R_1 , R_2 , R_3 and R_4 ; source-impedance mismatches; and parasitic resistances in the PCB routing can all contribute to CMRR degradation in region 2. Mismatched source impedances (R_{S1} and R_{S2} in Figure 1) will produce errors in the matching of R_1 and R_3 .

Another common culprit is resistance in series with R_4 . In single-supply systems, R_4 may connect to a reference voltage rather than to ground. The output impedance of that reference voltage is in series with R_4 and adds

additional error to the matching of the four resistors in the difference amplifier. A very common mistake is using an unbuffered voltage divider to produce this reference voltage.

Equation 3 can be used to calculate the worst-case CMRR for a difference amplifier circuit.^[2]

$$CMRR \text{ (dB)} = 20 \times \log \left(\frac{1 + R_2 / R_1}{4T / 100} \right) \quad (3)$$

where T is the resistor tolerance in percent (%).

Table 1 below shows the worst-case CMRR for several values of resistor tolerance. These values are pessimistic because they assume each resistor in the difference amplifier is unbalanced in the worst direction to the full extent of its tolerance.

The graph in Figure 3 was generated with a 0.5% error among the difference amplifier resistors. This assumption is realistic if the circuit is constructed with 1% resistors from the same manufacturing lot. Improving performance in region 2 may require resistors with tighter tolerance specifications; however, the price for these components may be extremely high. At the time of this writing, an array containing two matched 10-kΩ resistors with a tolerance of 0.01% was \$17.20 (U.S.) each in 500-unit quantities at a major online distributor, and the difference-amplifier circuit would require two such arrays.

Region 3

The AC performance of the op amp and parasitic capacitances from the PCB layout usually limit the overall CMRR performance at high frequencies. Even with ideal matched impedances in the difference-amplifier circuit, the op-amp’s

open-loop gain, open-loop output impedance and intrinsic CMRR will tend to cause the circuit CMRR to degrade at high frequencies. The OPA1678 TINA-TI™ macromodel correctly simulates all high-frequency performance parameters that could affect CMRR performance and was used to generate the curve in Figure 3. Additionally, adding a 1-pF capacitor to the simulation schematic from the op-amp’s non-inverting input to ground shows the effects of mismatched PCB parasitics.

To maximize the CMRR in region 3, the PCB layout should have the signal traces routed as a differential pair. The signal traces should also have equal lengths and trace widths, and be placed on the PCB as close to each other as possible. Ground pours used above, beside and below the signal traces will provide shielding as long as there are matching parasitic capacitances from each signal trace to the ground pour. It may also be necessary to replace the op amp to improve high-frequency CMRR performance in region 3. CMRR limitations imposed by the op amp at high frequencies can be analyzed with a SPICE-based simulator.

An improved audio line-receiver circuit

The architecture of the line-receiver circuit shown in Figure 4 offers numerous performance benefits over the circuit shown in Figure 2. Rather than being constructed from an op amp and discrete resistors, the circuit in Figure 4 uses the INA1650 integrated line receiver to implement the same functionality (showing two audio input channels).

Table 1. Worst-case CMRR for several resistor tolerances

Resistor tolerance (%)	Worst-case CMRR (dB)
5.000	20
1.000	34
0.100	54
0.010	74
0.001	94

Figure 4. Two-channel line-receiver circuit using the INA1650 integrated line receiver

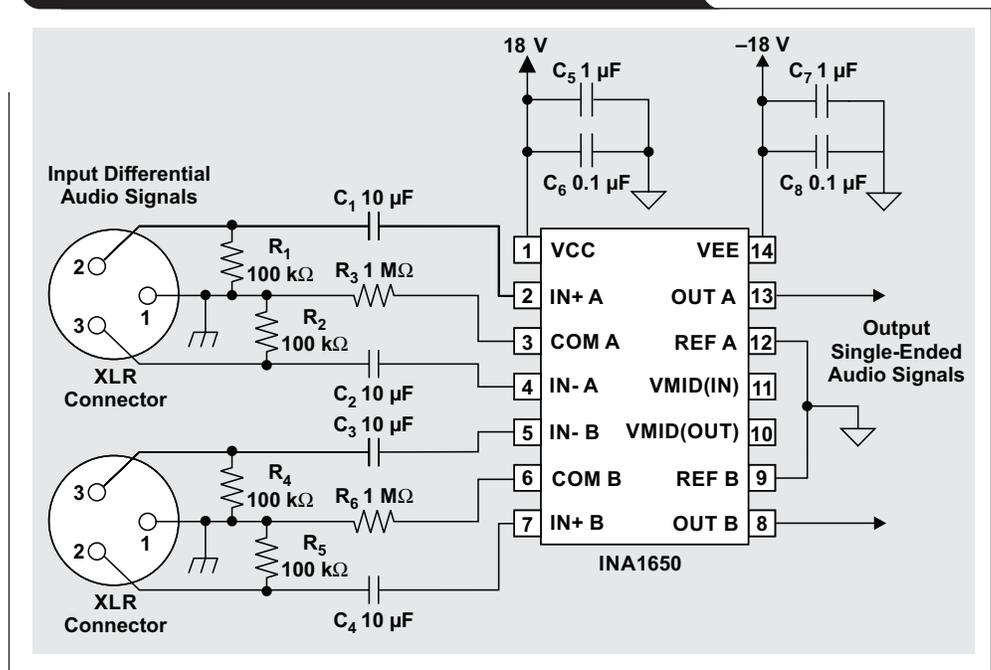


Figure 5 shows the internal topology of the INA1650 (and the automotive-qualified version, the INA1650-Q1). Adding input buffer amplifiers (A1 and A2) in front of the standard four-resistor difference amplifier isolates the resistors in the difference amplifier from the external circuitry. They also enable matched input impedances on each signal line. A1 and A2 are amplifiers with field-effect transistor (FET) inputs that have input-bias currents in the picoamperes, which also allows for very-high input impedance.

The INA1650 includes two 500-k Ω resistors between the inputs (IN- and IN+) and the COM pin (R_{BIAS1} and R_{BIAS2}). These resistors are typically matched within 0.01% and provide a pathway for the input bias current of A1 and A2 to flow, while also maintaining excellent CMRR at the system level.

A major advantage of integrated line-receiver products over discrete circuits is the incredible matching made possible by using on-chip thin-film resistors. The INA1650's internal 10-k Ω resistors ($R_{DA1,2,3,4}$) are matched within 0.0028%, enabling the device to have a guaranteed minimum CMRR of 85 dB (tested in production). TI designed the internal layout of the INA1650 to minimize parasitic capacitances that would degrade high-frequency CMRR.

Notice that in Figure 4, there is a 1-M Ω resistor connected between the COM pins of channel A and channel B (R_3 and R_6) to ground. To simplify discussion, these resistors will be referred to as R_{COM} . The addition of this resistor further improves the line-receiver CMRR, even with large mismatches in the AC-coupling capacitors or the line-driver source impedance.

Figure 6 shows the CMRR of the INA1650 (with a typical CMRR of -92 dB) for increasing source-impedance mismatches. When connecting the COM pin directly to ground (R_{COM} equal to 0 Ω), a 20- Ω source-impedance mismatch degrades the CMRR from -92 dB to -83.7 dB. However, if R_{COM} has a value of 1 M Ω , the CMRR only degrades to -89.6 dB.

The same 20- Ω source-impedance mismatch would degrade the CMRR of a typical line receiver to -60 dB (assuming it also had a 92-dB nominal CMRR and 10-k Ω internal resistors). R_{COM} does not need to be a high-precision resistor with a very tight tolerance; low-cost 5% or 1% resistors will not degrade CMRR performance.

Figure 5. Internal architecture of the INA1650 (showing a single channel)

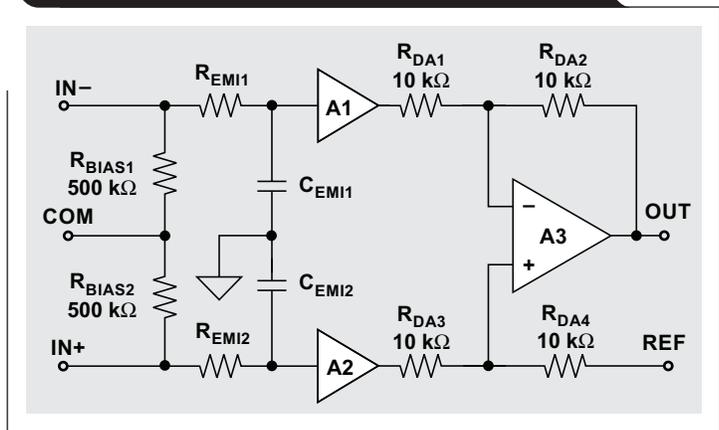


Figure 6. CMRR of the INA1650 and a traditional difference amplifier for increasing source-impedance mismatches

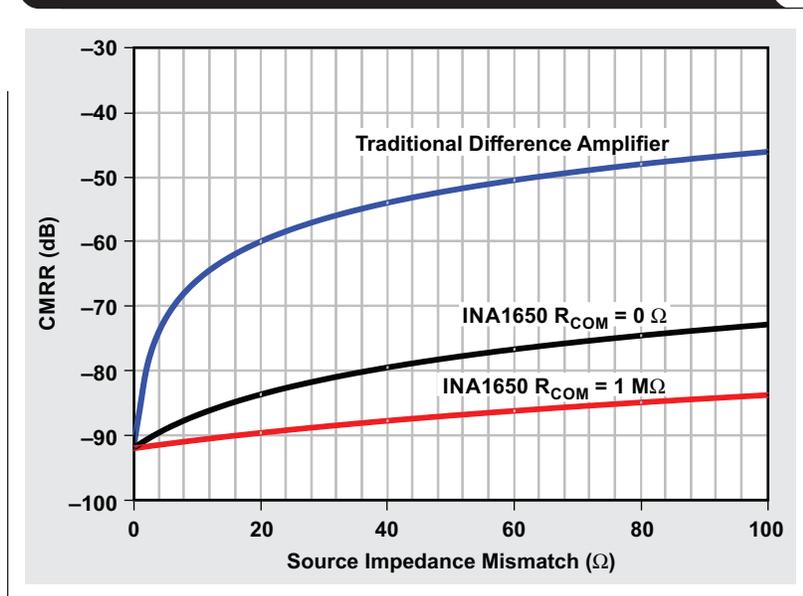


Figure 7. CMRR comparison of the INA1650 and the discrete circuit

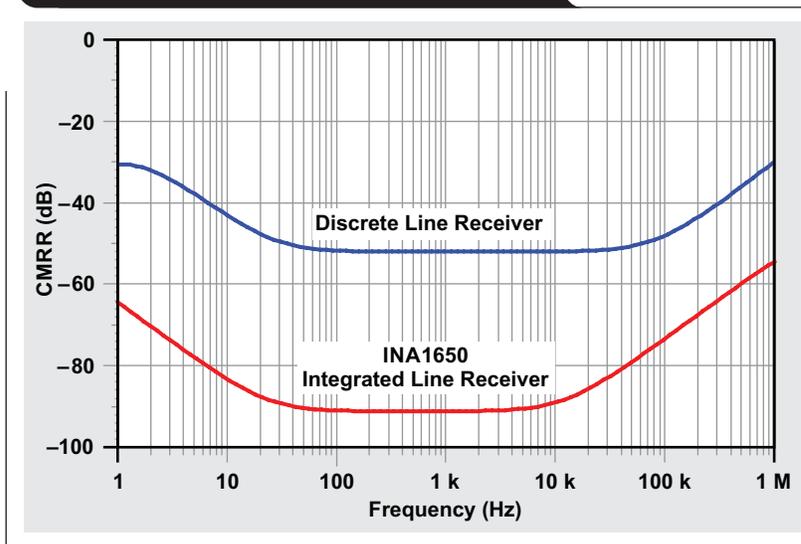


Figure 7 shows the performance of the INA1650 circuit in Figure 4 compared to the original simulation results of the discrete circuit in Figure 2.

The simulation of the INA1650 also used the same 10% mismatch in the input AC-coupling capacitors. At the critical range of frequencies between 50 Hz and 400 Hz, where mains interferences usually introduce audible hum into audio systems, the INA1650 shows a 40-dB improvement in CMRR over the discrete circuit.

Conclusion

Achieving high CMRR in line-receiver circuitry for balanced audio applications requires careful circuit design, component selection and PCB layout. By examining the CMRR of a circuit versus frequency, it is possible to deduce which part of the line-receiver circuit is limiting performance.

Unfortunately, the closely-matched passive components required to achieve very-high levels of CMRR are too expensive for mass-produced products. Some manufacturers have trimmed the CMRR of each individual circuit with a potentiometer, but this is time- and labor-intensive, which results in a more expensive product. By using the INA1650 integrated line receiver, system designers can achieve extremely high levels of CMRR with significantly lower cost and size for the total solution.

References

1. John Caldwell, "Overlooking the obvious: the input impedance of a difference amplifier," TI E2E™ Community, August 14, 2015.
2. Douglas Self, "Small-Signal Audio Design," Waltham, Massachusetts: Focal Press, 2010.

Related Web sites

Tools and software:

INA1678 simulation models

TINA-TI™ SPICE-based analog simulation program

Product information:

OPA1678

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