How to parallel two DC/DC converters with digital controllers

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Introduction
In high-power applications or N+1 redundant power systems, two or more power converters are connected in parallel to provide power to the load, thus increasing the amount of current available.

However, parallel operation is not as simple as just connecting the outputs together; it brings new challenges. A properly operating parallel system should meet these criteria:

- **Interleaving**: Interleaving means that the switching frequency of the second power converter should be phase-shifted relative to the first converter in order to evenly space the power pulses. Proper interleaving reduces the voltage ripple of the combined converters, resulting in potential output-capacitance reduction and cost savings. Different topologies require different degrees of shift. For two buck converters, the phase should shift by 180 degrees. For two full-bridge converters, because the frequency of output pulses is twice the switching frequency, a phase shift of 90 degrees is appropriate.

- **Current sharing**: Due to the component tolerance, the output voltages of the power converters will not be exactly the same. A slight difference in output voltage will cause a huge difference in output current; thus the converter with the higher voltage will provide most of the current to the load. This will cause two side effects. First, the converter with the high output current suffers high stress and thus reduced reliability. Second, overcurrent protection may be triggered and shut down the converter.

- **Simultaneous startup**: If a heavy load is already applied during startup and one converter starts up earlier than the other, it has to provide all of the load current. Overcurrent protection may be triggered and shut down the converter, causing startup to fail.

Not every controller has integrated these functions, especially digital controllers. On the other hand, digital controllers dominate systems where parallel operation is mandatory. Although most digital controllers have a synchronize pin and some digital controllers even have a current-sharing pin, they won’t do proper interleaving and current sharing if the pins are simply connected together. Because of component tolerance, they will most likely not start up simultaneously either.

It is important to define and implement a proper parallel-operation algorithm. This article uses two UCD3138-controlled, phase-shift full-bridge DC/DC converters to implement these functions. Figure 1 shows the hardware connections.

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![Figure 1. Parallel operation of two phase-shift full-bridge DC/DC converters](image-url)
Interleaving

Like most digital controllers, the UCD3138 has a SYNC pin that can synchronize pulse-width modulation (PWM) outputs to an external signal. One power converter, designated as the master, can generate a synchronize signal (DPWMOA in this example) that equals its switching frequency but is phase-shifted 90 degrees. Connecting this signal to the SYNC pin of the other power converter (designated as slave) and configuring the slave to synchronize to it will shift the slave’s switching frequency by 90 degrees.

However, there’s a problem: because of component tolerances, no two controllers have exactly the same internal clock frequency. Moreover, the clock frequency changes with temperature; even if the two clock frequencies are close at room temperature, they can be different when the temperature changes. If the master and slave clock frequencies are significantly different, forcing them to synchronize may cause PWM pulse stretching or missing pulses, resulting in power-stage damage.

Therefore, the first thing to do is to match the switching frequencies. To do that, the slave converter needs to know the master’s switching frequency. One option is to measure the frequency of the SYNC signal because it matches the master’s switching frequency. However, the SYNC signal is high frequency and the capture function of the UCD3138 has limited resolution. The frequency measurement may not be accurate enough.

For a more accurate measurement, let the master converter generate another PWM signal (PWM0 in this example) with a much lower frequency and send this signal to the timer-capture (TCAP) pin of the slave converter. The slave converter captures this signal and determines the switching frequency of the master, and then adjusts its switching frequency to match. Once this process is complete, it is safe to enable the synchronization function. The two converters will now be interleaved.

There is a general-purpose input/output (GPIO) signal from slave to master in this configuration used for simultaneous startup, which will be discussed later.

Here are some things to note about Figure 1:

- The master should keep sending SYNC and PWM0 signals even if it shuts down due to fault protection.
- During normal operation, the master continues sending out the PWM0 signal; the slave continues measuring this signal and adjusting its switching frequency to match the master. This way, the slave will track the master’s switching frequency as temperature and clock frequencies change.

Figures 2 and 3 show test results. Figure 2 is the fixed-leg PWM waveform after interleaving. Note that the master and slave channels are phase-shifted by 90 degrees. Figure 3 is the output voltage before the output inductor. Its frequency is twice the switching frequency and the master and slave signals are well interleaved. The inductor-current pulses are 180 degrees out of phase.
Current sharing

There are two popular current-sharing methods: active current sharing and passive-droop current sharing. Each has its own pros and cons. In active current sharing, a current-share bus connects the paralleled power converters. The signal on the share bus represents the average current of all modules; each power supply attempts to adjust its output current in order to match its output current with the average current.

In this article, passive-droop current sharing is used as the example. There is no current-share bus required, so droop current sharing is also called zero-wire current sharing. Compared to active current sharing, passive-droop current sharing is a simple but reliable current-sharing method. In this method, the power-supply circuitry measures its output current and adjusts its voltage either up or down. If the load current increases, the voltage decreases linearly.

Figure 4 shows the characteristics of output-voltage versus output-current for two power converters. The extra voltage drop or “droop” is proportional to the load current. If one of the paralleled power converters tries to provide more current, its output will droop slightly, resulting in a reduced current. The other converter will provide more current to the load; thus, the power supplies will share the output load between them.

With digital-controller firmware, the implementation is easy. The firmware monitors its output current through an analog-to-digital converter (ADC) and adjusts the voltage-loop reference accordingly. Equation 1 shows how the voltage-loop reference is calculated:

\[ \text{Voltage loop reference} = \left( k \times \frac{I_{\text{OUT}} - I_{\text{OUT,max}}}{2} \right) \]

where \( k \) is the slope of the curve in Figure 4.

Equation 2 calculates \( k \) as:

\[ k = \frac{\text{Maximum allowed voltage drop}}{I_{\text{OUT, max}}} \]

Simultaneous startup

A power-converter startup sequence usually goes like this:
1. Turn on \( V_{\text{IN}} \).
2. The bias starts up and provides \( V_{\text{CC}} \) to the controller.
3. The controller initializes.
4. The controller checks that \( V_{\text{IN}} \) is correct and that there are no other faults.
5. The converter turns on.

With the addition of interleaving function, the master and slave converters have different firmware. This causes the controllers to have different initialization times. Also, given the component tolerance of the two converters, even without the interleaving function, they won’t turn on simultaneously.

Thus, a “handshaking” mechanism is required. A simple way to achieve this is to use both the SYNC signal and the connection between a GPIO pin on both the master and slave converters. The master does not send a SYNC signal until it has finished the initialization and is ready to turn on. Once the slave receives the SYNC signal and is ready to turn on, it sends a “SLAVE READY” signal back to the master and turns on. The master will turn on immediately once it receives this SLAVE READY signal. This way, master and slave will turn on at the same time, as shown in Figure 5. Now the SYNC signal is not only used as a synchronization signal but also as a handshaking signal. The GPIO and SYNC connections are the same as shown in Figure 1.
If the extra GPIO pin is not available, a delay in the master code can be added right before it starts sending out the SYNC signal. The delay should be long enough to guarantee that when the slave receives the first SYNC signal, its initialization is complete and it is ready to turn on. This way, the master does not need to wait for SLAVE_READY; it can turn on immediately after it starts sending the SYNC signal. The slave will turn on immediately after it receives the first SYNC signal and both the master and slave will turn on at the same time. This method saves the extra GPIO pin, but at the cost of extra startup delay time.

**Conclusion**

High-power applications or N+1 redundant power systems require two or more power converters running in parallel. The power supplies in a properly paralleled operating system should start up simultaneously, be interleaved and share the load current.

This article presented an example of how to implement such functions in a digital controller that does not already have these capabilities built-in. Although two converters were used in the example, the same concepts can be extended to three or more converters running in parallel.

**Related Web sites**

Product information: UCD3138
TI Worldwide Technical Support

TI Support
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www.ti.com/support
China: http://www.ti.com.cn/guidedsupport/cn/docs/supporthome.tsp
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China: http://www.deyisupport.com/
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