Application Report
SNAA062A–December 2008–Revised April 2013

AN-1879 Fractional N Frequency Synthesis

ABSTRACT

The topics included in this application report are: Integer N and Basic PLL Concepts, Traditional Fractional N Concepts, and Delta Sigma Fractional N Concepts.

Contents

List of Figures

List of Tables

1 Introduction

The premise of fractional N frequency synthesis is to use a feedback (N) counter that can assume fractional values. In many applications, this allows a lower N counter value and a higher phase detector frequency. The lower N counter value leads to lower phase noise because the N counter value multiplies the noise of the PLL system. The higher phase detector frequency leads to spurs that are farther from the carrier and thus easier to filter as well as the option to widen the loop bandwidth for faster lock time.

Although all these benefits predicted by theory are true, they are based on the assumption that the fractional circuitry of the N counter is ideal. The actual performance improvements that are realized will not be as good as theory predicts because the circuitry involved in allowing the N counter to be fractional generates phase noise and spurs of its own. To really understand the true benefits of using a fractional N PLL, a greater understanding of the device, application, and architecture is required. In terms of fractional N PLLs, they will be grouped into two distinct categories: traditional and delta-sigma. Traditional fractional PLLs are those that use analog compensation to reduce the fractional spurs. Delta sigma PLLs are those that use digital delta-sigma techniques to reduce the fractional spurs. Both of these will be discussed in much greater depth later.

In order to understand fractional PLLs can be explored at all, one must first have a good understanding of integer N and basic PLL concepts. The next step of understanding is traditional fractional PLLs, because their spur levels and phase noise are easy to predict. The final step is to explore delta sigma PLLs, since the prediction of their spurs and phase noise has the most challenges and exceptions.

By understanding all of these concepts, then you will have a better understanding of when it makes the most sense to choose an integer PLL, traditional fractional PLL, or delta-sigma fractional PLL.

2 Integer N PLL Concepts

2.1 Basic PLL Concepts and Architecture

The phased locked loop (Figure 1) takes a fixed frequency, f_{OSC}, and divides it by a fixed value, R, to get the phase detector frequency, f_{PD}. This phase detector frequency is multiplied by N to get the final output frequency of f_{VCO}. The VCO frequency is tuned by changing the N counter value, and the channel spacing of this VCO is f_{CH}.

$$f_{VCO} = f_{OSC} \times N/R \quad (1)$$

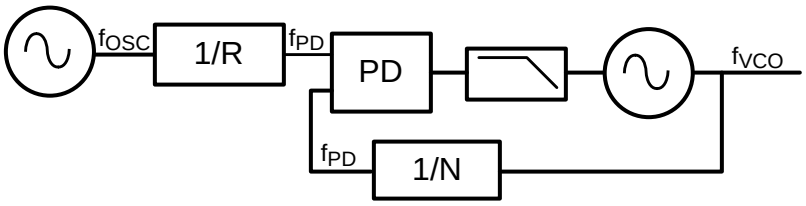

Figure 1. Basic PLL

For performance reasons, it is desirable to minimize the N counter value and maximize the phase detector frequency. Assuming the N counter value to be an integer, the largest that f_{PD} can be chosen is the channel spacing, f_{CH}. However, there could be additional restrictions that can restrict f_{PD} to a smaller divisor of f_{CH}. For instance, the phase detector frequency must also divide the oscillator frequency. This implies that :

Because of the channel spacing requirement, the phase detector frequency is:

$$f_{PD} = GCD (f_{OSC} , f_{CH}) \quad (2)$$

In Equation 2, GCD(x,y) denotes the greatest common divisor, which is the greatest number that divides x and y. The *AN-1865 Frequency Synthesis and Planning for PLL Architectures Application Report* (SNAA061) discusses application of this concept to non-integer arguments as well as other frequency planning concepts. For instance, if a channel spacing of 1 MHz was desired, then it would be desirable to choose the phase detector frequency to be 1 MHz, but this would only work if f_{OSC} was also a multiple of 1 MHz. If the oscillator frequency was 19.68 MHz, then the above formula would have to be used to calculate f_{PD} = GCD(19.68 MHz, 1 MHz) = 10 kHz.

2.2 Understanding Transfer Functions and Rolloff

In order understand spurs and phase noise of a PLL, it is necessary to understand how they are shaped by the loop filter. The first step in doing so is to understand the open loop transfer function, G(s), which can be found from the phase detector gain, K_{PD}, the VCO gain K_{VCO}, and loop filter transfer function, Z(s).

$$G(s) = \frac{K_{PD} \times K_{VCO}}{s} \times Z(s) \tag{3}$$

From the open loop transfer function, the closed loop transfer function, CL(s), is given by:

$$CL(s) = \frac{G(s)}{1 + G(s)/N} \tag{4}$$

The closed loop transfer function is important because it shapes the phase noise and spurs. At frequencies less than the loop bandwidth, the closed loop transfer function is relatively flat as a function of frequency and has a magnitude of 20·log(N):

$$\left\| CL(2 \times \pi \times f) \right\|_{f << \text{Loop Bandwidth}} \approx 20 \times \log(N) \tag{5}$$

It is this factor in that multiplies the phase noise and integer N PLL spurs, which is the motivation for doing a fractional N PLL that allows lower N values. Although this factor holds true for integer N PLL spurs and phase noise, it does not always come into play for fractional N PLL phase noise and spurs. For this reason, it is more convenient to subtract off this factor of 20·log(N) from magnitude of the closed loop transfer equation and define a new term called rolloff. Rolloff is a function of the offset frequency and shapes the phase noise and spurs:

$$\text{rolloff}(f) = 20 \times \log\left|CL(2\pi \times j \times f)\right| - 20 \times \log\left|N\right| \tag{6}$$

Figure 2 shows the rolloff of a PLL system that has a loop bandwidth (BW) of 237 kHz, which will be used in later examples.

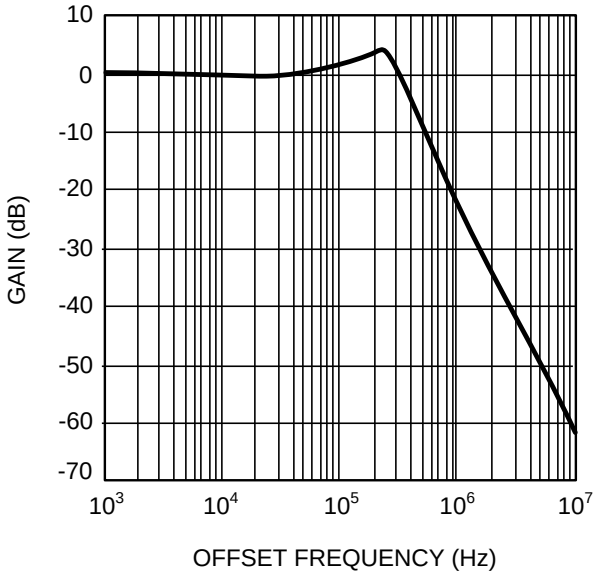

Figure 2. PLL Rolloff Example (BW = 237 kHz)

2.3 PLL Phase Noise

There are many contributors to the phase noise such as the reference oscillator, VCO, loop filter resistors, PLL dividers, PLL phase detector, and PLL charge pump. The oscillator, VCO, and loop filter resistor noise are application specific and not the focus of this application note. For the purposes of simplification, the noise of the PLL dividers, phase detector, and charge pump will all be lumped together and referred to as PLL noise. There are basically three main contributors to the PLL phase noise. For all PLLs, there is a flat noise and 1/f (flicker) noise produced by the charge pump. In addition to this, fractional parts will also have noise added due to their fractional compensation. After all these noise sources are added together, they are shaped by the rolloff of the PLL system. The PLL phase can be calculated as:

$$\text{PLLnoise}(f) = 10 \times \log\left|10^{\text{PLLnoise}_{\text{flat}}(f)/10} + 10^{\text{PLLnoise}_{1/f}(f)/10} + 10^{\text{PLLnoise}_{\text{fractional}}(f)/10}\right| + \text{rolloff}(f) \quad (7)$$

For the purposes of modeling integer PLL phase noise, it is usually sufficient to only consider the impact of the PLL flat noise, provided that the phase detector frequency is not too high (<1 MHz). However, if the phase detector frequency is higher, the 1/f noise may become more exposed and need to be considered.

2.3.1 PLL Flat Noise

The PLL flat noise increases as the N divider value increases and the part-specific performance can be captured in a convenient index called the 1 Hz normalized phase noise, PN1Hz. If the charge pump current is increased, then this index will improve, but there will be a point of diminishing returns.

$$\text{PLLnoise}_{\text{flat}}(f) = \text{PN1Hz} + 20 \times \log|N| + 10 \log\left|\frac{f_{PD}}{1\ \text{Hz}}\right| \quad (8)$$

If the output frequency is held constant, but the N counter value is decreased, then this also means that the phase detector frequency increases. For this situation, the phase noise is proportional to 10·log (N_{New} / N_{Old}). In other words, if the N counter value is decreased by a factor of 10 with the output frequency held constant, then the phase detector frequency will increase by a factor of 10 and the PLL flat noise will improve by 10 dB. However, this phase noise improvement may be masked at some offsets by the 1/f noise and the noise due to the fractional compensation.

2.3.2 PLL 1/f Noise

Active devices, including the PLL charge pump, produce a flicker (1/f) noise that decreases at 10 dB/decade with offset from the carrier. The 1/f noise of the PLL does not improve with higher phase detector frequencies as the flat noise does, so it becomes more important consideration when the phase detector frequency is high, as is the case with fractional PLLs. Simple experiments show that the PLL 1/f noise increases 20 dB/decade as a function of f_{VCO}, but is independent of f_{PD} and the N counter value, provided that f_{VCO} is held constant. This 1/f noise can be normalized to a 10 kHz offset and 1 GHz VCO frequency, PN10kHz. From this index, the unshaped 1/f noise of the PLL can be calculated anywhere.

$$PLLnoise_{1/f}(f) = PN10\ kHz + 20 \times \log\left|\frac{f_{VCO}}{1\ GHz}\right| - 10 \times \log\left|\frac{f}{10\ kHz}\right| \quad (9)$$

If the phase detector frequency is increased with a constant VCO frequency, the flat noise will improve, but the 1/f noise will not. Figure 3 shows phase noise data from an LMX2485 evaluation board driven with 100 MHz Wenzel crystal that has phase noise far below what is being measured. Raising the phase detector frequency improves the far out phase noise at offsets past 10 kHz, but for low offsets that are part of the 1/f noise, like 100 Hz, the impact is minimal.

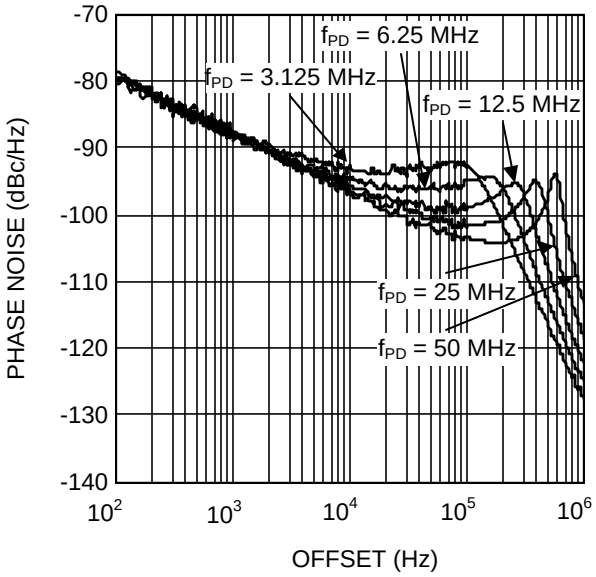

Figure 3. 1/f Noise and Phase Detector Frequency (K_{PD} = 16X)

[1] establishes that the charge pump is the only phase noise source that is theoretically divided by the charge pump gain and therefore suggests the 1/f noise in Figure 3 is really due to the charge pump and not some other source.

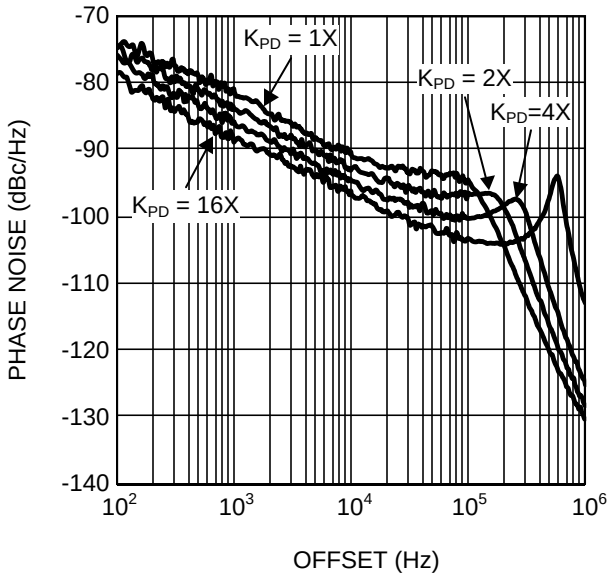

Figure 4. Charge Pump Current and 1/f Noise (f_{PD} = 50 MHz)

2.4 Integer PLL Spurs

Because the phase detector is updating the loop filter voltage at a rate equal to the phase detector frequency, there will be spurious tones at the output of the VCO at offsets equal to the phase detector rate. For an integer N PLL, this phase detector rate will be equal to the channel spacing. There are basically two causes of these spurs: leakage of the charge pump causes modulation on the VCO tuning line, which leads to spurs [1].

$$\text{LeakageSpur} = 20\cdot\log(2\pi\cdot\text{Leakage}/K_{PD}) + 20\cdot\log(N) + \text{rolloff}(f_{PD}) \quad (10)$$

In addition to this, there are other effects such as dead zone elimination circuitry and unequal turn on times of the PMOS and NMOS transistors in the charge pump. All these additional effects can be lumped into a single index called BasePulseSpur that can be used as an part-specific index. The spur due to these pulse effects can be modeled as [1]:

$$\text{PulseSpur} = \text{BasePulseSpur} + 20\cdot\log(N) + 40\cdot\log(f_{PD}) + \text{rolloff}(f_{PD}) \quad (11)$$

The integer PLL spur can be found by adding these two spur contributors together [1].

$$\text{IntegerSpur} = 10\cdot\log\left(10^{\text{LeakageSpur}/10} + 10^{\text{PulseSpur}/10}\right) \quad (12)$$

[1] goes into considerable detail as to the theory of integer PLL spurs and discusses how to predict them for various PLLs. If the phase detector frequency is low, then the LeakageSpur tends to dominate. If it is higher, then the BasePulseSpur tends to dominate due to the $40\cdot\log(f_{PD})$ term. Regardless of whether the spur is dominated by pulse effects or leakage effects, notice the $20\cdot\log(N)$ term in their calculations. This is why integer PLL spurs increase as $20\cdot\log(f_{VCO})$.

3 Traditional Fractional N PLLs

3.1 Fractional N Basic Concepts

Recall that for the integer N PLL, the phase detector frequency was limited to the channel spacing, or smaller. The reason for this is that the N counter is restricted to integers. For fractional PLLs, the N counter is allowed to assume some fractional values as well. The fractional denominator, Fden, for a specific device can either be fixed or programmable. Fnum is the fractional numerator and is intended to assume values from 0 to Fden-1. Traditional fractional N and delta-sigma fractional N PLLs are the same in this regard, although delta sigma PLLs typically have more flexibility for the choice of Fden due to architecture. The total N counter value is:

$$N = N_{INT} + Fnum/Fden \quad (13)$$

For fractional parts, the phase detector frequency can now be chosen as:

$$f_{PD} = GCD(f_{OSC}, f_{CH} \times Fden) \quad (14)$$

For a fractional PLL that has Fden programmable, Fden should be chosen to maximize the above expression for f_{PD}. For example, consider a case with a device that has Fden programmable from 2 to 128 with a f_{CH} = 1 MHz and f_{OSC} = 19.68 MHz. In this case:

$$f_{PD} = GCD (19.68 \text{ MHz}, 1 \text{ MHz} \times Fden) = 0.04 \text{ MHz} \times GCD (492, 25 \times Fden) \quad (15)$$

So Fden should be chosen from 2 to 128 and to have the largest possible common factor with 492. Since 492 = 2 × 2 × 41 × 3, it follows that a value of Fden = 41 × 3 = 123 would be the optimal choice. The phase detector frequency can be calculated as:

$$f_{PD} = 0.04 \text{ MHz} \times GCD (492, 25 \times 123) = 1.23 \text{ MHz} \quad (16)$$

Table 1 shows an example with a f_{CH} = 1 MHz channel spacing and a f_{OSC} = 19.68 MHz using three different kinds of PLLs.

Table 1. PLL Configuration Example

Parameter	Integer PLL Example	Fractional PLL Example	Delta Sigma Fractional PLL Example
f_{OSC}	19.68 MHz		
f_{VCO}	902-928 MHz		
f_{CH}	1 MHz		
Device	LMX2316	LMX2364	LMX2485
Doubler	No	No	Yes
Maximum f_{PD}	10 MHz	10 MHz	50 MHz
Minimum N Value	992	56	31
Allowable Fden	1	1 - 128	1 - 4194303
Chosen Fden	1	123	1968
f_{PD}	10 kHz	1.23 MHz	19.68 MHz
N Value	90200-92800	$733\ ^{41}/_{123}$-$754\ ^{58}/_{123}$	$45\ ^{1640}/_{1968}$ -$47\ ^{304}/_{1968}$

For the delta sigma fractional part, f_{PD} can be chosen as high as f_{OSC}. Although this device has a frequency doubler, the doubler can not be used because this would violate the minimum N counter value of 31. For the avid reader, the *AN-1865 Frequency Synthesis and Planning for PLL Architectures Application Report* (SNAA061) goes into more detail of how to calculate the GCD and calculate frequencies for fractional PLLs.

3.2 Theory of Operation

Traditional fractional N PLLs allow f_{PD} to be increased by allowing the N counter to assume fractional values. The way that this is achieved is that the the N counter is alternated between two integer values such that the average value is the desired fraction. Figure 5 shows a traditional fractional PLL with no analog compensation. Due to the digital nature of this circuit, it is common to represent this in the Z domain, which is discussed in more detail in Appendix A. The integer portion of the N counter value, N_{INT}, is handled normally and the fractional part is handled by additional fractional circuitry, which is made up of an accumulator and a quantizer. The previous output of the quantizer is subtracted from the input fraction and this error is added in the accumulator. When the error in the accumulator is less than one, the output of the quantizer is zero. However, when the error in the accumulator adds to one or more, then the output of the accumulator is one. On the next phase detector event, this output is subtracted from the fractional word input. In this way, the output of the quantizer is a stream of ones and zeros that have an average value equal to the desired fraction of Fnum/Fden.

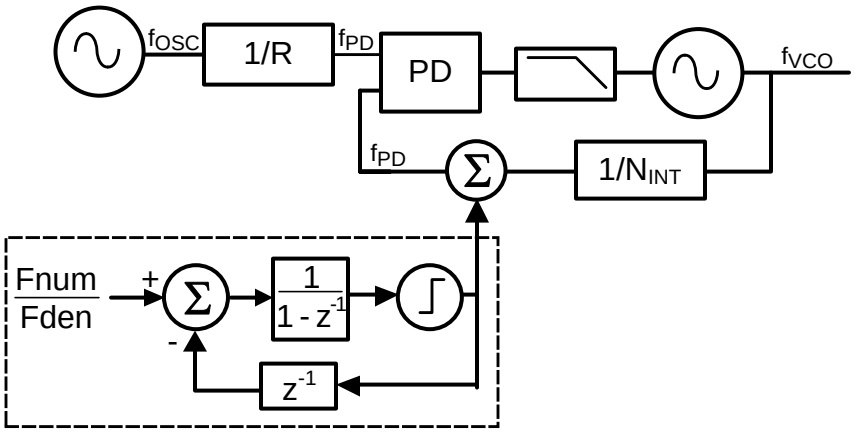

Figure 5. Traditional Fractional N PLL

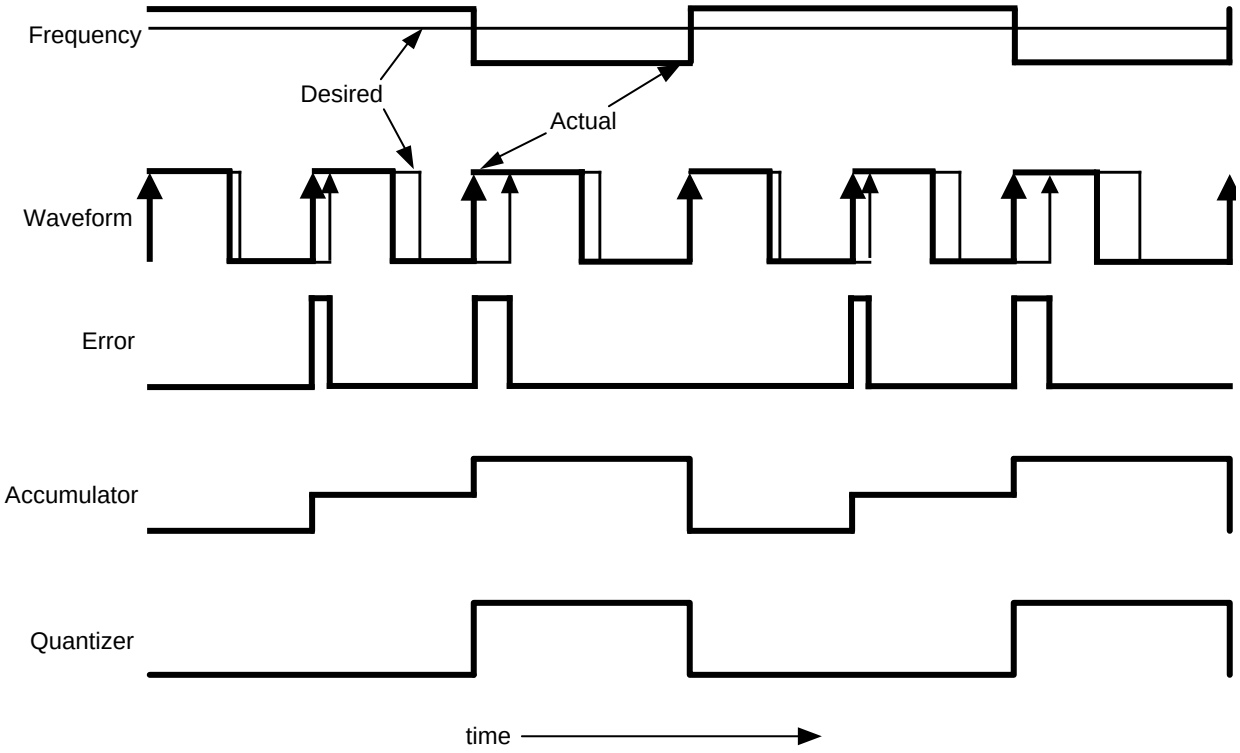

Figure 6. Uncompensated Fractional N Example

Consider the fractional PLL example in Table 1 with a desired output frequency of 902 MHz. In this case, the N counter value is 733 + $^{41}/_{123}$, which simplifies to a fraction of 733 $^{1}/_{3}$. For the first two times the divider divides by 733, the frequency will be too high, but then for the third time when the divider divides by 734, this frequency will be lower in an amount such that the total period is equal to the period of the ideal signal.

Figure 6 shows that although the average frequency is correct, the actual frequency is frequency modulated between 733 and 734 MHz. This frequency modulation gives rise to undesired spurious tones in the frequency domain. In the time domain, this can be viewed as an instantaneous phase error. Because this error is presented to the phase detector, which is triggered only on the rising edges of the output of the N counter, only the errors in the timing of the rising edges matters. This error gives rise to large fractional spurs if not corrected. For the traditional fractional PLL, there are two common methods that are used to compensate for this instantaneous phase error. One method is to allow this error to go to the phase detector/charge pump and then cancel the resulting error current it produces with a current of opposite polarity. The challenge with this method is that it is difficult to get a current value that is good over voltage, process and temperature. A second method is to use an analog delay to make the output correspond to the ideal output. Although this method might be easier to optimize over voltage, process, and temperature, it also adds phase noise. Both the current compensation and the delay methods can certainly reduce the spurs, but they have their imperfections.

3.3 Phase Noise for Traditional Fractional PLLS

Phase noise for traditional fractional N PLLs behaves in a very similar way to fractional PLLs with the exception that the fractional compensation may add noise. The nature of this noise is device specific. For instance, the LMX2364 uses analog delays to compensate for the fractional spurs. Because these analog delays are not perfect they add phase noise. For this device, the added phase noise is 7 dB to the PLL flat noise when this compensation is enabled. For traditional fractional N PLLs, one has to weigh the added benefits of the lower N counter value against the added noise from the fractional circuitry. Knowing that the PLL flat noise improve 3 dB every time the phase detector frequency is doubled, and that log (5) ~ 7, it follows that using this device in a fractional mode only provides a phase noise benefit if the phase detector frequency can be increased by at least a factor of 5.

3.4 Understanding Traditional Fractional N Spurs

The first step in understanding fractional spurs of any sort is to is to understand the behavior of a traditional fractional N PLL with no compensation for a worst case fraction. By doing a Fourier analysis on the quantizer output in Figure 6 the fractional spurs can be calculated as they are in [1] . Real world devices will have fractional compensation, and the effect of this will be to lower the fractional spurs by some fixed amount. For instance, the LMX2364 spurs can be predicted with good accuracy by mathematically calculating the uncompensated spur levels and then reducing all their levels by 18 dB. The magnitude of these fractional spurs will change around, but the worst case is when Fnum=1 and the offset frequency of this worst case spur will be f_{PD} / Fden. For this worst case, a device-specific index of InBandSpur can be extrapolated from measured data as is done in Table 2, which is what this worst case fractional spur would theoretically be with no filtering from the loop filter.

Table 2. InBandSpur for Various PLLs

Part	InBandSpur (Fnum = 1)	Comments
Theoretical (Uncompensated)	0 dBc	Calculated from pure theory Fden > 7
LMX2364 (Compensation Disabled)	1.6 dBc	Measured and very predictable
LMX2364 (Compensation Enabled)	-18 dBc	Measured and fairly predictable
LMX2470 (4^{th} Order Modulator)	-40 dBc	These numbers can vary based on setup conditions. Far outside the loop bandwidth, crosstalk effects may need to be considered.
LMX2485 (2^{nd} Order Modulator)	-36 dBc	
LMX2485 (3^{rd} Order Modulator)	-46 dBc	
LMX2485 (4^{th} Order Modulator)	-55 dBc	
LMX2531	-40 dBc	

In order to account for the effects of the loop filter, simply add the rolloff (refer to the rolloff equation in Section 2.2).

FractionalSpur (Worst Case) = InBandSpur + rolloff(f_{Spur}) **(Traditional Fractional Spur Equation)** (17)

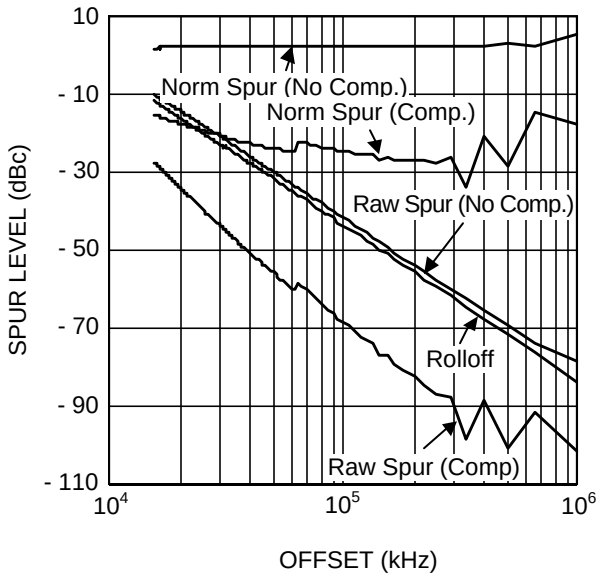

Figure 7. Traditional LMX2364 Fractional Spurs

Figure 7 shows fractional spurs measured on the LMX2364 evaluation board with setup conditions described in Appendix C. Fnum fixed at one and Fden varied from 2 to 128 in steps of one. For this example, f_{PD} was 2 MHz, so therefore the spur offset frequency in MHz was 2 / Fden. There are some minor irregularities, such as near 62 kHz offset frequency and at higher offsets, but these can be explained by part-specific behaviors of the LMX2364 and approximations that break down down for Fden < 8. However, the general trend of both the compensated and uncompensated fractional spur following the rolloff of the loop filter is clear.

So far, only first fractional spur, which is at an offset of f_{PD} / Fden has been discussed, but there are higher order fractional spurs. In general, the n^{th} fractional spur is at an offset equal to n × f_{PD} /Fden. These spurs can also be predicted, but typically they are less troublesome than the first fractional spur because they are at higher offsets and are easier to filter. These spurs can also be predicted with excellent accuracy, as done in [1]. One easy case where these can be predicted is in the case of the case when Fden is large (>20). In this case, the worst case for the n^{th} fractional spur occurs when Fnum = n and has a magnitude about the same as InBandSpur. For instance, if a part has InBandSpur of -18 dBc, f_{PD} = 2 MHz, Fden = 100, and Fnum = 7, then the spur at 140 kHz would be -18 dBc + rolloff(140 kHz).

The next question that might come up is how the first fractional spur might vary for a numerator that is not equal to one. One simple case is when Fnum = Fden -1, which yields the same spur spectrum as Fnum = 1. Following this case, the first thing one should check is that if Fnum and Fden have any common factors. If they do, then the first fractional spur will not be present. In the case that Fnum and Fden have a common factor, the easiest way to calculate the fractional spurs would be to simplify the fraction of Fnum / Fden to lowest terms and then to the analysis on this new fraction. For instance, if the fractional denominator was fixed to 123, the fraction is 3/123 would reduce to 1/41. So although most channels in this example would have fractional spurs at every multiple of 1.23 MHz / 123 = 10 kHz, this particular frequency would have fractional spurs at every multiple of 1.23 MHz / 41 = 30 kHz. Another way of thinking about this would be that the first and second fractional spurs are not present for this channel, but the third fractional spur would be present. So provided that the fraction simplifies to something with a numerator of 1 or Fden - 1, the fractional spurs can be predicted with the methods already discussed.

The next thing to account for is when the fraction simplifies to something that does not have a numerator of 1 or Fden - 1. To do this, a new term , SpurMagnitude, is introduced to quantify how close to the worst case the Fden is. A SpurMagnitude of one is the spur for the worst case numerator. A SpurMagnitude of 2 is for the second worst case numerator. Summarizing the results in [1] , the following generalization can be made:

$$\text{FractionalSpur} = \text{InBandSpur} + \text{rolloff}(f_{Spur}) - 20 \cdot \log(\text{SpurMagnitude}) \quad (18)$$

Table 3. In-Band Uncompensated First Fractional Spur

Spur	Fractional Numerator of Occurrence		Uncompensated In-Band Spur Magnitude	
	General Case	This Case	GeneralCase	This Case
Worst Case	1 and Fden-1	1 and 122	0 dBc	0 dBc
2nd Worst Case	int($^{Fden}/_{2}$) and Fden - int($^{Fden}/_{2}$)	61 and 62	-6 dBc	-6 dBc
3rd Worst Case	int($^{Fden}/_{3}$) and Fden - int($^{Fden}/_{3}$)	Not Present	-9.5 dBc	Not Present
4th Worst Case	int($^{Fden}/_{4}$) and Fden - int($^{Fden}/_{4}$)	Not Present	-12 dBc	Not Present
kth Worst Case	int($^{Fden}/_{k}$) and Fden - int($^{Fden}/_{k}$)	-20·log (SpurMagnitude) (If Present)		

Summarizing further the results of [1] , the second worst case for the spur occurs at when Fnum is int(Fden/2) or Fden - int(Fden/2). If it turns out that this value for Fden has common factors with Fden, then the second worse case is not present, and one just goes the third worst case. The third worst case occurs when Fnum is int(Fden/3) or Fden - int(Fden/3), provided that this value for Fnum has no common factors with Fden.. The k^{th} worst case occurs when Fden is int(Fden/k) or Fden - int(Fden/k), provide that this value for Fnum has no common factors with Fden. To further explain this, Table 3 applies this concept to the fractional PLL example given in Table 1 and assuming a theoretical uncompensated fractional PLL. In this case, Fden is 123 and the channel spacing is 10 kHz. Therefore, the first fractional spur will be 10 kHz offset from the carrier, and will have a worst case magnitude of 0 dBc occurring at a numerator value of 1 and 122. The second worst case for this fractional spur will be when the fractional numerator is int($^{123}/_{2}$) or int($^{123}/_{2}$ - 1) with a magnitude of -20·log (2). This works out to Fden = 61 or 62 with a magnitude of -6 dBc. Now for the third and fourth worst cases, these spurs are not present because int($^{123}/_{3}$) = 41 and int($^{123}/_{4}$) = 30 both have a common factor with 123. The pattern for the second and third worse cases for these higher order spurs is much more complicated than for the first order spur and beyond the scope of this application note. For more detailed information on these spurs, the avid reader is encourage to consult [1] .

In some applications it may be possible to avoid some of these worst case spurs by changing the TCXO frequency or shifting the VCO frequency. For this example, consider what would happen if the crystal frequency was changed to 10 MHz. In this case, the phase detector frequency could be raised to 10 MHz, and the fractional spurs would be at offsets in multiples of 1 MHz from the carrier, instead of 10 kHz. This would be a massive improvement. However, further improvement is possible still. If the TCXO frequency was changed to 30 MHz, then, the fractional denominator, Fden, would be 30. Now the worst case fraction would be when the fractional numerator would be 1 or 29. However, these values correspond to frequencies of 901 MHz and 929 MHz, which are both out of the frequency band of 902 – 928 MHz, so these worst case numerators could be avoided. The second worst case would be when the fractional numerator is 15, but since this divides evenly into 30, the first fractional spur would not be present in this case either. The same thing would happen for the third fractional spur. So finally, on the fourth fractional spur, this spur would be present, but theoretically it would be 12 dB lower than what it would be for the 10 MHz TCXO.

In conclusion, the worst and most troublesome cases for traditional fractional spurs can be reasonably modeled provided that the fraction and rolloff are known. One observation regarding fractional spurs that, unlike integer PLL spurs, fractional spurs are theoretically independent of VCO frequency. This lays the foundation for the understanding for all fractional spurs, but for delta-sigma PLLs there are other complexities that need to be considered.

4 Delta-Sigma PLLs

4.1 Theory of Operation

For the traditional fractional PLL, analog compensation is used to reduce the fractional spurs, although this has its shortcomings. Delta sigma PLLs aim to reduce spurs using digital techniques so that there is minimal added phase noise and the fractional spurs are reduced even lower. There are really two common digital techniques that are employed. The first technique involves varying the N counter value over a wider range of values in order to reduce the primary fractional spurs. Just as the first order modulator alternates the N counter between two values, the n^{th} order delta sigma fractional PLL modulates the N counter between 2^n different values. Expanding on the example presented for the traditional fractional PLL, instead of using just the values of 773 and 774 to achieve 773 1/3, the values of 772, 773, 774, and 775 could be used in a second order delta sigma PLL. A third order modulator could alternate between 8 different counter values and a fourth order modulator could alternate between 16 different counter values. As a rule of thumb, higher order modulators outperform lower order modulators, but not in all situations; this is application specific.

Table 4. Delta Sigma Modulator Example

Modulator Order	Range	Sample Sequence
First (Traditional PLL)	0, 1	773, 773, 774, ...
Second	-1, 0, 1, 2	772, 774, 771, 773, 775, 774, ...
Third	-3, -2, ..., 3, 4	770, 773 ,774, 771, 772, 776, 775, 772, 770, 771, 777, 772, ...
Fourth	-7, -6, ..., 7, 8	766, 777, 770, 767, 781, 780, 769, 771, 774, 773, 775, 776, 768, 780, 768, 771, 773, 781, 780, 772, 777 772, 770, 769 ...

A second technique used to improve sub-fractional spurs in delta sigma PLLs is called dithering. For the first order modulator example in Table 4, the cycle repeats every three time steps (each time step is $1/f_{PD}$). The period is twice that for the second order modulator, 4 times that for the third order modulator, and 8 times that for the fourth order modulator. This periodicity is undesirable and can give rise to sub-fractional spurs, which are spurs that occur at a fraction of the primary fractional spur frequency. In order to reduce this periodicity, a technique called dithering can be used. Dithering involves randomizing this sequence so that it is pseudo-random and the period is not so obvious. By doing this, the sub-fractional spurs are reduced. In practice, dithering impacts sub-fractional spurs, but has little impact on the primary fractional spurs. In some situations, it can add small amounts of phase noise.

The traditional fractional PLL as shown in Figure 5 is technically a first order delta sigma PLL with analog compensation, although the industry standard for the term "delta-sigma" PLL typically assumes no analog compensation and the order is at least second order or at least dithering is used. There is more than one way to create a higher order delta sigma PLL, but one common way is the the MASH (Multi-stAge noise SHaping) architecture. In this architecture, the output of each stage is fed into the next stage, and the errors from all stages are summed together. Figure 8 shows a third order delta sigma PLL using MASH architecture.

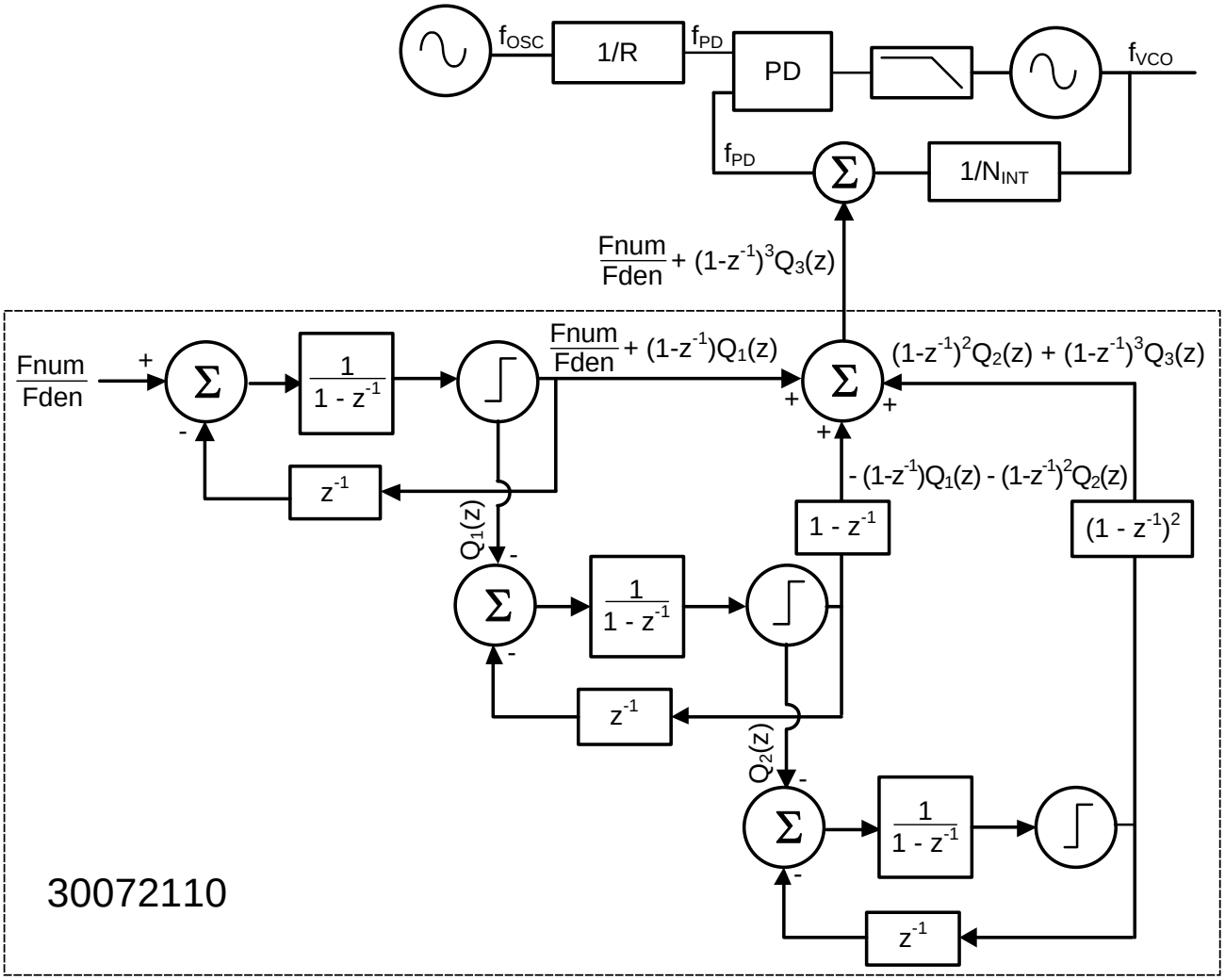

Figure 8. Third Order Delta Sigma Modulator

4.2 Delta Sigma PLL Phase Noise

4.2.1 Simplified Delta Sigma Phase Noise

Figure 8 shows that the quantization noise from all stages except for the last is canceled out. If one makes the simplifying assumption that the quantizer output is a uniformly distributed random variable between zero and one, the spectral density of an n^{th} order delta sigma modulator can be calculated as follows [4]:

$$\left|Y_{Noise}(f)\right|^2 = (2\pi)^2 \cdot \left(2 \cdot \sin\left(\frac{\pi \cdot f}{f_{PD}}\right)\right)^{2(n-1)} \cdot \left(\frac{1 \cdot Hz}{12 \cdot f_{PD}}\right) \quad (19)$$

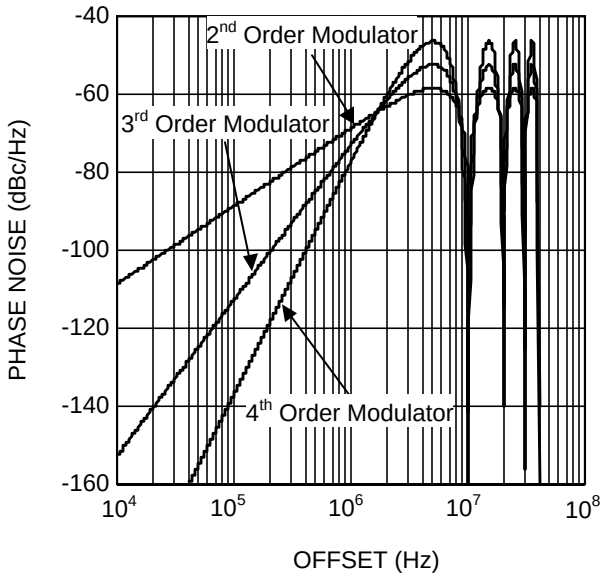

Figure 9. Simplified Delta Sigma Modulator Noise (f_{PD} = 10 MHz)

Figure 9 shows this theoretical noise for a 10 MHz phase detector frequency. Notice at 5 MHz, which is exactly half of the phase detector frequency, there is a maximum value. In general, the quantization noise achieves its maximum value at $f_{PD}/2$. After this frequency, the noise decreases and is also attenuated more by the loop filter. Therefore, it is this particular frequency that commonly is the one that is most likely to cause a problem. The theoretical value of this peak value in the noise is shown in Table 5.

Table 5. Magnitude of the First Lobe vs. f_{PD}

f_{PD}	2nd Order Modulator	3rd Order Modulator	4th Order Modulator
1.25 MHz	-49.8	-43.8	-37.8
2.5 MHz	-52.8	-46.8	-40.8
5 MHz	-55.8	-49.8	-43.8
10 MHz	-58.8	-52.8	-46.8
20 MHz	-61.8	-54.8	-49.8
40 MHz	-64.8	-57.8	-52.8

It can also be shown that for offsets that are much less than $f_{PD}/2$, the noise increases with a slope of 20·(n-1) dB/decade. In other words, if the order of the modulator is increased, then a higher order loop filter may be necessary. One rule of thumb for delta sigma PLLs is that the order of the loop filter should be one greater than the order of the delta sigma modulator. This rule is approximate and over-conservative in some cases. In practice, if the loop bandwidth is narrow enough, then these higher order loop filters may not be necessary. It also turns out that although the fourth order modulator would theoretically require a fifth order loop filter, a fourth order loop filter is typically sufficient. Appendix B has more properties of the delta sigma modulator noise as well as their corresponding derivations.

4.2.2 Measured Delta Sigma Noise and Randomization Effects

In order to validate the modulator noise equation in Section 4.2.1, a LMX2485 PLL evaluation board was used with the wide loop bandwidth setup in Appendix C to have the rolloff as described in Figure 2. It must be firmly emphasized that many of these examples are done with much less filtering than is typically used to fully expose all the effects to be studied. In other words, it is invalid to compare these results to some other results without taking into account the impact of the loop filter. The measured delta sigma noise with the rolloff subtracted away is shown in Figure 10.

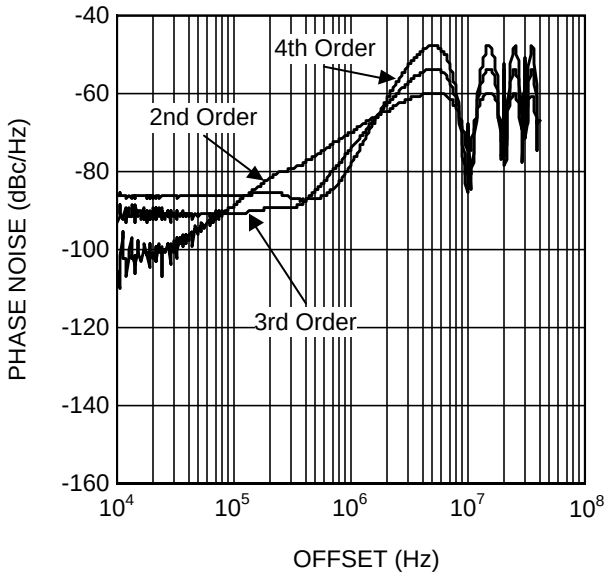

Figure 10. Measured Delta Sigma Modulator Noise (f_{PD} = 10 MHz, Strong Dithering, Fraction = 1/4914303)

Comparing the measurements to the theoretical data, there is excellent agreement except at very low frequencies. At these low frequencies, the noise becomes flat. Further experiments showed that there was no consistent trend for this low offset noise for a particular modulator order, phase detector frequency, dithering mode, output frequency. In this case as shown in Figure 10, the quantization noise was well randomized and the assumption that it is a uniformly distributed random variable between zero and one holds. This is why there is such nice agreement.

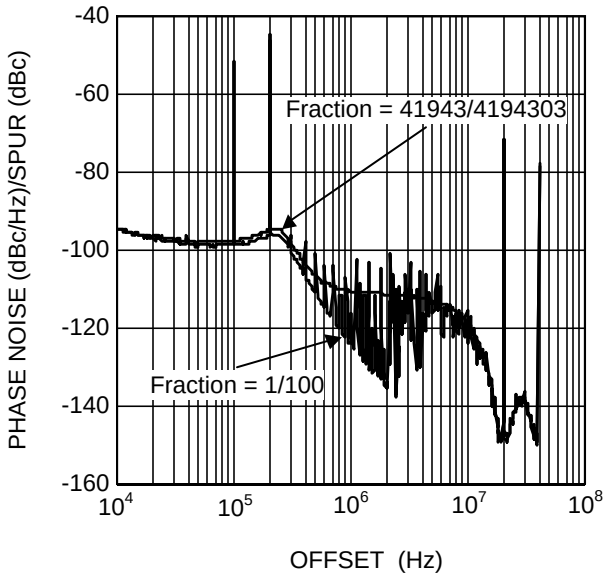

Figure 11. Impact of Fractional Denominator (f_{PD} = 10 MHz, No Dithering, 3rd Order Modulator)

Figure 11 shows the raw phase noise data taken with an E5052 phase noise analyzer with the spurs in dBc. Even though both fractions are both very close to 1/100, the one with the larger denominator shows that the noise is much more uniformly distributed with less discrete spurs, especially the one at 100 kHz offset.

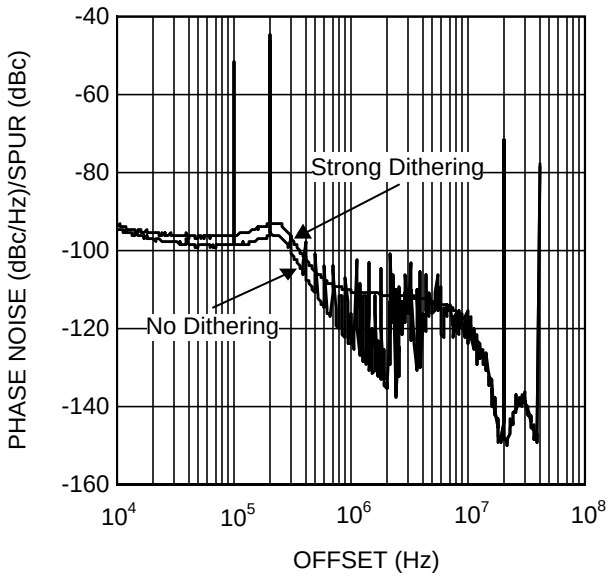

Figure 12. Impact of Dithering (f_{PD} = 10 MHz, Order = 3rd, Fraction = 1/100)

When dithering was used, this also made the noise more randomized as shown in Figure 12.

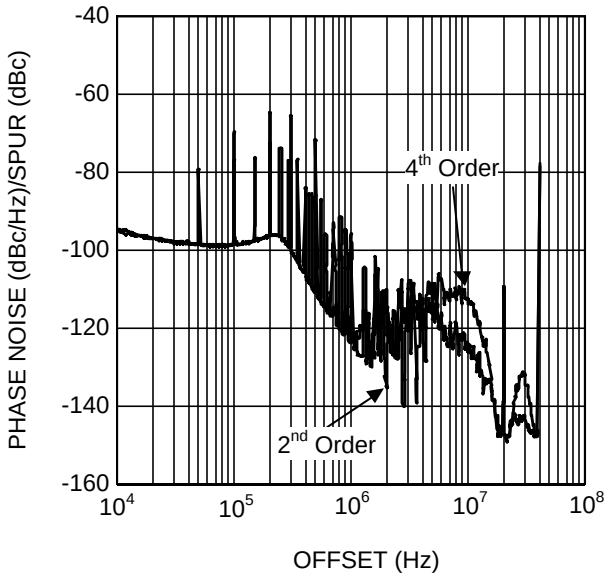

Figure 13. Impact of Modulator Order (f_{PD} = 10 MHz, No Dithering, Fraction = 1/100)

Figure 13 shows the impact of the modulator order. Although higher order modulator does seem to produce less spurious content in this case, it is much more obvious in Figure 14 where the fraction of 1/100 is expressed in higher terms of 10000/1000000.

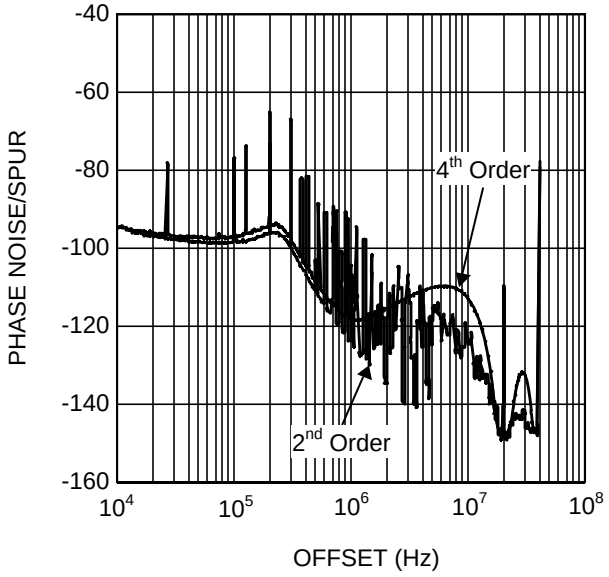

Figure 14. Impact of Modulator Order (f_{PD} = 10 MHz, No Dithering, Fraction = 1000/1000000)

These figures demonstrate that the delta-sigma modulator noise is best randomized when large fractions, higher order modulators, and dithering is used. Although these conditions are best for randomizing the delta sigma modulator noise, they might not be right for every application. In some situations, expressing fractions in larger terms might give rise to additional spurs at lower offsets. Higher order modulators help with randomization and also the primary fractional spur, but sometimes give rise to sub-fractional spurs that occur at a fraction of where the fractional spur would occur. Dithering randomizes the noise, but sometimes can degrade close-in phase noise. Also, if dithering is used with a fractional numerator of zero, it creates noise and spurs that would otherwise would not be there.

4.3 Delta Sigma Fractional Spurs

In general, delta sigma spurs can be of two types: primary and sub-fractional. The primary spurs are those that would occur at offsets that would be the same as a traditional fractional N PLL. There are various things that can be done to adjust their level, but they behave and can be modeled in the same way as traditional N fractional spurs. The other type of spurs are sub-fractional spurs that occur at an offset that is a fraction of where the primary fractional spur occurs. These spurs rolloff with the loop filter in a similar way as the primary fractional spurs, but there are many nuances to their behavior. The following sections go into discussion of both of these types of spurs.

4.3.1 Understanding Delta Sigma Primary Fractional Spurs

Delta sigma PLLs greatly reduce the in-band fractional spur by modulating the N counter value with more than two values. Although the compensation is digital, the spur levels are impacted by many factors. All of the architecture specific factors can be captured in the in-band spur metric. However, there are also many other settings that can be under the user's control that also impact these spur levels, such as phase detector frequency and modulator order. These effects are often difficult to predict and often pure textbook predictions with no grounding of measured results can be far off. Recall that for phase noise, it was assumed that the quantization noise, Qn(t) was uniformly distributed between 0 and 1. A lot of the effects seen on spurs are seen because this noise is not uniformly distributed in this manner.

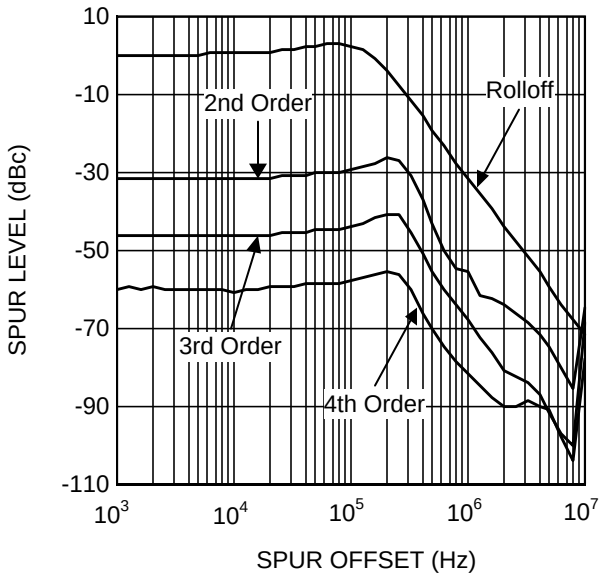

Figure 15. Measured Fractional Spurs
(f_{PD} = 10 MHz, Strong Dithering, Fraction = x / 4194303)

Figure 15 shows delta sigma primary fractional spurs measured on the same modified LMX2485 evaluation board. It should be emphasized that although this figure and many others to follow might appear as a smooth graph, they are really a collection of discrete spur measurements taken with an automated test program over many different fractional numerators and should not be confused with phase noise plots.

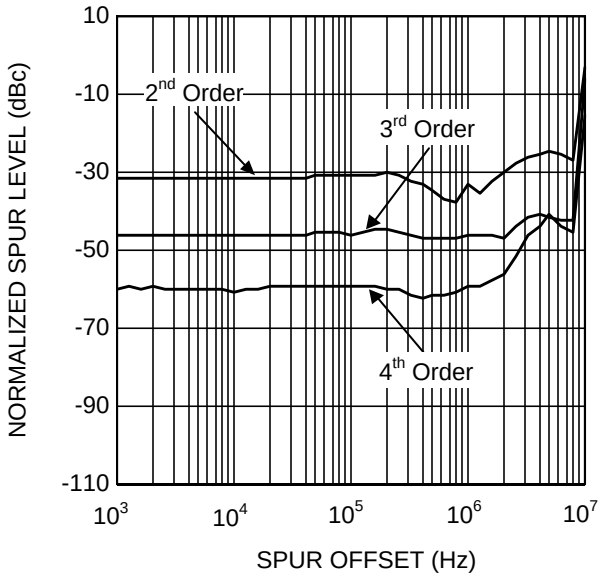

Figure 16. Normalized Fractional Spurs
(f_{PD} = 10 MHz, Strong Dithering, Fraction = x / 4194303)

Figure 16 shows the normalized fractional spurs, which are the measured fractional spurs with the rolloff subtracted away.In Figure 16, the normalized fractional spurs are relatively consistent until the spur offset gets close to f_{PD} / 2, which is the same offset where the phase noise peaks. Furthermore, at 1.67 MHz, which is f_{PD}/ 6, the difference in normalized spur levels between modulator orders is about the same as it is in-band. Experiments with other loop bandwidths and phase detector rates show that this unshaped peaking at f_{PD}/2 is not really impacted much by the loop bandwidth, although it will always be at a frequency higher than the loop bandwidth because the PLL loop bandwidth can only be made as wide as about f_{PD} / 10. Although there is the shaping of the modulator at offsets far outside the loop bandwidth, these effects can easily be masked by spurs due to crosstalk, so it makes little sense to try to account for this. In other words, primary delta sigma fractional spurs can be roughly modeled in the same way as traditional fractional spurs. There may be various settings that can impact the value for InBandSpur, such as the modulator order, but once this is known for one offset, it can be estimated for any other offset as well. For offsets far outside the loop bandwidth, there are crosstalk effects that will be discussed later.

4.3.1.1 Impact of Dithering and Fractional Numerator on Delta Sigma Primary Fractional Spurs

All the discussion so far has been done assuming a worst case fraction, which is a fractional numerator of 1 and Fden-1. For traditional fractional spurs, there was a big advantage if one could avoid the fractional numerator of 1 or Fden-1. For delta sigma PLLs, this benefit becomes more blurred and harder to predict, but is generally true provided that the fraction is well-randomized. In general, any large fraction (after being simplified to lowest terms) is well randomized. Also, for fractions that do simplify, such as 10000/100000, they still can be well randomized if higher order modulators (3rd or 4th) are used. Dithering is typically useful to make any fraction act more randomized, but if the fraction is small, it may also create extra phase noise and spurs at other offsets.

Figure 17 shows data taken from the LMX2485 PLL with a fractional denominator of 101. The phase detector frequency was 10 MHz and the spur at (10 MHz/101 = 99 kHz) was measured every time. The loop bandwidth was made very wide, so this is mostly inside the loop bandwidth. If dithering is not used, then basically every spur for every numerator looks like the worst cases of 1 and 100. However, if dithering is used, then there is a huge advantage if the worst case numerators of 1 and 100 can be avoided. Furthermore, by traditional PLL N theory, the next worse case would be for a fractional numerator of 50 and 51 which Table 3 would predict to be 6 dB lower. In this case they are closer to 20 dB lower! This experiment shows it can be very worthwhile to avoid these worst case spurs with delta sigma PLLs and dithering can be helpful.

Figure 18 shows the same experiment with a fractional denominator of 11. In this case, dithering helped all around with the spurs, since the fractional numerator was less randomized. However, now it is only about a 12 dB benefit of avoiding the worst case numerators of 1 and 10.

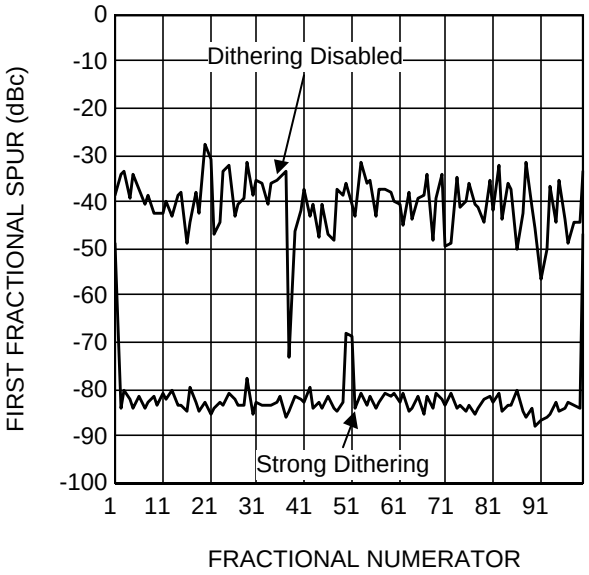

Figure 17. Impact of Fractional Numerator (Fraction = x / 101, LMX2485 PLL)

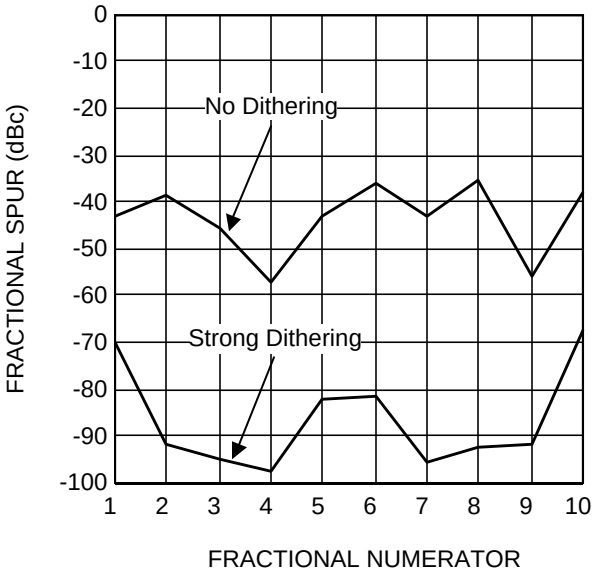

Figure 18. Impact of Fractional Numerator (Fraction = x / 11, LMX2485 PLL)

4.3.2 Accounting for Crosstalk Effects on Primary Delta Sigma Fractional Spurs

For integer PLL spurs and traditional fractional PLL spurs, the models presented so far do a good job at predicting the spur levels. However, for primary delta sigma fractional spurs that are far outside the loop bandwidth, measured data quickly shows that there are other effects that need to be accounted for. Figure 19 shows primary fractional spurs measured an LMX2485 PLL. Far outside the loop bandwidth, the modulator order has minimal impact. If the rolloff is subtracted from the raw spur levels, then the normalized spur can be found as shown in Figure 20. Looking at this figure, you can see that the normalized spurs are nothing close to being a constant at frequencies outside the loop bandwidth and the fractional spur equation presented in Section 3.4 needs some adjustment.

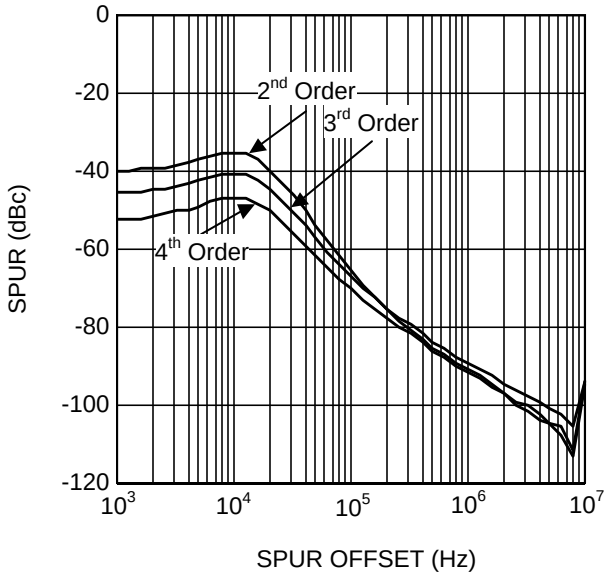

Figure 19. Raw LMX2485 Spurs (BW = 10 kHz)

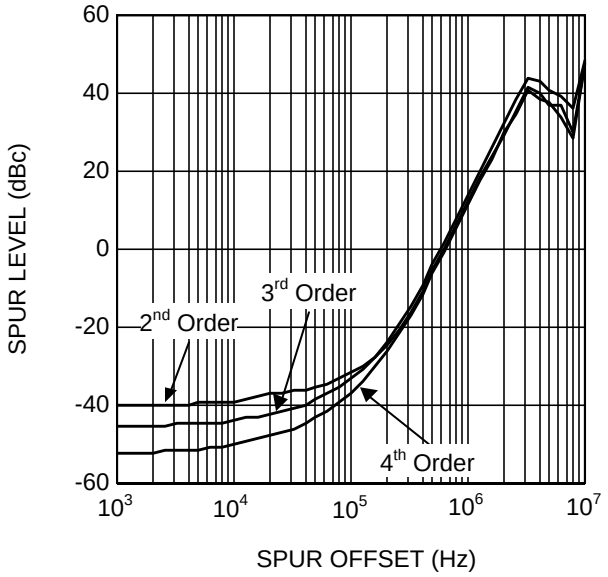

Figure 20. Normalized LMX2485 Spurs (BW = 10 kHz)

Judging from the behavior of these primary delta sigma fractional spurs at high offsets, it seems that the unexplained effects are not being directly filtered by the loop filter. In fact, it seems that these unexplained effects follow the transfer function of the VCO rather than the PLL. The natural things to suspect would be noise on the VCO power supply or noise produced at the high frequency input pin getting back to the VCO output. Experiments were done on the LMX2485 evaluation board to investigate this and it was found that increasing the filtering to the VCO power supply had minimal impact, but there the spurs could be improved about 5 dB by decreasing the DC blocking capacitor or increasing the series resistor to the high frequency input pin. Because these spurs do not seem to be directly filtered by the loop filter, they will be referred to as crosstalk spurs (XtalkSpur). However, the nature of this crosstalk seems to be more something related to the isolation between the VCO output and the N counter input rather than crosstalk between board traces.

In Figure 19, observe that the spurs degrade at 20 dB/decade with the spur offset frequency. By treating the spur offset frequency as the modulation frequency and applying traditional FM modulation theory, these 20 dB/decade degradation of these spurs can be explained by:

$$\text{Spur} = 20 \cdot \log(\beta) \quad \beta = \text{Frequency Deviation} / \text{Modulation Frequency} \tag{20}$$

One factor that seems to have an impact on these crosstalk dominated spurs is the charge pump current. Figure 21 shows the impact of changing the charge pump current on this normalized spur for the LMX2485 PLL. Decreasing the charge pump current helps to a point, but after a certain threshold is reached, then it does not help any more.

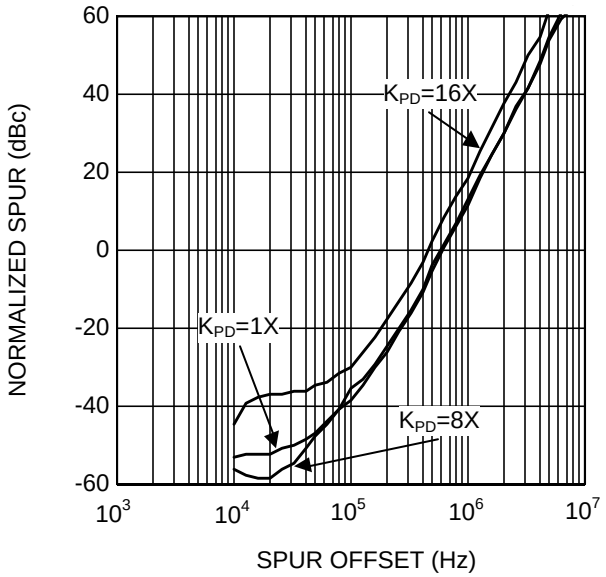

Figure 21. Normalized Spur Levels vs Charge Pump Current

In general, the following observations have been made regarding these crosstalk dominated spurs (XtalkSpur):

- General Observations:
  - Crosstalk effects are typically far outside the loop bandwidth.
  - These spurs decrease 20 dB/decade, regardless of the number of poles in the filter.
  - These spurs follow the shaping of the VCO transfer function
  - These spurs can be normalized to a 1 MHz offset frequency to create the index of BaseXtalkSpur.
  - Although loop filter may have some residual impact, these spurs are not impacted nearly as much as the rolloff would predict
  - They increase as $10 \cdot \log(K_{PD})$ beyond a certain charge pump current
  - There may be some dependence, but there is no clear trend with f_{VCO}

- LMX2485 Observations:
  - Normalized crosstalk Spur is independent of f_{PD}
  - Reducing the coupling cap to the Fin pin may improve this spur a few dB
  - BaseXtalkSpur is about -93 dBc for K_{PD}=1X
  - Below K_{PD} = 8X, charge pump current has no large impact
  - Increasing the resistor, or decreasing the capacitor at the FinRF pin can lower these spurs a few dB.
  - For narrow loop bandwidths and in-band fractional spurs at offsets more than half of the loop bandwidth, it is possible to see the effect that the in-band fractional spur gets lower if the loop bandwidth is widened. This would suggest crosstalk effects.
- LMX2531 Observations:
  - Crosstalk spur increases as $10 \cdot \log(f_{PD})$
  - BaseXtalkSpur is about -99 dBc for 1X charge pump current and f_{PD} = 2.5 MHz
  - Even between 1X and 2X charge pump current, there is a 6 dB difference in this spur.

In general, the total fractional spurs for the LMX2485 and LMX2531 families of delta sigma PLLs can be decomposed as:

$$\text{TotalFractionalSpur} = 10 \cdot \log\left(10^{\text{FractionalSpur}/10} + 10^{\text{XtalkSpur}/10} \right) \quad (21)$$

Figure 22 shows how the fractional spur levels shown in Figure 19 can be decomposed into a FractionalSpur and a XtalkSpur.

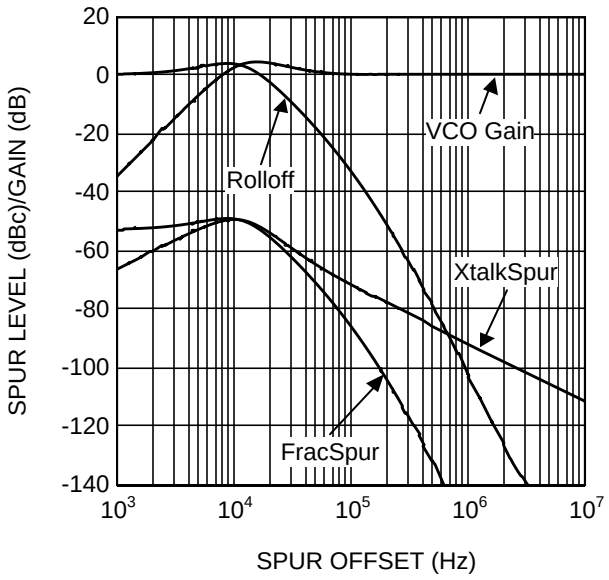

Figure 22. Theoretical Spur Decomposition (4th Order Modulator)

In Figure 22, observe the XtalkSpur at farther offsets decreases 20 dB/decade and tracks the VCO transfer function. The crosstalk spur can therefore be normalized to a 1 MHz offset frequency to create a part-specific index, BaseXtalkSpur, which relates to the crosstalk spur as:

$$\text{XtalkSpur} = \text{BaseXtalkSpur} - 20 \cdot \log(\text{offset} / 1\text{MHz}) - 20 \cdot \log(\mid (1+G(2\pi \cdot j \cdot \text{offset}) / N) \mid) \quad (22)$$

At offsets far outside the loop bandwidth, the transfer function for the VCO is one, but at frequencies below the loop bandwidth, it is less than one. Applying this theoretical model against the modeled data, Figure 23 shows that this model fits the measured data quite well.

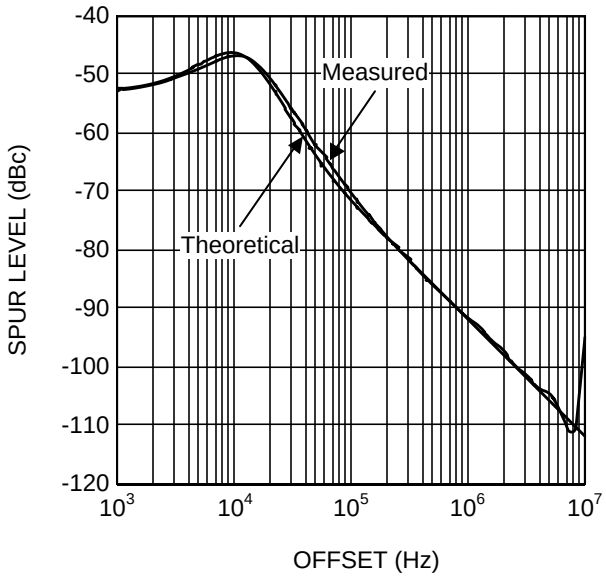

Figure 23. Theoretical vs. Measured Data (LMX2485 PLL, Standard Loop Filter, 4th Order Modulator

The observations presented here are based on the LMX2485 and the LMX2531 evaluation boards, that may have some influence on the value of BaseXtalkSpur. If the spur level is high relative to crosstalk effects, then these crosstalk effects can be ignored. However, if their level is low, as is the case for delta-sigma fractional spurs far outside the loop bandwidth, crosstalk effects need to be considered. Although these crosstalk effects could technically apply to all spurs, they are included in the discussion of delta sigma fractional N spurs because this is the only case where it really has a noticeable impact. Figure 7 shows spurs with a traditional fractional PLL that do not show these crosstalk effects, so this suggests that these crosstalk spurs may be something that are more inherent to delta sigma PLLs.

In conclusion, crosstalk effects are too significant to not be considered for delta sigma primary fractional spurs that are far outside the loop bandwidth. For integer PLL and traditional fractional PLL spurs, these crosstalk effects have not been observed. Perhaps the reason for this is that delta-sigma spurs are lower and therefore some of these crosstalk effects are more exposed. Another possible explation is that the digital fractional circuitry in delta sigma PLLs could be producing noise that can crosstalk on the chip itself. If there is a question rather crosstalk effects are really dominating a spur, one simple test is to simply program the modulator order to a different value and see if the spur changes. If it does not, then this implies that crosstalk effects may be at play.

4.3.3 Delta Sigma Sub Fractional Spurs

For the first order modulator example in Table 1, the cycle repeats every three time steps (each time step is $1/f_{PD}$). The period is twice that for the second order modulator, 4 times that for the third order modulator, and 8 times that for the fourth order modulator. For this example, the second order modulator would theoretically have an a fractional spur that is ½ of the offset frequency (in addition to the primary fractional spur) because the period is twice as long. The third order modulator would theoretically have a sub-fractional spur that is $1/4^{th}$ of the primary fractional spur offset in addition to these other existing spurs. The fourth order modulator would have all these existing spurs and also a spur at $1/8^{th}$ of the offset of the primary fractional spur, although this sub-fractional spur is typically not present. These sub-fractional spur levels can change based on the fraction used, part architecture, dithering mode, and various bit settings in the part, which makes them a challenge to theoretically predict.

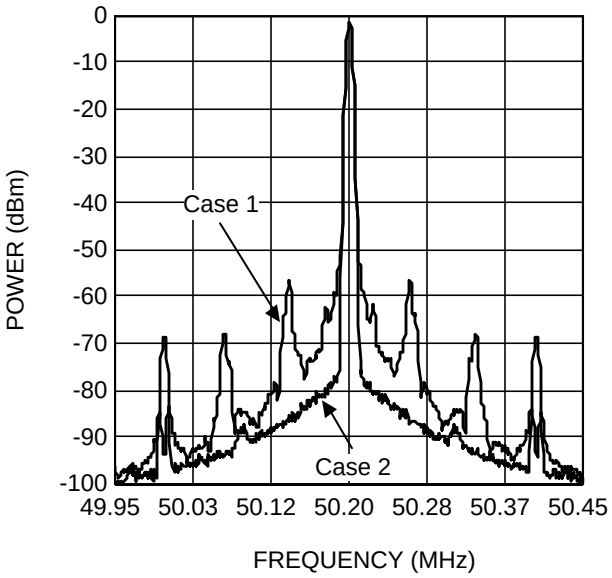

Figure 24. Sub-Fractional Spurs (LMX2485E PLL, f_{PD} = 2 MHz,2nd Order Modulator)

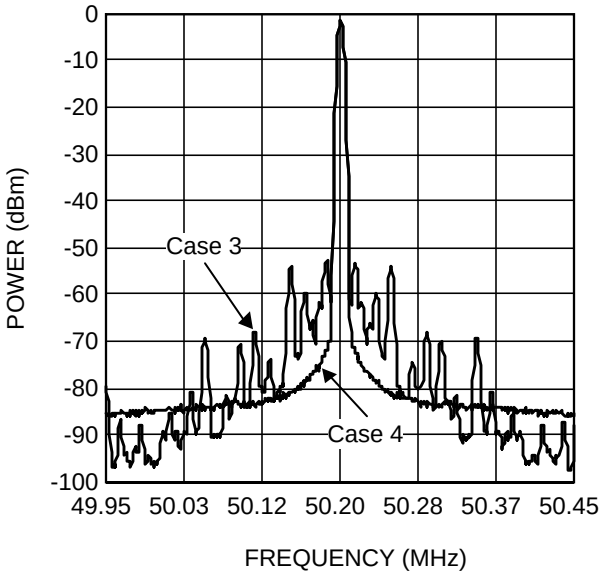

Figure 25. Sub-Fractional Spurs (LMX2485E PLL, f_{PD} = 2 MHz,2nd Order Modulator)

Figure 24 and Figure 25 show an LMX2485E PLL with a 200 kHz channel spacing at 50.2 MHz output frequency. Depending on how the part is set up, the sub-fractional spurs can vary. For case 1, the PLL was tuned to 50.2 MHz with a fractional word of 10000 / 50000 and dithering disabled. The result is a spectrum full of sub-fractional spurs that looks terrible. In case 2, the modulator was first reset, then set to 2nd order. Although the final settings for the part are exactly the same, the action of the modulator dramatically improved the spurs. In case 3, the PLL in case 2 was tuned to 50.1 MHz and then back to 50.2 MHz and the spurs again became very bad. What is going on is that the starting place in the delta sigma sequence is different. By using the reset modulator, this basically ensures a predictable spur

performance, although it is a hassle. If dithering is used as in case 4, this issue of unpredictable spurs is resolved, but then the phase noise is greatly increased. For this example, the delta sigma noise and spurs are emphasized because the lower VCO frequency. This is because although other noise sources improve with lower VCO frequency, , the delta sigma modulator noise and spurs are theoretically independent of f_{VCO}.

One confusing thing about sub-fractional spurs is that they can change based on the initial starting point of the modulator input. If they are measured at a particular frequency, then the VCO is tuned away and tuned back to the original frequency, they can change. Some parts have features such as dithering and an automatic reset of the modulator that can these more predictable. This erratic behavior of sub-fractional spurs is emphasized in cases with wide loop bandwidths, low VCO frequencies, and low phase detector frequencies. In addition to this, the sub-fractional spurs tend to be more erratic for the second order modulator because it does not randomize enough in some cases. The third and fourth order modulators typically have less of an issue with this randomness. Dithering is very effective in making the sub-fractional spurs more predictable, but should be used with caution because it can increase the phase noise in certain situations. When dithering is used, it is often beneficial to express the fraction in higher terms.

In other words, even though 1/5 and 10000 / 50000 are mathematically equivalent, the larger fraction may yield better sub-fractional spurs. On the other hand, in this case, it can also create a bunch of sub-fractional spurs at multiples of f_{PD}/50000. If a fraction is not well randomized, then the phase noise lobes are typically broken up into smaller spurs. Inside the loop bandwidth, the fractional spurs are similar, but outside the loop bandwidth, the well randomized fraction typically can have better spurs than the randomized fraction.

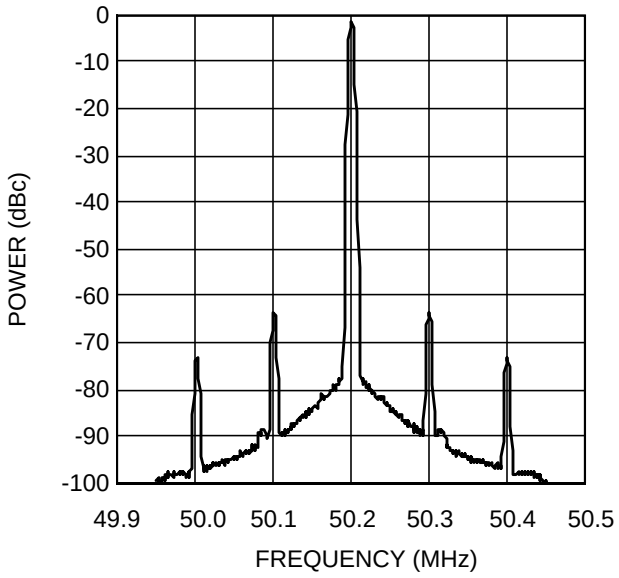

Figure 26. LMX2485E Fractional Spurs (Fden = 1/4)

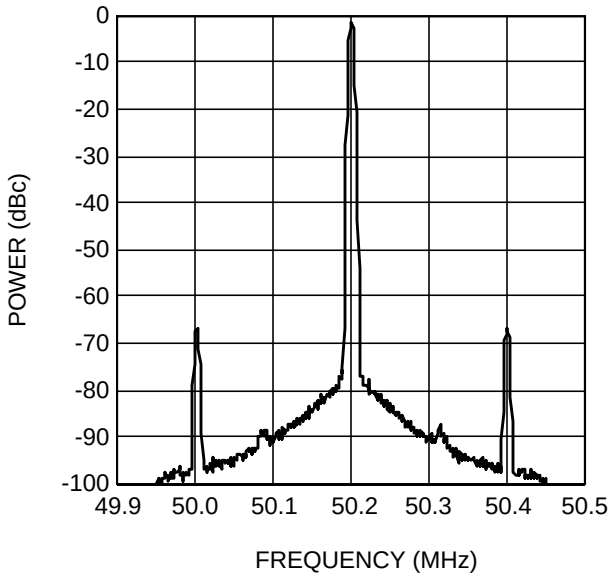

Figure 27. LMX2485E Fractional Spurs (Fden = 1/5)

For the LMX2485 family of delta sigma PLLs, expressing the fraction with an odd denominator can help as shown in Figure 26 and Figure 27. In this case, the phase detector frequency was shifted from 800 kHz to 1 MHz and this eliminated the sub-fractional spurs at the expense of making the primary fractional spurs a few dB higher. For the LMX2485 family of PLL, this relationship seems to hold for all odd denominators.

In conclusion, although sub-fractional spurs can be deterministic if the part is set up in a given way, there are many inherent nuances and it is very difficult to find one single rule that is best in all situations. It is difficult to know the optimal way to configure a part to reduce or eliminate these spurs without some experimentation. Theory and models can take one so far, but there is no substitute for the timeless techniques of trial and error and the process of elimination [5].

5 Comparing Integer and Fractional N PLL Performance

One natural consideration is to know when it is best to use a fractional N PLL. The answer is application specific, but some general rules of thumb is that fractional N PLLs provide the most benefit to performance for narrower channel spacings. Comparisons tend to be apples to oranges because integer PLL and fractional PLLs can have other differences, such as different charge pumps and phase detectors. Nevertheless, some comparisons of phase noise and spurs can be made, if done in the right way.

5.1 Comparing Phase Noise

Whether valid or not, there will be those who insist on doing an apples to apples comparison between integer and fractional PLLs without providing the context of the application. One commonly used but completely invalid way to directly compare is to simply the 1 Hz normalized phase noise (PN1Hz). However, this method is completely invalid if the differences in phase detector frequency are not accounted for by adding the following term to the integer PLL phase noise index:

$$\text{Fractional Advantage} = 10 \cdot \log(f_{PD}(\text{Fractional PLL}) / f_{PD}\ (\text{Integer PLL}) \quad (23)$$

Consider the comparison between the LMX2531 (PN1Hz = -212 dBc/Hz) and the LMK03000 (PN1Hz = -224 dBc/Hz). Observe that the LMK03000 has 12 dB better normalized phase noise. If both parts were operated at the same phase detector frequency, then this 12 dB difference would be real, at least at farther offsets, but because the LMX2531 is fractional and the LMK03000 is an integer PLL, this comparison is not fair. If the channel spacing was 200 kHz and the crystal frequency was 10 MHz, then the correction would be 17 dB, implying that the LMX2531 would be 17 - 12 = 5 dB better at farther offsets. At closer offsets (<10 kHz), one would have to compare the 1/f noise and the noise of the crystal. On the other hand, if the channel spacing was 10 MHz and the crystal frequency was 10 MHz, then there is no Fractional Advantage and maybe an integer part would make more sense.

5.2 Comparing Integer Spurs to Fractional Spurs

Both integer and fractional N PLLs will produce spurs at an offset from the carrier equal to the channel spacing. One natural question to ask would be to know which part would have lower spur levels. [1] describes how to calculate these spurs for integer PLLs and these have also been discussed for fractional PLLs. A summary of these results is in Table 6.

Table 6. Spur Comparison

PLL Type	Spur Type	Formula
Integer	Pulse Spur	PulseSpur = BasePulseSpur + 40·log(f_{PD}) + rolloff(f_{PD})
	Leakage Spur	LeakageSpur = 20·log(2π·Leakage / K_{PD}) + 20·log(N) + rolloff(f_{PD})
	Integer Spur	Total Spur = 10·log($10^{PulseSpur/10}$ + $10^{LeakageSpur/10}$)
Fractional	Fractional Spur	FractionalSpur = InBandSpur + rolloff(Offset)
	Xtalk Spur	XtalkSpur = BaseXtalkSpur - 20·log(Offset/10kHz) - 20·log(| (1+G(2π·j·Offset) / N) |)
	Total Fractional Spur	Total Spur = 10·log($10^{FractionalSpur/10}$ + $10^{XtalkSpur/10}$)

As for spurs, integer PLL spurs are multiplied by the N counter value, where fractional N PLL spurs are not. This implies that fractional N PLLs spurs theoretically would perform best relative to integer PLL spurs at higher VCO frequencies. Using integer spurs models in [1] for the LMX2306 (K_{PD} = 1 mA, BasePulseSpur = -313 dBc), traditional spur models for the LMX2364 (InBandSpur = -18 dBc), and delta sigma models for the LMX2485 (InBandSpur = -55 dBc), Figure 28 shows a comparison based on a variable channel spacing and fixed 10 kHz loop bandwidth.

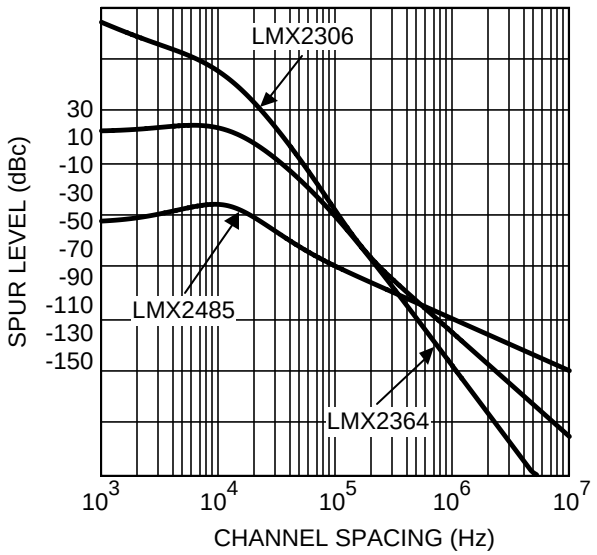

Figure 28. Comparing Integer and Fractional PLLs

6 Conclusion

Fractional N PLLs allow better resolution and performance by allowing the N counter to support fractional values. By supporting fractional values, the overall N counter can be made lower and the phase noise substantially reduced. Fractional spurs are created and there is a lot to say about how these fractional spurs are reduced. In the traditional PLL, this is corrected with analog compensation. Although analog compensation may be easier to understand and predict, the spurs are much higher than those with digital delta-sigma compensation. Fractional N PLLs provide the most benefits for applications that have low channel spacing and higher output frequencies, although they provide a significant benefit to almost every application. In fact, it is advantageous to use a fractional part at higher frequencies and then divide this down, since the spurs will be the same offset, but reduced in amplitude, and the fractional spurs are independent of VCO frequency.

7 References

1. Banerjee, Dean “PLL Performance, Simulation, and Design, 4th Ed” Dogear Publishing 2006.
2. Crawford, James “Advanced Phaselocked Techniques” Artech House. 2008
3. Howard, Andy “Delta Sigma Modulator PLLs with Dithered Divide-Ratio”. Agilent Application Note available at *http://eesof.tm.agilent.com/pdf/HF_TechNote_110201.pdf*
4. Perrot, H.H, M.D.Trott, G.G.Sodini “A Modeling Approach for a D-S Fractional-N Frequency Synthesizers Allowing Straightforward Noise Analysis” IEEE Journal of Solid_State Circuits, Vol 37, No. 8, August 2002
5. Seuss, Dr. "The Cat in the Hat". Dr. Seuss Enterprises 1985. Also 1971 DFE film production based on this book describing the "Calculatus Eliminatus" technique.

Appendix A Fundamental Z Transform Properties

The Z transform can be thought of as a discrete version of a Fourier transform that converts a time domain signal to the frequency domain. It has several applications, such as solving difference equations and finding the frequency content of discrete time-domain signals. In the context of delta-sigma PLLs, it is useful in order to find the frequency content of the output of the delta sigma modulator. In this context, the time step is the period of the phase detector frequency, $1 / f_{PD}$. The Z transform is defined as:

$$F(z) = \sum_{k=0}^{\infty} f(n) \cdot z^{-k} \tag{24}$$

There are a few properties of the Z transform that are useful to know as shown in Table 7.

Table 7. Common Z Transform Pairs

Time Domain	Z Domain	Comments
f (n-1)	$z^{-1} \cdot f(z)$	This is a 1 clock cycle delay
$\sum f(n)$	$1 / (1 - z^{-1})$	This is a summation which occurs in the accumulator of a fractional N PLL

The first property can be easily derived by multiplying both sides for the Z transform equation by a factor of z^{-1}. It is very useful to recognize this property that multiplying by a factor of z^{-1} is the same as a one clock cycle delay. The second property is useful because this applies to any summation, which occurs in the accumulator of a PLL. A summation can be viewed as adding the previous sum to the current output as shown in Figure 29.

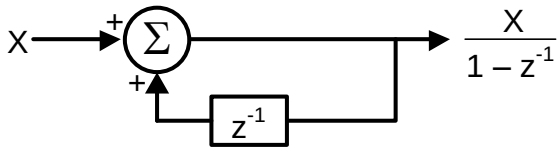

Figure 29. Summation in the Z Domain

There are situations where it is useful to know the spectral density of something with a digital output. For this, it is useful to develop a link between the discrete Z domain and the continuous frequency domain. Recall the Fourier transform:

$$F(\omega) = \int_{-\infty}^{\infty} f(t) \cdot e^{-j\omega t} \cdot dt \tag{25}$$

The following substitution can be made to convert from the Z domain to the frequency domain:

$$e^{j\omega T} = e^{2\pi \cdot j \cdot \left(\frac{f}{f_{PD}}\right)} \Rightarrow z \tag{26}$$

Appendix B Derivation of Delta Sigma Noise Characteristics

From Figure 8, you can see that the output of an n^{th} order modulator would be:

$$Y(z) = \frac{Fnum}{Fden} + (1 - z^{-1})^n \times Q_n(z) \tag{27}$$

However, as discussed in good detail in [4] this result is incomplete because it does not account for the digital sampling action of the phase detector and the fact that the N counter value is not constant, but rather being dithered around. In order to account for these effects, it is necessary to introduce the term h(z):

$$h(z) = 2\pi \frac{z^{-1}}{1 - z^{-1}} \cdot \frac{1}{f_{PD}} \tag{28}$$

Accounting for this term, the modulator noise becomes:

$$Y(z) = \frac{Fnum}{Fden} + h(z) \cdot (1 - z^{-1})^n \cdot Q_n(z) \tag{29}$$

To get the output spectrum of the delta sigma modulator, it is necessary to transform from the Z domain to the frequency domain, use the following substitution (Appendix A):

$$z = e^{s \cdot T} = e^{2\pi \cdot j \cdot f \cdot T} = e^{2\pi \cdot j \cdot \left(f / f_{PD}\right)} \tag{30}$$

As an intermediate step, the following derivation is useful:

$$\begin{aligned} &\left|1 - z^{-1}\right| = \left|1 - e^{j \cdot x}\right| \\ &= \left|1 - \cos(x) - j \cdot \sin(x)\right| = (1 - \cos(x))^2 + \sin^2(x) \\ &= 1 - 2 \cdot \cos(x) + \cos^2(x) + \sin^2(x) = 2 \cdot (1 - \cos(x)) \\ &= 4 \cdot \sin^2(x/2) \end{aligned} \tag{31}$$

Applying the transform and identities yields [4]:

$$\left|Y_{Noise}(f)\right| = \left(2 \cdot \sin\left(\frac{\pi f}{f_{PD}}\right)\right)^{2 \cdot (n-1)} \cdot \left|\frac{Q_n(s)}{f_{PD}}\right| \tag{32}$$

The above formula applies to both phase noise and spurs. Q_n (z) is simply the output of the n^{th} quantizer minus its input. Because the output of the quantizer can be zero or one, this is bounded between (and including) zero and one. The spectral density of the quantization noise, Q_n (s), can change based on the fractional word. However, if the fraction is large and the modulator order is 3 or 4, then it is a fair assumption to assume that this is a uniformly distributed random variable between zero and one [4]. Under this assumption, the spectral density of the quantizer output can be modeled as a uniformly distributed random variable between zero and one, which has a resulting spectral density of:

$$Q_n(s) = 1/12 \tag{33}$$

For noise, the appropriate function is [4]:

$$\left|Y_{Noise}(f)\right|^2 = (2\pi)^2 \cdot \left(2 \cdot \sin\left(\frac{\pi \cdot f}{f_{PD}}\right)\right)^{2 \cdot (n-1)} \cdot \left(\frac{1 \cdot Hz}{12 \cdot f_{PD}}\right) \tag{34}$$

In Figure 9, note there is a point at which all the modulators theoretically have the same performance. This can easily be found by setting:

$$2 \cdot \sin\left(\frac{\pi \cdot f}{f_{PD}}\right) = \pm 1 \tag{35}$$

This occurs at:

$$f = \frac{f_{PD}}{6} + k \cdot f_{PD}, k = 0,1,2,... \tag{36}$$

Of most interest is the case where k=0. Indeed there are theoretically higher order occurrences, but for these, other noise sources can mask this and the delta sigma noise tends to be better filtered out for these frequencies. The most interesting occurrence is therefore:

$$f = \frac{f_{PD}}{6} \tag{37}$$

Another frequency of interest is where the unshaped noise peaks in value. This can be found by setting:

$$\sin\left(\frac{\pi \cdot f}{f_{PD}}\right) = \pm 1 \tag{38}$$

This has a solution of:

$$f = \frac{f_{pd}}{2} \cdot (2 \cdot k + 1), k = 0,1,2,... \tag{39}$$

The magnitude of the first phase noise peak can be found by substituting this frequency:

$$\begin{aligned} PLLnoise_{fractional}(f_{PD}/2) &= 10 \cdot \log\left[(2\pi)^2 \cdot \left(2 \cdot \sin\left(\frac{\pi}{2}\right)\right)^{2 \cdot (order-1)} \cdot \left(\frac{1 \cdot Hz}{12 \cdot f_{PD}}\right)\right] \\ &= 20 \cdot \log(2\pi) - 10 \cdot \log(12) + 20 \cdot \log(2) \cdot (order-1) - 10 \cdot \log\left(\frac{1 \cdot Hz}{f_{PD}}\right) \\ &\approx 6 \cdot order - 10 \cdot \log\left(\frac{f_{PD}}{1 \cdot Hz}\right) - 0.8 \end{aligned} \tag{40}$$

One final property of the delta sigma modulator noise is the slope for lower frequencies at offsets much less than $f_{PD}/2$. At these lower frequencies, sin (x) can be approximated by x and the slope can therefore be approximated as:

$$\begin{aligned} &d/df\left[(2\pi)^2 \cdot \left(2 \cdot \sin\left(\frac{\pi \cdot f}{f_{PD}}\right)\right)^{2 \cdot n} \cdot \left(\frac{1 \cdot Hz}{12 \cdot f_{PD}}\right)\right] \\ &\approx k \cdot \left(\frac{f}{f_{PD}}\right)^{2 \cdot (n-1)} \\ &\Rightarrow 20 \cdot (n-1) \text{ dB/decade} \end{aligned} \tag{41}$$

Appendix C Setup Conditions

This appendix discusses setup conditions that were used. Table 8 is a list of the equipment that was used. Automated test scripts were used for the spur measurements. To measure spurs at such low levels, the span of the spectrum analyzer was a set to 10 Hz and the reported spur levels was the difference between the spur power and the carrier power. When phase noise was measured, special care was taken to ensure that the phase noise of the signal source was far below the noise being measured at the VCO output.

Table 8. List of Equipment

Equipment	Model	Comments
Power Supply	HP6623A	A LC filter with a pole of 60 Hz was placed on this output to ensure that the power supply was clean.
Signal Source	Back of E4445A	This was used when the reference frequency was 10 MHz
	SML03	This was only used when the reference frequency was different than 10 MHz
Spectrum Analyzer	E4445A	This was used for spurs
Phase Noise Analyzer	E5052A	This was used for phase noise.

All these measurements were made with evaluation boards. For the case of the LMX2485 wide loop filter, the components on the board were modified to increase the loop bandwidth so that it would be easier to see the performance of the delta sigma modulator. In the other cases, the default loop filter that came with the board was used. One thing that was done on the LMX2364 and LMX2485 standard loop filters was that the phase detector frequency was decreased and the charge pump gain was raised in the same proportion. This preserves the same loop filter characteristics but makes it easier to measure the delta sigma noise and spurs.

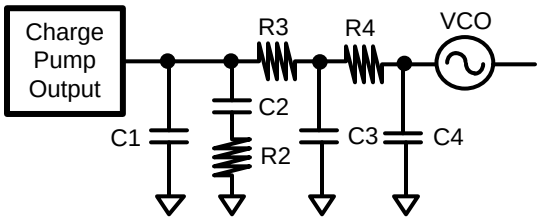

Figure 30. Loop Filter Setup

Attribute	LMX2364	LMX2485	LMX2485	LMX2485E
Setup	Standard Loop Filter	Wide Loop Filter	Standard Loop Filter	Standard Loop Filter
K_{PD} (µA)	1000	1520 (16X)	1520 (16X)	760 (8X)
K_{VCO} (MHz/V)	45	60	60	2.5
f_{PD} (MHz)	2	10	10	1
f_{VCO} (MHz)	1960	2440	2440	50
BW (kHz)	5.1	237.9	11.3	4.5
Phase Margin (degrees)	47.3	35	39.4	48
C1 (nF)	18	0.1	15	6.8
C2 (nF)	100	0.68	150	100
C3 (nF)	0	0	0.82	1.8
C4 (nF)	0	0	0.56	0
VCOcap (nF)	22	22	22	0.82
R2 (kΩ)	0.82	6.8	0.22	1

Attribute	LMX2364	LMX2485	LMX2485	LMX2485E
R3 (kΩ)	0	0	1.5	2.2
R4 (kΩ)	0	0	2.7	0

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265