ABSTRACT

The purpose of this applications report is to present phase noise and jitter measurements representing the clock outputs of the LMK04000 family of Precision Clock Conditioners, when paired with various voltage controlled oscillators (VCXOs). The intent is to illustrate the relationship between clock output phase noise and VCXO phase noise.

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<td>8</td>
</tr>
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<td>Crystek CVHD-950-122.88MHz</td>
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</tr>
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<td>5</td>
<td>Crystek CVHD-950-80</td>
<td>14</td>
</tr>
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<td>6</td>
<td>Crystek CVPD-920-61.44</td>
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<td>Epson Toyocom VG-4501, 61.44 MHz</td>
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<td>8</td>
<td>Epson-Toyocom VG-4231, 19.44 MHz</td>
<td>23</td>
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<td>9</td>
<td>Epson-Toyocom TCO-2111-AA 245.76</td>
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<td>10</td>
<td>Suntsu SVD Series, 54 MHz</td>
<td>29</td>
</tr>
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<td>11</td>
<td>Suntsu SVD Series, 61.44 MHz</td>
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<td>12</td>
<td>Suntsu SVD Series, 30.72 MHz</td>
<td>35</td>
</tr>
<tr>
<td>13</td>
<td>Vectron Model 5310, 155.52 MHz</td>
<td>38</td>
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<tr>
<td>14</td>
<td>Vectron Model 5310, 134.4 MHz</td>
<td>41</td>
</tr>
</tbody>
</table>
1 Introduction

The purpose of this applications report is to present phase noise and jitter measurements representing the clock outputs of the LMK04000 family of Precision Clock Conditioners, when paired with various voltage controlled oscillators (VCXOs). The intent is to illustrate the relationship between clock output phase noise and VCXO phase noise. The LMK04000 family provides superior jitter cleaning capability by employing a dual, cascaded phase locked loop (PLL) architecture. A generic example of a dual PLL architecture is shown in Figure 1. The figure also shows a clock distribution section following the VCO output.

The first PLL utilizes a narrow loop bandwidth to frequency lock the external VCXO to the incoming reference clock. The narrow loop bandwidth rejects most of the phase noise associated with the reference clock, allowing the VCXO phase noise to dominate. The frequency-locked VCXO is injected as the reference clock to the second PLL that employs a wider loop bandwidth to lock an internal VCO. This wider loop bandwidth means the VCO is both phase and frequency-locked to the VCXO, thus the VCXO phase noise dominates. For phase noise offsets higher than the loop bandwidth, the internal VCO phase noise and the output dividers and drivers will determine the output phase noise. This can be illustrated more explicitly by considering the total phase noise at the output of the synthesizer. Because the synthesizer noise determines the clock output noise, it is sufficient to only look at the synthesizer noise. The following equation shows that the total noise is the weighted sum of reference clock noise, PLL noise and VCO noise:

\[ S_{\text{TOTAL}}(f) = S_{\text{REF}}(f) \cdot G_{\text{REF}}^2 |H(f)|^2 + S_{\text{PLL}}(f) \cdot G_{\text{PLL}}^2 |H(f)|^2 + S_{\text{VCO}}(f) \cdot |1 - H(f)|^2 \]

The weighting function H(f) is the lowpass closed loop transfer function, formed by parameters such as the charge pump gain, loop filter response, VCO gain, and feedback path (N) counter. This equation represents the noise model at the output of each of the PLL stages shown in Figure 1. The gains associated with the reference clock noise (G_{\text{REF}}) and PLL noise (G_{\text{PLL}}) are also functions of specific loop parameters. Though the explicit expressions for these gains and closed loop response H(f) are not derived here, the relevance of this equation can still be seen. In general, the synthesizer parameters that comprise H(f) and the gain values represented in the equation are under the control of the designer and should be chosen such that the overall noise at the synthesizer output (S_{\text{TOTAL}}(f)) is minimized. In this case, minimization means achieving the smallest integrated noise. When the noise equation is applied to PLL2, S_{\text{REF}}(f) represents the VCXO noise. In the case of the LMK04000 family, S_{\text{PLL}}(f) and S_{\text{VCO}}(f) are “fixed” by the device characteristics, but S_{\text{REF}}(f) is dependent on the VCXO chosen by the designer. **Therefore it is important to select a VCXO that supports the phase noise and jitter requirements of the target application.**

The inclusion of a particular VCXO model or manufacturer in this report does not constitute an endorsement by National Semiconductor. The purpose of the data contained in this report is to offer the reader some insight on the direct relationship between the phase noise and jitter performance of the total clocking solution and VCXO characteristics. Though no VCXO cost data is presented here, there is a significant correlation between VCXO cost and performance. The LMK04000 family is targeted toward applications that require jitter cleaning, frequency synthesis and multiple clock distribution. While the LMK04000 family offers the industry’s best performance in these categories, not all applications require the same level of performance. Hence, the LMK04000 family offers designers the capability to tailor the cost and performance of their clocking solutions by selecting the VCXO that best meets the overall needs of the application. This objective is further enhanced through the built-in features of the LMK04000 family that support the use of discretely implemented external crystal oscillators as well as off-the-shelf VCXO modules. The use of external crystal oscillators is addressed in a separate applications report.
2 LMK04000 Family Description

Figure 2 shows a detailed block diagram of the LMK04000 Precision Clock Conditioner family. The redundant reference clock inputs (CLKin0, CLKin1) for PLL1 support frequencies up to 400 MHz. The reference clocks may be either single-ended or differential, and an auto-switching mode can be enabled for fail-safe operation. The maximum allowable frequency of the VCXO driving the OSCin port is 250 MHz. The signal at the OSCin port is fed back to the PLL1 phase comparator and is also injected to PLL2 as a phase and frequency reference. Though not shown in the diagram, there is internal support for a discretely implemented VCXO using an external crystal resonator. An optional frequency doubler path for the reference input to the PLL2 phase comparator allows the phase comparison frequency to be increased, thereby lowering the in-band noise of PLL2. An internal VCO is integrated with PLL2, along with optional internal loop filter components that support 3rd and 4th order poles for the PLL2 loop filter. The VCO output is buffered and made available at the Fout pin, and is also routed through a VCO divider to the internal clock distribution bus. The clock distribution section buffers and divides the bus clock through separately configured channels. Each channel features a divider, delay block and output buffer. The mixture of signal formats at the clock outputs is fixed according to the specific device part number.

Table 1 shows the currently released devices of the LMK04000 family. As Table 1 shows, two VCO frequency bands are offered along with two configurations of clock output formats. The device used for the measurements reported here was the LMK04031.

<table>
<thead>
<tr>
<th>NSID</th>
<th>PROCESS</th>
<th>2VPECL/LVPECL OUTPUTS</th>
<th>LVDS OUTPUTS</th>
<th>LVCMOS OUTPUTS</th>
<th>VCO FREQUENCY RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMK04011BISQ</td>
<td>BiCMOS</td>
<td>5</td>
<td></td>
<td></td>
<td>1430 to 1570 MHz</td>
</tr>
<tr>
<td>LMK04031BISQ</td>
<td>BiCMOS</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1430 to 1570 MHz</td>
</tr>
<tr>
<td>LMK04033BISQ</td>
<td>BiCMOS</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1840 to 2160 MHz</td>
</tr>
</tbody>
</table>
3 LMK04000 Clock Output Phase Noise and Jitter

Various VCXOs were paired and tested with the LMK04031. The phase noise and jitter was measured at the clock outputs using an Agilent E5052A Signal Source Analyzer. The loop filters for PLL1 and PLL2 were fixed for all measurements. They are shown in Figure 3. The closed loop bandwidth was adjusted either by the charge pump current or by adjusting the phase comparison frequency. The VCXOs cover various frequencies, so the measured clock frequencies vary, but are in the range of 122.88 MHz to 129 MHz. Figure 4 illustrates the test setup for the measurements.
Table 2 summarizes the RMS jitter measured at the Fout pin (buffered VCO output) and at clock output pins for LVDS, LVCMOS and LVPECL clock types. For all jitter measurements at the LMK04031 outputs, the integration bandwidth is 100 Hz to 20 MHz. The VCXO RMS jitter values listed in Table 2 are based upon a measurement bandwidth of 100 Hz to 200 kHz. 200 kHz was chosen as the upper limit because in most cases the loop bandwidth employed for PLL2 will not exceed 200 kHz, and so the VCXO contribution to total jitter beyond a 200 kHz offset is insignificant. Furthermore, because the measurement bandwidth is consistent for all of the VCXOs represented in this note, one can make useful comparisons between them when determining suitability for a particular application.
Table 2. Summary of RMS Jitter Measurements

<table>
<thead>
<tr>
<th>VCXO MODEL</th>
<th>FREQ (MHz)</th>
<th>RMS JITTER (fs)</th>
<th>Fout RMS JITTER (fs)</th>
<th>CLOCK OUTPUT FREQ (MHz)</th>
<th>LVDS RMS JITTER (fs)</th>
<th>LVPECL RMS JITTER (fs)</th>
<th>LVCMOS RMS JITTER (fs)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(1)</td>
<td>(2)</td>
<td></td>
<td>(3)</td>
<td>(4)</td>
<td>(5)</td>
<td>(6)</td>
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<tr>
<td>pp. 6-9</td>
<td>CTS Model 357</td>
<td>61.44</td>
<td>311</td>
<td>1474.56</td>
<td>390.3</td>
<td>122.88</td>
<td>398.6</td>
</tr>
<tr>
<td>pp. 10-14</td>
<td>Crystek CVHD-950</td>
<td>122.88</td>
<td>32</td>
<td>1474.56</td>
<td>127.8</td>
<td>122.88</td>
<td>160.7</td>
</tr>
<tr>
<td>pp. 15-19</td>
<td>Crystek CVHD-950</td>
<td>80</td>
<td>71</td>
<td>1520</td>
<td>165.5</td>
<td>126.6666</td>
<td>193.1</td>
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<tr>
<td>pp. 20-24</td>
<td>Crystek CVPD-920</td>
<td>61.44</td>
<td>285</td>
<td>1474.56</td>
<td>337.5</td>
<td>122.88</td>
<td>339.9</td>
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<tr>
<td>pp. 25-29</td>
<td>Epson Toyocom VG-4501</td>
<td>61.44</td>
<td>143</td>
<td>1474.56</td>
<td>230.2</td>
<td>122.88</td>
<td>250.4</td>
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<tr>
<td>pp. 30-34</td>
<td>Epson Toyocom VG-4231</td>
<td>19.44</td>
<td>383</td>
<td>1516.32</td>
<td>609.8</td>
<td>126.36</td>
<td>635.7</td>
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<td>pp. 35-39</td>
<td>Epson Toyocom TCO-2111-AA</td>
<td>245.76</td>
<td>74</td>
<td>1474.56</td>
<td>148.1</td>
<td>122.88</td>
<td>183.3</td>
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<tr>
<td>pp. 40-44</td>
<td>Suntsu SVD series</td>
<td>54</td>
<td>336</td>
<td>1512</td>
<td>486.3</td>
<td>126</td>
<td>497.2</td>
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<tr>
<td>pp. 45-49</td>
<td>Suntsu SVD series</td>
<td>61.44</td>
<td>295</td>
<td>1474.56</td>
<td>489</td>
<td>122.88</td>
<td>495.9</td>
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<tr>
<td>pp. 50-54</td>
<td>Suntsu SVD series</td>
<td>30.72</td>
<td>655</td>
<td>1474.56</td>
<td>842.5</td>
<td>122.88</td>
<td>860.2</td>
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<tr>
<td>pp. 55-59</td>
<td>Vectron 5310</td>
<td>155.52</td>
<td>110</td>
<td>1555.2</td>
<td>155.7</td>
<td>129.6</td>
<td>179.5</td>
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<td>134.40</td>
<td>82</td>
<td>1523.2</td>
<td>155.5</td>
<td>126.9333</td>
<td>181.8</td>
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</table>

(1) Integration bandwidth for VCXO jitter is 100 Hz to 200 kHz
(2) Jitter integration bandwidth for clock measurements is 100 Hz to 20 MHz

The remainder of this application report presents phase noise plots captured using the E5052A. Each VCXO section begins with a table that lists the reference clock frequency, PLL1 phase comparison frequency and closed loop bandwidth, and the PLL2 phase comparison frequency and closed loop bandwidth. Each VCXO section also contains a plot of the open loop phase noise of the VCXO, and closed loop phase noise plots of the LMK04031 outputs.

3.1 CTS Model 357 VCXO

Table 3. CTS Model 357, 61.44 MHz

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>F_{comp1} (MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>F_{comp2} (MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30.72</td>
<td>1.024</td>
<td>30</td>
<td>30.72</td>
<td>95.4</td>
</tr>
</tbody>
</table>
Figure 5. CTS Model 357 VCXO Open Loop Phase Noise, 61.44 MHz

Figure 6. LMK04031 Fout Phase Noise, CTS model 357 VCXO
Figure 7. LMK04031 LVDS Phase Noise, CTS model 357 VCXO

Figure 8. LMK04031 LVCMOS Phase Noise, CTS model 357 VCXO
3.2 **Crystek CVHD-950-122.88 MHz VCXO**

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>$F_{\text{comp1}}$ (MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>$F_{\text{comp2}}$ (MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>122.88</td>
<td>1.024</td>
<td>20</td>
<td>61.44</td>
<td>189.7</td>
</tr>
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</table>

Figure 9. LMK04031 LVPECL Phase Noise, CTS model 357 VCXO
Figure 10. Crystek CVHD-950-122.88 VCXO Open Loop Phase Noise

Figure 11. LMK04031 Fout Phase Noise, Crystek CVHD-950-122.88 VCXO
Figure 12. LMK04031 LVDS Phase Noise, Crystek CVHD-950-122.88 VCXO

Figure 13. LMK04031 LVCMOS Phase Noise, Crystek CVHD-950-122.88 VCXO
3.3 **Crystek CVHD-950-80 VCXO**

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>$F_{comp1}$ (MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>$F_{comp2}$ (MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
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<tbody>
<tr>
<td>40</td>
<td>1.0</td>
<td>20</td>
<td>40</td>
<td>120.3</td>
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Figure 15. Crystek CVHD-950-80 VCXO Open Loop Phase Noise

Figure 16. LMK04031 Fout Phase Noise, Crystek CVHD-950-80 VCXO
Figure 17. LMK04031 LVDS Phase Noise, Crystek CVHD-950-80 VCXO

Figure 18. LMK04031 LVCMOS Phase Noise, Crystek CVHD-950-80 VCXO
3.4 Crystek CVPD-920-61.44 VCXO

Table 6. Crystek CVPD-920-61.44

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>$F_{\text{comp1}}$(MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>$F_{\text{comp2}}$(MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30.72</td>
<td>1.024</td>
<td>20</td>
<td>30.72</td>
<td>95.4</td>
</tr>
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</table>
Figure 20. Crystek CVPD-920-61.44 VCXO Open Loop Phase Noise

Figure 21. LMK04031 Fout Phase Noise, Crystek CVPD-920-61.44 VCXO
Figure 22. LMK04031 LVDS Phase Noise, Crystek CVPD-920-61.44 VCXO

Figure 23. LMK04031 LVCMOS Phase Noise, Crystek CVPD-920-61.44 VCXO
3.5 Epson Toyocom VG-4501 VCXO

Table 7. Epson Toyocom VG-4501, 61.44 MHz

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>$F_{comp1}$ (MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>$F_{comp2}$ (MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
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<tbody>
<tr>
<td>30.72</td>
<td>1.024</td>
<td>20</td>
<td>30.72</td>
<td>95.4</td>
</tr>
</tbody>
</table>

Figure 24. LMK04031 LVPECL Phase Noise, Crystek CVPD-920-61.44 VCXO
Figure 25. Epson Toyocom VG-4501 VCXO, 61.44 MHz, Open Loop Phase Noise

Figure 26. LMK04031 Fout Phase Noise, Epson Toyocom VG-4501 VCXO
Figure 27. LMK04031 LVDS Phase Noise, Epson Toyocom VG-4501 VCXO

Figure 28. LMK04031 LVCMOS Phase Noise, Epson Toyocom VG-4501 VCXO
3.6 Epson-Toyocom VG-4231 VCXO

Table 8. Epson-Toyocom VG-4231, 19.44 MHz

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>( F_{\text{comp}} ) (MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>( F_{\text{comp}} ) (MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>19.44</td>
<td>1.08</td>
<td>20</td>
<td>19.44</td>
<td>59</td>
</tr>
</tbody>
</table>
Figure 30. Epson Toyocom VG-4231 VCXO, 19.44 MHz, Open Loop Phase Noise

Figure 31. LMK04031 Fout Phase Noise, Epson Toyocom VG-4231 VCXO
Figure 32. LMK04031 LVDS Phase Noise, Epson Toyocom VG-4231 VCXO

Figure 33. LMK04031 LVCMOS Phase Noise, Epson Toyocom VG-4231 VCXO
3.7 Epson-Toyocom TCO-2111-AA VCXO

Table 9. Epson-Toyocom TCO-2111-AA 245.76

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>$F_{comp1}$(MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>$F_{comp2}$(MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>122.88</td>
<td>1.024</td>
<td>20</td>
<td>61.44</td>
<td>189.7</td>
</tr>
</tbody>
</table>
Figure 35. Epson Toyocom TCO-2111-AA VCXO, 245.76 MHz, Open Loop Phase Noise

Figure 36. LMK04031 Fout Phase Noise, Epson Toyocom TCO-2111-AA VCXO
Figure 37. LMK04031 LVDS Phase Noise, Epson Toyocom TCO-2111-AA VCXO

Figure 38. LMK04031 LVCMOS Phase Noise, Epson Toyocom TCO-2111-AA VCXO
Figure 39. LMK04031 LVPECL Phase Noise, Epson Toyocom TCO-2111-AA VCXO

3.8 Suntsu SVD Series VCXO, 54 MHz

Table 10. Suntsu SVD Series, 54 MHz

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>F_{comp1}(MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>F_{comp2}(MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
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<tbody>
<tr>
<td>27</td>
<td>1.0</td>
<td>30</td>
<td>27</td>
<td>81.9</td>
</tr>
</tbody>
</table>
Figure 40. Suntsu SVD Series VCXO, 54 MHz, Open Loop Phase Noise

Figure 41. LMK04031 Fout Phase Noise, Suntsu SVD Series VCXO, 54 MHz
Figure 42. LMK04031 LVDS Phase Noise, Suntsu SVD Series VCXO, 54 MHz

Figure 43. LMK04031 LVCMOS Phase Noise, Suntsu SVD Series VCXO, 54 MHz
3.9 **Sunatsu SVD Series VCXO, 61.44 MHz**

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>$F_{\text{comp1}}$ (MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>$F_{\text{comp2}}$ (MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30.72</td>
<td>1.024</td>
<td>30</td>
<td>30.72</td>
<td>95.4</td>
</tr>
</tbody>
</table>
Figure 45. Suntsu SVD Series VCXO, 61.44 MHz, Open Loop Phase Noise

Figure 46. LMK04031 Fout Phase Noise, Suntsu SVD Series VCXO, 61.44 MHz
Figure 47. LMK04031 LVDS Phase Noise, Suntsu SVD Series VCXO, 61.44 MHz

Figure 48. LMK04031 LVCMOS Phase Noise, Suntsu SVD Series VCXO, 61.44 MHz
3.10 Suntsu SVD Series VCXO, 30.72 MHz

Table 12. Suntsu SVD Series, 30.72 MHz

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>F_{comp1}(MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>F_{comp2}(MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30.72</td>
<td>1.024</td>
<td>20</td>
<td>30.72</td>
<td>95.4</td>
</tr>
</tbody>
</table>
Figure 50. Suntsu SVD Series VCXO, 30.72 MHz, Open Loop Phase Noise

Figure 51. LMK04031 Fout Phase Noise, Suntsu SVD Series VCXO, 30.72 MHz
Figure 52. LMK04031 LVCMOS Phase Noise, Suntsu SVD Series VCXO, 30.72 MHz

Figure 53. LMK04031 LVPECL Phase Noise, Suntsu SVD Series VCXO, 30.72 MHz
Figure 54. LMK04031 LVDS Phase Noise, Suntsu SVD Series VCXO, 30.72 MHz

3.11 Vectron Model 5310 VCXO, 155.52 MHz

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>$F_{\text{comp1}}$ (MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>$F_{\text{comp2}}$ (MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>38.88</td>
<td>1.08</td>
<td>30</td>
<td>51.84</td>
<td>152</td>
</tr>
</tbody>
</table>
Figure 55. Vectron Model 5310 VCXO, 155.52 MHz, Open Loop Phase Noise

Figure 56. LMK04031 Fout Phase Noise, Vectron Model 5310 VCXO, 155.52 MHz
Figure 57. LMK04031 LVDS Phase Noise, Vectron Model 5310 VCXO, 155.52 MHz

Figure 58. LMK04031 LVCMOS Phase Noise, Vectron Model 5310 VCXO, 155.52 MHz
Figure 59. LMK04031 LVPECL Phase Noise, Vectron Model 5310 VCXO, 155.52 MHz

3.12 Vectron Model 5310 VCXO, 134.4 MHz

Table 14. Vectron Model 5310, 134.4 MHz

<table>
<thead>
<tr>
<th>Reference Clock (MHz)</th>
<th>$F_{\text{comp1}}$ (MHz)</th>
<th>PLL1 Loop BW (Hz)</th>
<th>$F_{\text{comp2}}$ (MHz)</th>
<th>PLL2 Loop BW (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>33.6</td>
<td>1.05</td>
<td>30</td>
<td>44.8</td>
<td>134.3</td>
</tr>
</tbody>
</table>
Figure 60. Vectron Model 5310 VCXO, 134.4 MHz, Open Loop Phase Noise

Figure 61. LMK04031 Fout Phase Noise, Vectron Model 5310 VCXO, 134.4 MHz
Figure 62. LMK04031 LVDS Phase Noise, Vectron Model 5310 VCXO, 134.4 MHz

Figure 63. LMK04031 LVCMOS Phase Noise, Vectron Model 5310 VCXO, 134.4 MHz
Figure 64. LMK04031 LVPECL Phase Noise, Vectron Model 5310 VCXO, 134.4 MHz
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