ADC08D1000,ADC08D1500,ADC08D500, ADC12DL080,LMH6502,LMH6550

LIDAR System Design for Automotive/Industrial/Military Applications

Literature Number: SNAA123

SIGNAL PATH designer℠

Tips, tricks, and techniques from the analog signal-path experts

No. 105

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LIDAR System Design for Automotive/ Industrial/Military Applications

— By Paul McCormack, Sr. Product Application Engineer

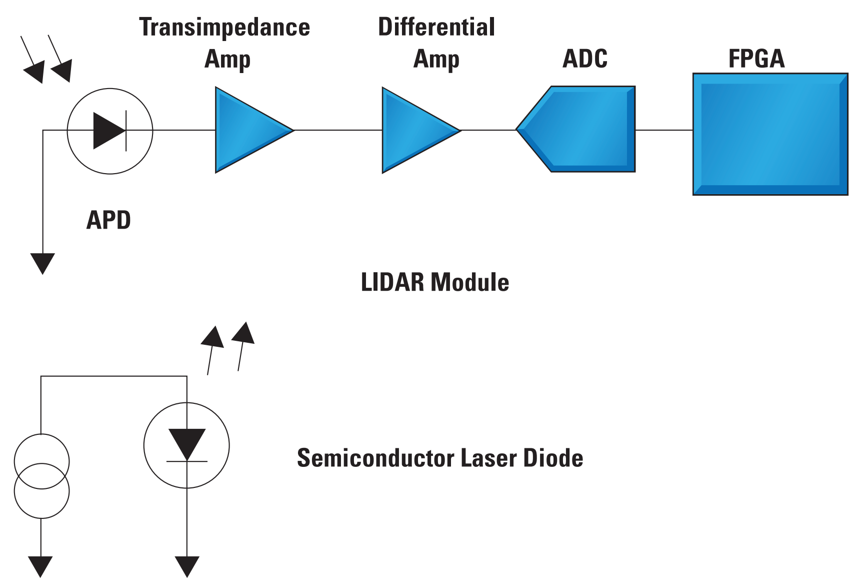

Figure 1. LIDAR block diagram

LIDAR (LIght Detection And Ranging) systems using the same principle as RADAR are developed for a wide range of locating, ranging, and profiling applications. Such a system consists of a laser capable of transmitting light (pulsed or continuous) over the required range of interest, and a high-speed, low-noise receiver for reflected signal analysis. Transmitted light interacts with and is changed by the target. A percentage of this light is reflected / scattered back to the receiver according to the reflectivity of the target. Changes in the properties of the transmitted signal enable some properties of the target to be determined. In the most common application, the Time Of Flight (TOF), is used to determine range.

As analog technology improves in performance and availability, LIDAR technology continues to find its way into more and more exciting

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Basestation Designs

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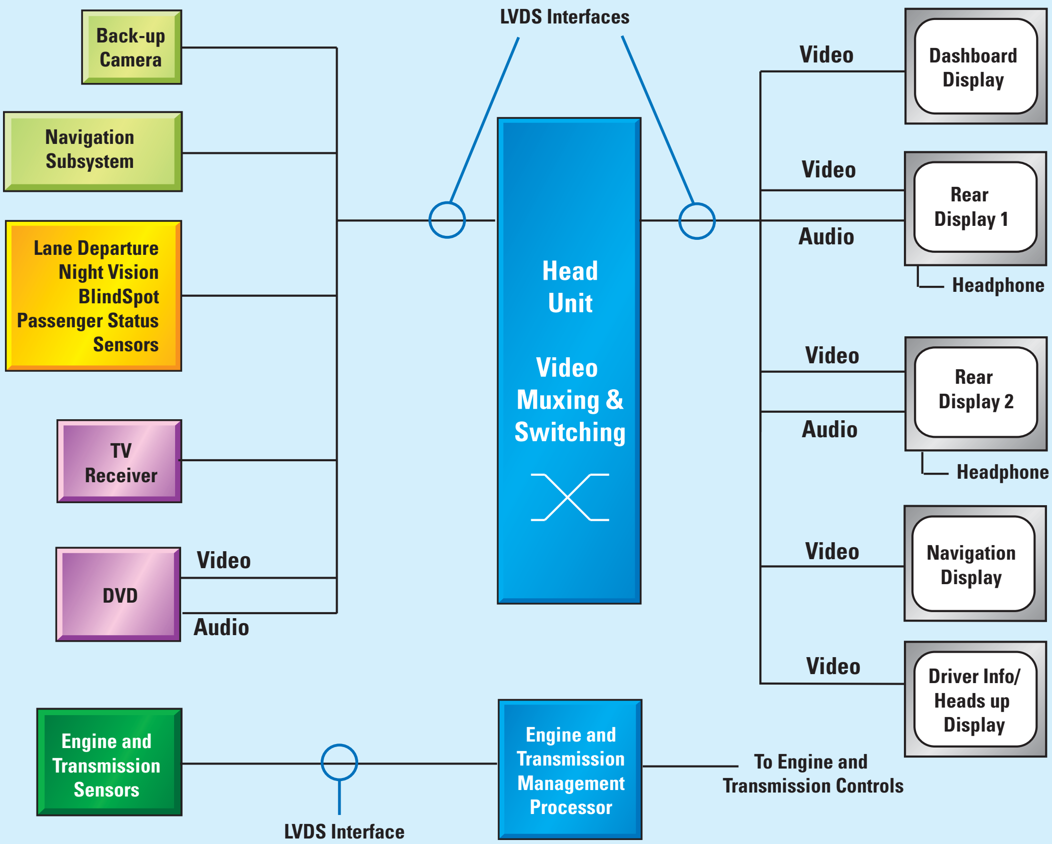
LVDS Solutions for Automotive Applications

Automotive Camera, Sensor, and Display Subsystems



Recommended LVDS Interfaces for Automotive Applications

Product ID	Description	Features
DS90LV011A	Single, 400 Mbps, LVDS driver	400 Mbps Throughput, tiny package, 125°C version available
DS90LT012A	Single, 400 Mbps, LVDS receiver	400 Mbps Throughput, input termination, tiny package, 125°C version available
DS90LV027A	Dual, 400 Mbps, LVDS driver	400 Mbps Throughput per channel, tiny package, 125°C version available
DS90LV028A	Dual, 400 Mbps, LVDS receiver	400 Mbps Throughput per channel, tiny package, 125°C version available
DS90LV004	4 Channel, 1.5 Gbps, LVDS repeater	1.5 Gbps per Channel, output pre-emphasis, integrated terminations, 15 kV ESD protection
DS90LV804	4 Channel, 800 Mbps, LVDS repeater	800 Mbps per Channel, integrated terminations, 15 kV ESD protection
DS90CP22	2x2, 800 Mbps, LVDS Crosspoint switch	800 Mbps per Channel, low power, Jitter and Skew, small 16-lead TSSOP and SOIC package, configurable as switch, splitter, mux, or buffer
DS92LV1021A DS92LV1212A	10-Bit, 16 to 80 MHz Serializer and Deserializer	Embedded clock, single differential pair, 125°C version available
DS90C241/124	5 to 35 MHz, DC-Balanced, 24-Bit LVDS Serializer and Deserializer	24:1 and 1:24 Serializer/Deserailizer, output pre-emphasis, DC balance coding, AC-coupled interface, wide -40C to +105C temp range

For more information on LVDS, visit us today at lvds.national.com

LIDAR System Design

applications. Particularly, recent developments in Analog-to-Digital Converter (ADC) technology allow for higher accuracy and lower power system designs.

Automotive system designers develop sophisticated LIDAR systems to automatically control vehicle speed and braking systems according to traffic conditions. Such systems can also dynamically control distance from other vehicles and obstacles and even manage safety features such as airbags. Advancements in this technology greatly improve driver comfort and safety. Other applications range in diversity from military range finding systems, which can operate over hundreds of kilometers, to vehicle detection systems at toll booths, which operate only over a few meters.

Irrespective of the application, the key analog component in the receive path of such a system is the ADC, which is used to digitize narrow pulses reflected from near and/or distant objects. Such ADCs need very fast sampling rates, large analog input bandwidth, and low power consumption. *Figure 1* shows a typical simplified block diagram for a LIDAR system.

Alternative System Methodologies

The most commonly used methods employed today are Continuous Wave (CW) laser with phase comparison and pulsed laser.

CW laser systems operate on the principle that the target object reflects a phase shifted version of the original transmitted signal. A phase comparator in the receiver compares the phase shifted version of the received signal with the original signal. The phase comparator output can be used to compute distance.

A pulsed laser system, as the name suggests, transmits and receives short, light pulses. Semiconductor pulsed lasers are used for applications requiring low cost, low power consumption, small size, and light weight. This methodology requires a very fast sampling ADC in the receiver and is the most common method in use today, and is therefore the focus of this article.

The distance that can be measured depends on several factors: the peak power of the laser, the laser beam divergence, optics and air transmittance, target reflectivity, and the sensitivity of the detector. Transmittance and reflectance parameters are usually imposed by the application. Design flexibility resides mainly in the selection of the laser source (power) and the receiver (sensitivity). The accuracy of TOF measurements depends on the pulse width of the laser and the speed and accuracy of the ADC used.

Depending on the application requirements, lasers in the order of a few milliwatts to several hundred Watts are used. The range equation gives the range of a semiconductor pulsed laser based on its power in Watts and the other system and atmospheric conditions. The range equation for a round trip distance to a foreign object is:

$$\text{Range} = \sqrt{\left[(P * A * Ta * To)/(Ds * PI * B)\right]}$$

P = Laser Power

A = Rx Optics Area (lens or mirror)

Ta = Transmittance of the atmosphere

To = Transmittance of the optics

Ds = Detector Sensitivity

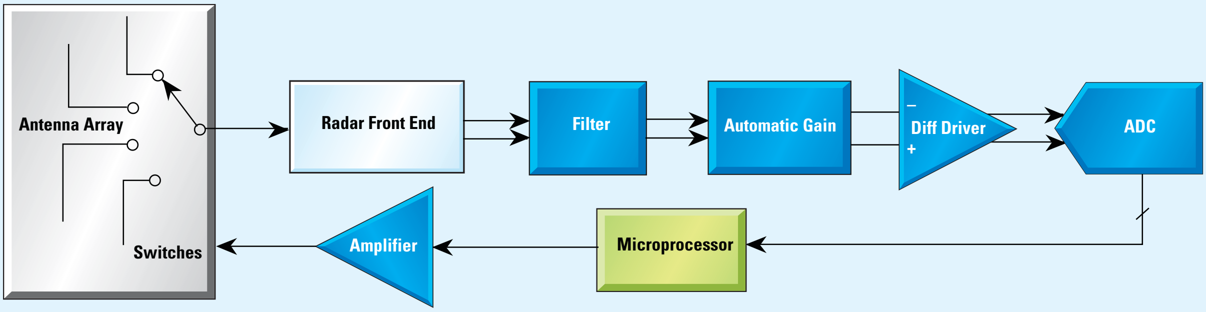
B = Beam Divergence in Radians

For low-light detection in the receiver, a designer has three basic detector choices: the silicon PIN detector, the silicon avalanche photodiode (APD), and the photomultiplier tube (PMT). APDs are widely used in instrumentation and aerospace applications, offering a combination of high speed and high sensitivity unmatched by other detectors.

The APD in the receiver converts the received light

Radar Solutions for Automotive Applications

Automotive Radar System



Amplifiers

amplifiers.national.com

High-Speed Amplifiers		
Product ID	**Description**	**Features**
LMH6502	Variable gain, linear in dB	130 MHz SSBW, 1800 V/μs Slew rate, >70 dB gain adjustment range, +/-75 mA output current
LMH6503	Variable gain, linear in V/V	135 MHz SSBW, 1800 V/μs Slew rate, -1V to +1V gain control range
LMH6505	Low power variable gain amplifier	150 MHz SSBW, 1500 V/μs Slew rate, 11 mA/ch supply current, 80 dB gain adjustment range
LMH6624/26	Single/dual, ultra low-noise, wideband, voltage-feedback amplifiers	1.5/1.3 GHz SSBW, 0.92/1.0 nV/√Hz Voltage noise, 100 μV Vos, +/-0.1 μV/√Hz, +5 to ±6V supply voltage range
LMH6550	Fully differential amplifier with disable	400 MHz SSBW, 3000 V/μs Slew rate, 2nd/3rd HD: -92/-103 at 5 MHz
LMH6551	Fully differential amplifier	370 MHz SSBW, 2400 V/μs Slew rate, 2nd/3rd HD: -94/-96 at 5 MHz
LMH6702	Single, ultra-low distortion, wide bandwidth, high-performance amplifier	1.7 GHz SSBW, 3100 V/μs Slew rate, 12.5 mA/ch output current, 2nd/3rd HD: -63/-70 at 60 MHz
LMH6703	Single, low-distortion, high-performance amplifier with shutdown	1.2 GHz SSBW, 4500 V/μs Slew rate, 11 mA/ch output current, 2nd/3rd HD: -69/-90 at 20 MHz
LMH6683	Triple, voltage-feedback amplifier, low differential gain/phase	190 MHz SSBW, 940 V/μs Slew rate, 6.5 mA/ch output current, CMIR < 0V
LMH6738	Triple, current-feedback amplifier, shutdown, 90 mA high-output current	750 MHz SSBW, 3300 V/μs Slew rate, 11.5 mA/ch output current, 2nd/3rd HD: -80/-90 at 5 MHz

Data Converters

www.national.com/adc

					Static Perf. (typ)	
Product ID	**Resolution (bits)**	**Speed (MSPS)**	**Supply Voltage**	**Power (mW)**	**INL**	**DNL**
ADC08200	8	200	3	210	±1.0, -0.3	±0.4
ADC081000	8	1000	1.9	1450	±0.35	±0.25
ADC081500	8	1500	1.9	1200	±0.3	±0.15
ADC08D500	8-bit dual	500	1.9	1400	±0.3	±0.15
ADC08D1000	8-bit dual	1000	1.9	1600	±0.3	±0.15
ADC08D1500	8-bit dual	1500	1.9	1840	±0.3	±0.15
ADC10040	10	40	3	55.5	±0.3	±0.3
ADC10065	10	65	3	68.4	±0.3	±0.3
ADC10080	10	80	3	78.6	±0.5	±0.25
ADC10DL065	10-bit dual	65	3.3	360	±1.0	±0.3
ADC12L080	12	80	3.3	425	±1.2	±0.4
ADC12DL040	12-bit dual	40	3	210	±0.8	±0.3
ADC12DL065	12-bit dual	65	3.3	360	±0.75	±0.4
ADC12DL080	12-bit dual	80	3.3	447	±1.1	±0.4
ADC12QS065	12-bit quad	65	3.3	800	±0.6	±0.3
ADC14L020	14	20	3.3	150	±1.4	±0.5
ADC14L040	14	40	3.3	235	±1.5	±0.5

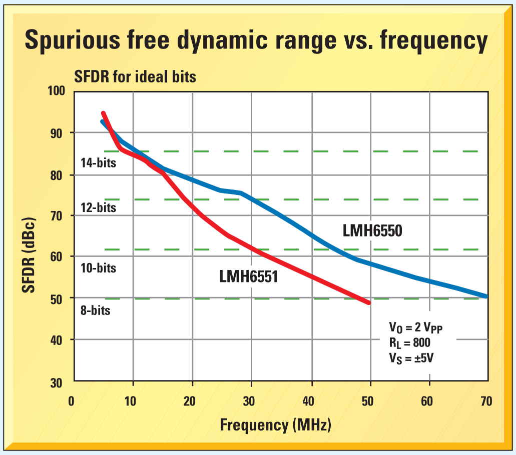
LMH6550 Features

- 400 MHz SSBW
- -92/-103 dBc HD2/HD3 at 5 MHz
- 10 ns shutdown/enable
- -68 dB balance error (V_{OUT} = 1.0 V_{P-P}, 10 MHz)

LMH6551 Features

- 370 MHz SSBW
- -94/-86 dBc HD2/HD3 at 5 MHz
- 70 dB balance error (V_{OUT} = 0.5 V_{P-P}, 10 MHz)
- Single +3.3V, +5V or ±5V supply voltages

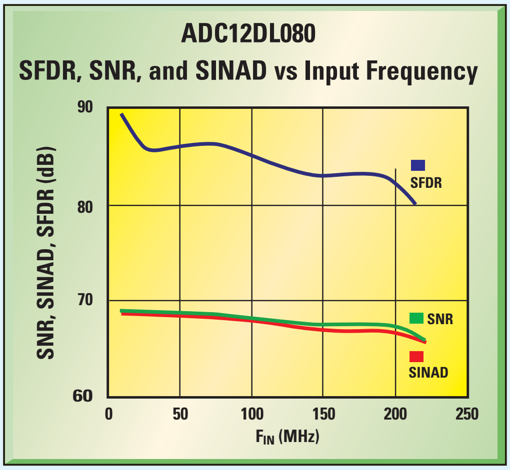
For FREE samples, datasheets, and more information, visit
www.national.com/pf/LM/LMH6550.html
www.national.com/pf/LM/LMH6551.html



ADC12DL080 Features

- Dual-channel, 12-bit, 80 MSPS sampling rate
- Single 3.3V supply operation
- Consistently high linearity and dynamic range for inputs up to 200 MHz
- Low power consumption
- Duty cycle stabilizer
- TQFP-64 package (10 x 10 x 1 mm, 0.5 mm pin pitch)
- Operates over the industrial temperature range of -40°C to +85°C

For FREE samples, datasheets, and more information, visit
www.national.com/pf/DC/ADC12DL080.html



Dynamic Performance (Typ)					
ENOB (bit)	SINAD (dB)	SNR (dB)	SFDR (dB)	THD (dB)	Packaging
7.3	46	46	60	-60	TSSOP-24
7.5	47	48	59	-57	LQFP-128 Exp. Pad
7.4	46.3	47	56	-54.5	LQFP-128 Exp. Pad
7.5	47	48	55	-55	LQFP-128 Exp. Pad
7.4	46	47	55	-55	LQFP-128 Exp. Pad
7.4	46.3	47	56	-54.5	LQFP-128 Exp. Pad
9.6	59	59	80	-77	TSSOP-28
9.5	59	59	80	-72	TSSOP-28
9.5	59	59	79	-75	TSSOP-28
9.8	61	60	80	-78	TQFP-64
10.7	66	66	80	-77	LQFP-32
11.1	69	69	86	-83	TQFP-64
11.1	69	69	86	-84	TQFP-64
11	69	69	82	-80	TQFP-64
11.1	69	69	85	-83	LLP-60
12	74	74	93	-90	LQFP-32
11.9	73	73.3	90	-86	LQFP-32

pulse to an electrical signal. It outputs a current proportional to the incident light. A transimpedance amplifier is then used to convert the current to a voltage signal. A good transimpedance amplifier should have high gain, high input impedance, ultra-low voltage and current noise, and low input capacitance. It normally has a FET or MOS input stage to meet these requirements. Input noise voltages <1.0 nv√Hz and current noise <15 fA√Hz are achievable with high performance devices. The output of the transimpedance amplifier is generally converted to a differential signal and amplified before digitization by an ADC.

The transmitted pulse is generally greatly attenuated (atmospheric conditions etc.) leading to a large difference in strength between transmitted and received pulses. Objects in the near vicinity of the transmitter can also reflect high power signals back to the receiver. This leads to demanding dynamic range requirements for the receive system. The receive system should be sensitive enough to deal with full power and very low reflected pulses. Dynamic range requirements in the order of 100 dB are not uncommon. This dynamic range is generally achieved by using a Variable Gain Amplifier (VGA) or Digital VGA (DVGA) in the front end prior to the ADC.

Benefits of Gigahertz Sample Rate ADC and Over-Sampling in LIDAR Systems

The range measurement accuracy that can be achieved is directly related to the ADC sampling frequency.

The Speed of light c = 3E+08 m/s.

At 1 GSPS, the ADC has a clock period of 1 ns. In a 1 ns sampling instant, light will travel 0.3m or 30 cm. Therefore the resolution at 1 GSPS is 30 cm/m, meaning an accuracy of +/- 15cm is achievable at 1 GSPS over any given distance. The error will increase as sampling frequency is reduced.

As briefly mentioned above, certain physical properties of the target can be determined by the change in wavelength of the reflected light pulse, known as the Doppler shift. To measure the change in wavelength of narrow pulses, ADCs with sample rates in the order of 1 GHz or higher are required.

The shape of a received pulse also contains information regarding the properties of the target. The shape can only be determined by a considerable over-sampling ratio. Over-Sampling also benefits in the digital domain in terms of processing gain, which results in higher SNR.

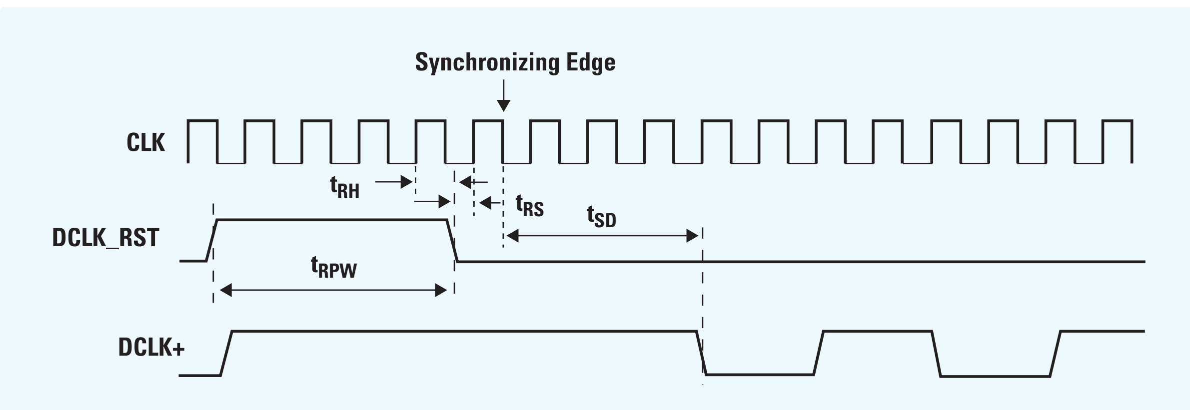


Figure 2. DCLK reset timing in DDR mode

Multiple ADC synchronization

ADCs are often time interleaved to increase sampling frequencies beyond what is available from single devices. The benefits of increasing the sampling frequency are finer pulse shape and timing resolution. One of the inherent challenges addressed by this article is synchronizing the ADC output data streams. The system developer must know exactly which digital words at the ADC outputs correspond to the pulse sampled at the system front end. How is this achieved?

To simplify time interleaving, the ADC08Dxxx family has the capability to precisely reset its sampling clock input to Data Output Clock (DCLK) output relationship as determined by the user-supplied DCLK_RST pulse. This allows multiple ADCs in a system to have their DCLK (and data) outputs transition at the same time with respect to the shared CLK input that they all use for sampling. *Figure 2* shows the DCLK reset timing in DDR mode.

As a signal propagates at 20 cm/ns (i.e. 1cm in 50ps) on FR04 PCB material, the setup times shown in *Figure 2* can be very difficult to achieve if the ADCs are not placed very close together.

In such cases, we recommend stopping the clock for a short time (< 50 ns) so that the AC coupling is maintained during the DCLK_Res assertion. Note that AC coupling for the input clock is recommended. The time constant of the AC-coupling capacitors is 50 Kø (internal bias resistors) x 4.7nF (external AC-coupling capacitors) = 235 µs. Thus there is no concern that stopping the clock for < 50ns will significantly de-bias the AC coupling capacitors.

It is also recommended to use the duty-cycle stabilizer in the clock-receiver (default configuration). Its correction time-constant is short (100 ns to 500 ns) and is slew limited. For this reason also, the clock should be stopped for no more than 50 ns, once the clock has run for > 3 ms to establish the correct potential on the AC coupling capacitors. During the stopped clock, the DCLK_Res can be asynchronously asserted. A simplified block diagram for DCLK reset is illustrated in *Figure 3*.

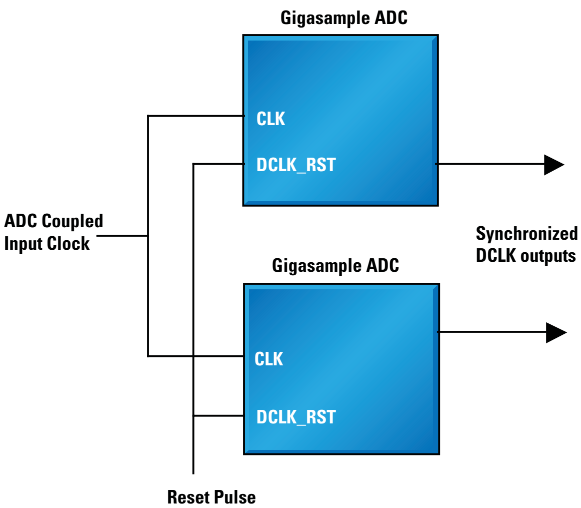


Figure 3. DCLK-RST for multiple ADC synchronization

Summary

By combining low power with excellent dynamic performance, the ADC08Dxxx family provides an excellent solution for high accuracy LIDAR systems. Integrated features such as the multiple ADC synchronization feature greatly simplify the process of time interleaving at board level. 6 GSPS is achievable by interleaving two 1.5 GSPS ADCs in Dual Edge Sampling (DES) mode giving a resolution of +/- 2.5 cm/m. ■

Design Tools

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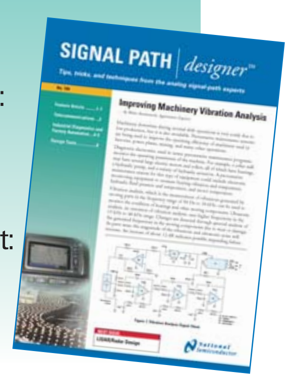

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