

# Wide Bandwidth Receiver Implementation by Interleaving Two Gigasampling ADCs

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High-Speed Data Converters

## ABSTRACT

Applications like wide bandwidth receivers for electronic warfare systems and Scan and track RADAR systems require large instantaneous sampling bandwidth. The Nyquist bandwidth for such requirements may extend from DC to more than 4 GHz. Stand-alone solutions for such applications with higher performance are not available today. However TI’s gigasample ADC family parts like the ADC12D1800RF, which can support an effective sampling rate of 3.6 GSPS, can be used in such applications in an interleaved architecture. This application note describes how such external interleaving of multiple ADCs can be carried out and the corresponding techniques to correct the performance loss seen.

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# 1 Introduction

## 1.1 Applications

Wideband frequency scanning applications require the system to detect the transmitted frequencies present in the airspace instantaneously. Such applications require the receiver chain to have a Nyquist band that accommodates all the possible frequencies. For example, for a system requiring frequency detection from 100 MHz to 4 GHz, the sampling system will require a clock of 8 GHz. Such wideband applications are also required for reconstruction of transmitted pulses with high time resolution for RADAR applications. They are essential for reconstruction of pulses with very short rise times.

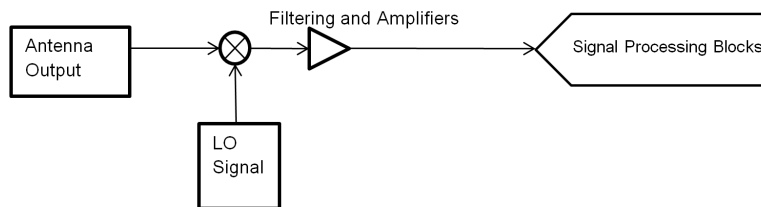


Figure 1. Sample Frequency Scanning Application

## 1.2 Current Techniques Used

Presently, due to the non-availability of ADCs which can handle signal Bandwidths up to 4 GHz, the implementations uses multiple parallel down-conversion stages using mixers to down-convert different filtered components of the frequency bandwidth of interest followed by multiple signal chains with ADCs.

The issues in this method are:

- Requires multiple MIXERs, ADCs, filter blocks in down-conversion stages
- More complexity in terms of implementation and meeting the system noise performance
- Higher power consumption
- Adds to system cost
- Required parallel processing on the digital block to carry out FFT on two parallel data streams

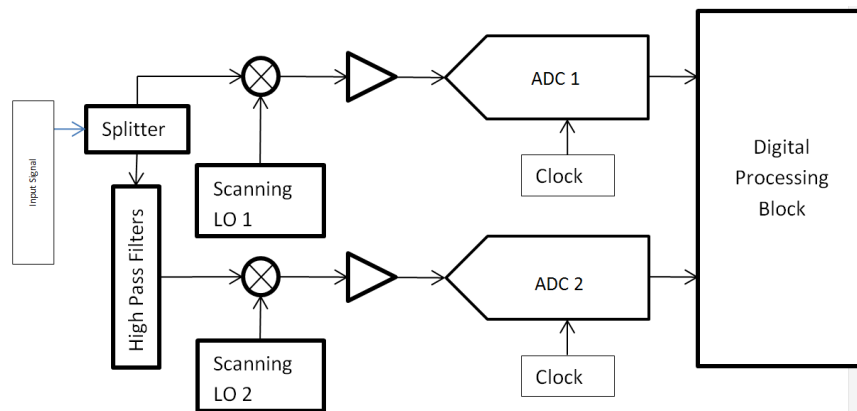
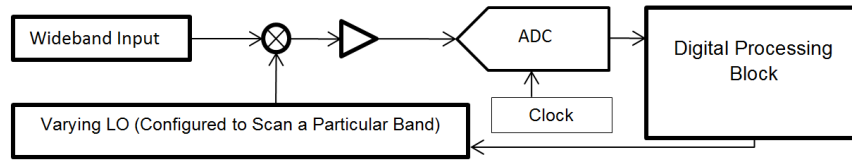


Figure 2. Conventional Wide Bandwidth Receiver With Parallel Signal Chains

Another option is to use a single signal chain while varying the LO using a DDS block and detecting different frequency ranges in separate time windows. However, this scheme has the possibility of missing frequencies emitted in a different band while the LO is configured to detect another band of frequencies. The system does not provide instantaneous wide bandwidth.



**Figure 3. Wideband Frequency Scanning With Varying LO**

### 1.3 Proposed Solution

The wideband receiver system solution can be implemented using the maximum available sampling rate ADCs and using the interleaving concept. A brief description of the proposed solution follows:

- The solution can be implemented with the interleaving of two Giga sampling ADCs from TI which are capable of sampling at 4 GSPS. This can make the overall sampling rate close to 8 GSPS, which is capable of handling up to 4-GHz Nyquist bandwidth.
- Interleaving Giga-sample ADCs needs phase-shifted sampling clocks. ADCs capture the input signal samples alternatively with half clock period delays between their sampling clocks. One ADC can sample the input at rising edge and other ADC can sample the input at the falling edge of the externally-generated sampling clock.
- Presently available Giga Sample ADCs already feature interleaving of two ADCs internal to the chip to give a sampling rate of double the clock frequency. This means, there are two 2 GSPS ADCs inside the chip with interleaving and sample the input at a clock with 180 degree phase shift.
- Thus, the clock to the next interleaving ADC is phase-shifted by 90 degrees. In this way, one ADC IC samples the input clock phase of 0 degrees, 180 degrees and the other ADC IC is sampling the input at 90 degrees and 270 degrees

The proposed system uses ADC12D1x00RF for ADC conversion and the LMK0480x is used to provide the phase-shifted clocks. The Giga sample ADCs from TI contain two integrated ADCs which can be used in an interleaved format as a single ADC, thereby, doubling the effective sampling speed. Externally interleaving two such ADCs will result in further doubling the effective sampling rate which results in a system sampling rate 4 times the sampling clock frequency. For example, if the system uses two ADCs, both internally interleaved and supplied a clock of 1.5 GHz the effective sampling rate will be extended to 6 GSPS.

The system advantages of the proposed solution are:

- Allows direct sampling of wide bandwidth signal without the requirement of parallel down-conversion stages
- Reduced power consumption compared to the existing solutions

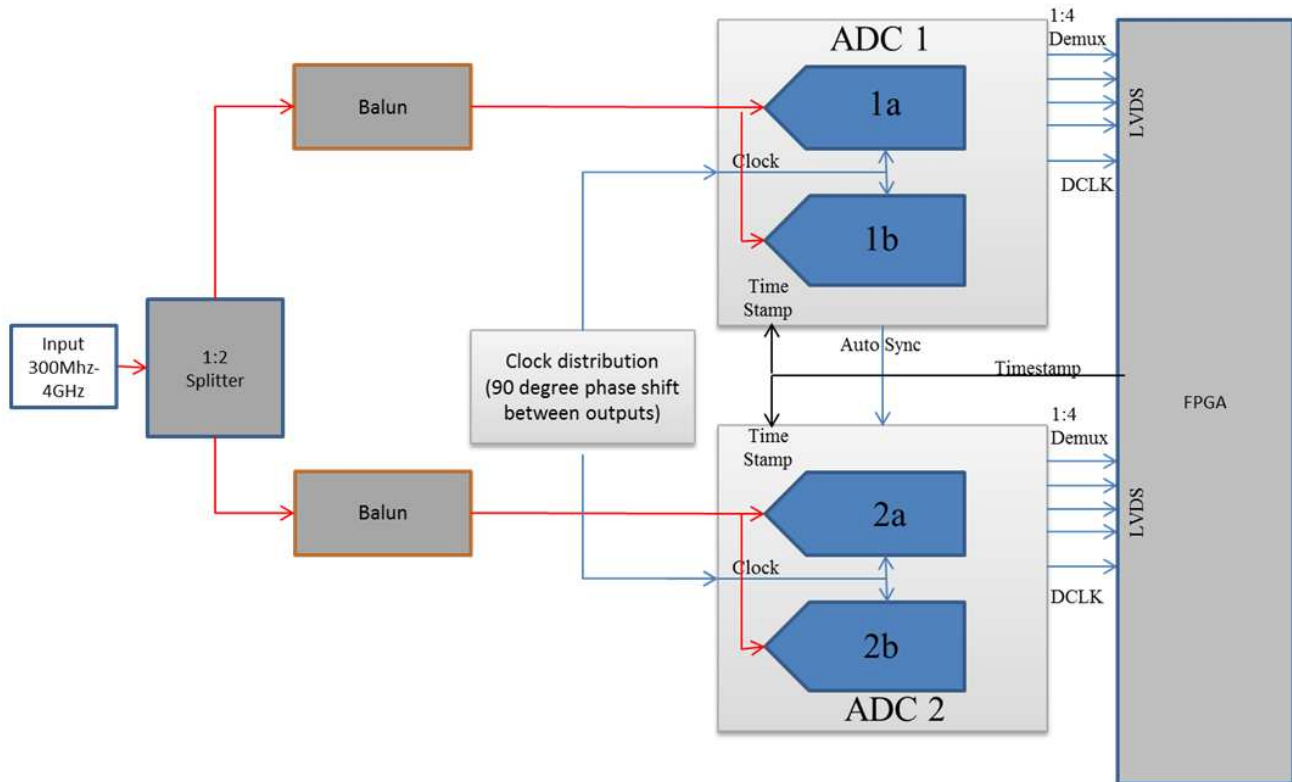


Figure 4. Proposed System for Wide Bandwidth Scanning Using Multiple Interleaved ADCs

## 2 Concept of ADC Interleaving

The ADCs sample the input waveform alternately, and the sample waveforms can be written as:

$$y_1(t) = x(t) \sum_k \delta(t - kT_{ck}) \text{ (Sampled waveform on ADC 1)} \tag{1}$$

$$y_2(t) = x(t) \sum_k \delta(t - kT_{ck} - T_{ck}/2) \text{ (Sampled waveform on ADC 2)} \tag{2}$$

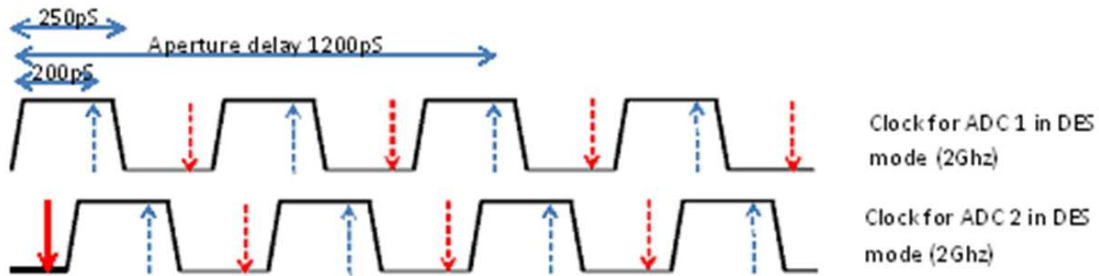


Figure 5. Sampling Timing for Both ADCs

In the frequency domain, this wave form can be interpreted as:

$$Y_1(f) = \frac{1}{T_{ck}} X(f) \sum_k \delta(f - k f_{clk}) \text{ (Frequency domain waveform on ADC 1)} \tag{3}$$

$$Y_2(f) = \frac{1}{T_{ck}} X(f) \sum_k \delta(f - k f_{clk}) e^{-j\pi k} \text{ (Frequency domain waveform on ADC 2)} \tag{4}$$

$f_{clk}$  is half the apparent sampling frequency after interleaving. Odd  $k$  terms in frequency domain cancel out when added while effectively doubling the Nyquist bandwidth of the system when the ADC outputs are multiplexed. (*Design Considerations for Interleaved ADCs*) [ 1].

### 3 System Implementation Challenges

The system suffers from certain challenges which may lead to the degradation of system performance in the implementation process:

- Phase-shifted clocks are required to be supplied to the ADCs in the system and need to be accurately generated. The sampling clock generator needs to have features to generate the 90-degree phase-shift clocks with delays built in for matching the phase of the clocks if the phase difference is not accurate. These clock signals can be generated with a single clock-generation PLL like the LMK04808, which has phase-shift options on the outputs.
- Timing or phase mismatch in signal path and clock timing mismatch will result in a loss in signal quality. Any error in generating the exact phase difference for different ADCs will create  $F_s/2 - F_{in}$  spurs. These imperfections need to be resolved with phase matching of the ADC signal chains with methods discussed in [Section 4](#).
- Any offset mismatch between the two ADCs will give rise to a spur at  $F_{clk}^*/2$ , due to toggling between unequal DC offsets when alternating samples are captured. DC offset is adjusted by calibrating ADC for offset correction. In this case,  $F_{clk}$  is the sampling rate of each individual ADC; the effective sampling rate after interleaving is  $F_s = 2 \times F_{clk}$ .
- Gain mismatch between the ADCs results in aliased spurs on the output spectrum due to the presence of aliased spurs after adding the waveforms represented in [Equation 3](#) and [Equation 4](#).
- The output data of the Giga sample ADCs should be synchronized. In Giga sample ADCs, the outputs are de-multiplexed and provided to reduce the data rates. This provides an easy interface with FPGAs. Synchronizing the multiple ADC output data needs to be done as multiple ADCs are used for the interleaving.

### 4 Phase Matching of Multiple ADCs

Any timing variation between the sampling clocks or the path delay of the ADC signal path will result in large spurs. Details of sources for this mismatch are explained in detail in section 1.3 of [ 6]. This section explains the impact of such an imperfection and methods to mitigate them.

#### 4.1 Occurrence of $F_s/2 - F_{in}$ Spur

A timing mismatch between the two ADCs will result in the input waveform being sampled away from the required instant. In the ideal case, the ADCs sample the waveforms at 90-degree offset. However, phase mismatch will cause variation from this case. Modifying [Equation 1](#) through [Equation 4](#) to accommodate for a phase variation of  $\Delta T$ , equations can be built to reflect this mismatch in the frequency domain (Design Considerations for Interleaved ADCs)[ 1].

$$y1(t) = x(t) \sum_k \delta(t - kT_{ck}) \text{ ADC 1 output} \quad (5)$$

$$y2(t) = x(t + \Delta T) \sum_k \delta\left(t - kT_{ck} - \frac{T_{ck}}{2}\right) \text{ ADC 2 output} \quad (6)$$

$$\approx \left[ x(t) + \Delta T \frac{dx}{dt} \right] \sum_k \delta\left(t - kT_{ck} - \frac{T_{ck}}{2}\right) \text{ (Assuming mismatch is small compared to clock period)} \quad (7)$$

$$Y1(f) = \frac{1}{T_{ck}} X(f) \sum_k \delta(f - k f_{clk}) \text{ ADC 1 output in frequency domain waveform} \quad (8)$$

$$Y2(f) = \frac{1}{T_{ck}} (X(f) + j2\pi f \Delta T X(f)) \sum_k \delta(f - k f_{ck}) e^{-j\pi f T_{ck}} \text{ ADC 2 output in frequency domain} \quad (9)$$

$j2\pi f \Delta T X(f)$  term creates images at  $f \pm f_{clk}$ , since they do not cancel with terms of  $Y1$  for  $k = 1, -1$  with amplitude proportional to input frequency and timing mismatch.

Final spur amplitude = carrier power +  $20 \log M 2\pi f \Delta T$  (for single tone input)

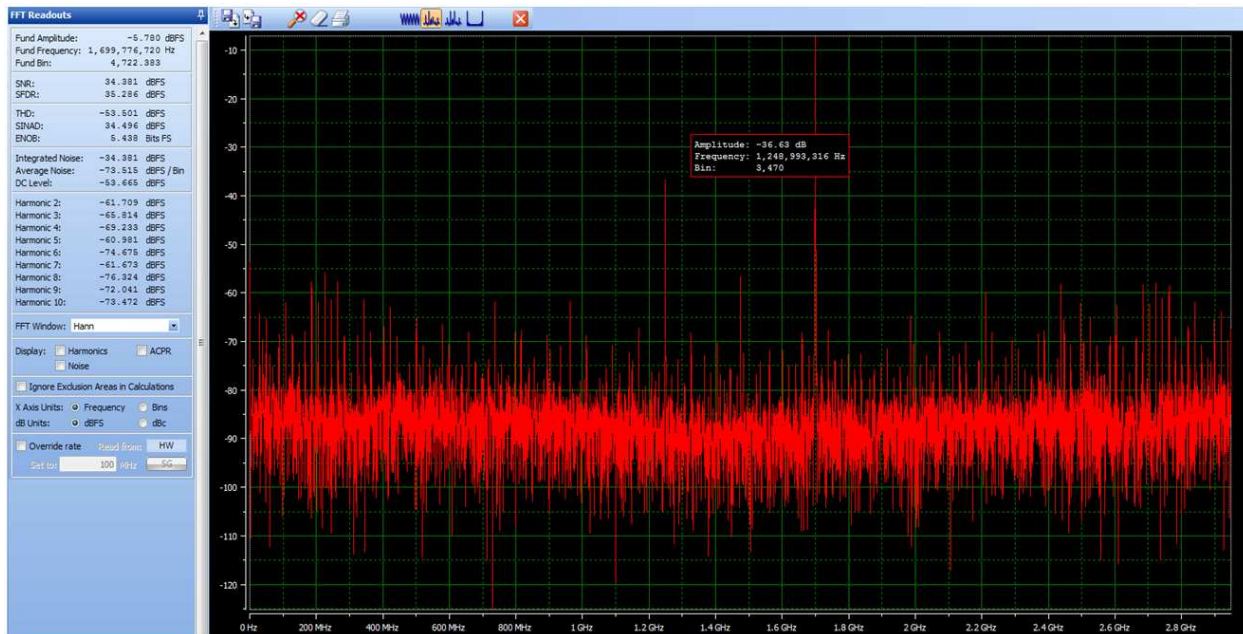


Figure 6. Interleaving Spur at  $F_s/2 - F_{in}$

For example, for the test case of  $F_{clk} = 2.949$  GHz, and for an input signal of 1.7 GHz, the interleaving spur can be seen at 1.248 GHz ( $F_{clk} - F_{in}$ ). In this case the effective sampling frequency is 5.898 GHz.

## 4.2 Methods to Minimize Phase Mismatch

The phase mismatch between the two ADCs can be minimized using various features in the ADC and LMK clock. Detailed explanation of the mismatch causes and correction techniques to avoid this mismatch is the subject of another application note ([SLAA643](#)). They are explained briefly in this section.

### 4.2.1 Synchronizing Digital Data Output to Resolve Phase Mismatches Greater Than a Sampling Period

The timestamp and auto-sync features of TI's Gigasample ADC family can be used to resolve any sample mismatches between the ADCs which may occur due to loss of synchronization in the digital interface or FPGA capturing.

#### Auto-sync

Auto-sync is a feature on the ADC12D1600RF/ADC12D1800RF/ADC12D200RF which can be used to synchronize the divided-down DCLKs from multiple ADCs such that the data is latched into the FPGA at the same time. It allows flexible length for the synchronizing signals by incorporating a delay block on the RCIN. The DRC delay block allows the system to select a stable region for the RCIN which meet setup hold time requirements over PVT variations. For detailed description on the autosync feature, refer to application note (AN-2132 Synchronizing Multiple GSPS ADCs in a System: The AutoSync)[ 2].

#### Timestamp

- Timestamp is a feature provided in the ADC12D1x00-series ADC which allows the user to input a synchronizing signal to the TIME STAMP (referred to D0 timestamp pin of the ADC) which is converted into a 1-bit value on the ADC. Using the last bit does not affect the ADC performance since ENOB of the 12-bit ADC is around only 9 bits.
- The signal faces the same delay as faced by the input signal, that is:  $t_{latency} + t_{output\ delay} - t_{aperture\ delay}$  through the ADC channel pipeline.
- An identical timestamp signal is sent to the multiple ADC modules in the system. The output data streams can be aligned according to the timestamp signal edges since it is known that the ADCs are receiving the input signals at the same time. It can be used to correct any sample delays between two

ADC output streams because a matched timestamp transition on the ADCs represents input samples are received on the same clock edge for both ADCs.

- It is not required for the timestamp signal to be synchronized to the sample clock, but by synchronizing the signal and providing an additional analog delay, the signal edge can be placed in the middle of the sampling clock period such that they always fall on the same side of the sampling clock edge.
- The timestamp signal can be generated by the clocking device or the FPGA with the previously mentioned delay. Timestamp to the ADC receiving the phase shifted clock should be shifted by the same delay.
- Using a higher frequency timestamp signal can cause mixing spurs with the input to the ADC, due to capacitive coupling with signal path inside the ADC. A low-frequency pulse is recommended with a time period greater than maximum phase error possible in system, but lesser than half the sample stream width. The frequency should be adjusted to less than the resolution bandwidth, if possible.

#### 4.2.2 Correcting Sub-Sample Period Phase Mismatch

##### Aperture delay correction

Fine variation of the aperture delay can enable the user to correct mismatch between the ADCs due to variations in signal path or clock skew.

- Aperture delay is defined as the amount of delay, measured from the sampling edge of the CLK input, after which the signal present at the input pin is sampled inside the device. (From Sample Instant to Data Output: Understanding Latency in the GSPS ADC)[ 2]
- The ADC provides an aperture delay adjust option where a programmed delay can be added to sampling clock changing  $T_{ad}$ . This delay can be adjusted using the coarse ( $\approx 340$ -fs steps) or finer ( $\approx 34$ -fs steps) adjust options provided.
- Varying aperture delay may affect signal integrity, especially at higher sampling rates and thus a minimal amount of adjustment should be used. The use of this feature should be avoided at maximum sampling rates. Adding additional delay in the clock path adds to the aperture jitter and delays all clocks generated by the clock tree inside the ADC module.
- Interleaving requires finer phase matching since the spur amplitude is proportional to the delay. The adjustment exhibits approximately 10% change with PVT variations. Therefore, it is recommended to calibrate this delay on power on with a sample waveform and maintain a temperature-based lookup table.

## 5 Gain Mismatch

As shown in Equation 3 and Equation 4 (repeated here for convenience), the ADC outputs in frequency domain can be shown as:

$$Y1(f) = \frac{1}{T_{ck}} X(f) \sum_k \delta(f - k f_{clk}) \text{ (Frequency domain waveform on ADC 1)}$$

$$Y2(f) = \frac{1}{T_{ck}} X(f) \sum_k \delta(f - k f_{clk}) e^{-j\pi f T_{ck}} \text{ (Frequency domain waveform on ADC 2)}$$

However, if the gain of ADC 2 is lesser than that of ADC 1 by a factor  $x$ , then the output power of the second ADC will be scaled by  $x^2$ . The  $Y1$  and  $Y2$  terms for  $k = 1, -1$  do not completely cancel out as expected and therefore result in spurs at  $F_s/2 - F_{in}$  with a power of  $(1 - x)^2$  times carrier power (Design Considerations for Interleaved ADCs)[ 1]. This mismatch can be eliminated by varying the full scale reading registers for both the ADCs to match the gain over full scale input.



## 6 System Implementation

A basic lab setup was made to prove the concept with two ADC12D1800RFRF EVMs with the ADC12D1800RF ADC (ADC12D1800RF datasheet)[ 4]. A block diagram is shown in Figure 7.

- LMK0480x-series clock generators were used to clock ADCs with required phase shift. These are low-jitter, dual-PLL devices with integer dividers and multiple outputs. (LMK04808 datasheet)[ 6]. The digital delay with the available half VCO frequency step feature is suitable for phase shift needs in this application.
- Analog delay can be used for fine tuning the phase mismatch in 25-ps steps. However it was observed that enabling the analog delay block reduces SNR of ADC by 3 dB.
- The LMK0480x was also used to generate the time stamp signal. The signal is synchronized to the input sampling clock with a fixed delay for stable sample capture on both the ADCs. 4.9-MHz LVCMOS clock outputs were used. However, a low-frequency FPGA pulse synchronized with the data clock can also be used to minimize the leakage of the timestamp signal into the signal path.
- 4 dBm, 1474.47-MHz LVPECL clock used for both ADCs synthesizing an equivalent ADC sampling speed of 2948.992 MHz and equivalent system sampling speed of 5897.984 MHz after interleaving.
- Optionally, a clock generator like LMX2581 with the fractional divider can be used to generate a wider range of sampling frequencies. The LMX2581 can be synchronized to the timestamp signal by deriving the reference from the same clock source generating the timestamp signal and running the sampling clock generator in zero-delay mode.

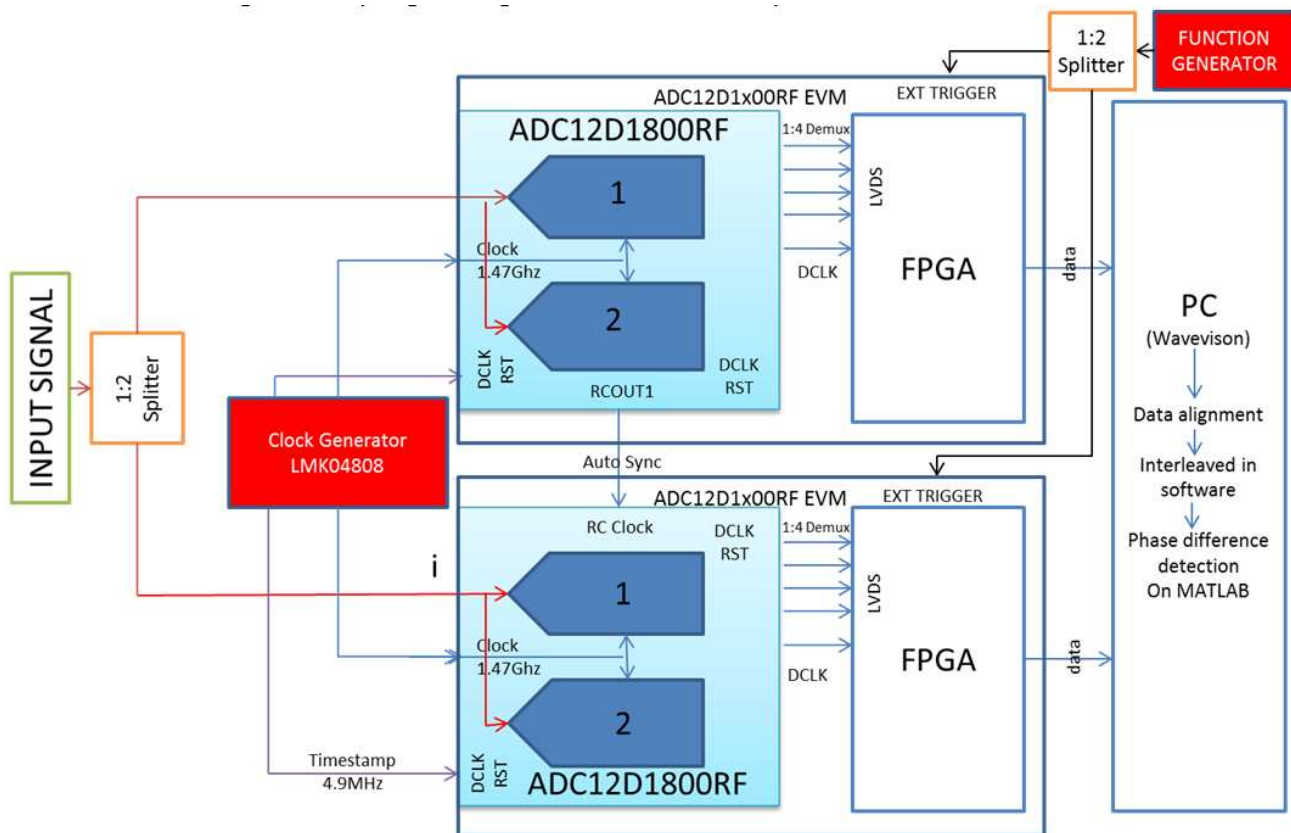
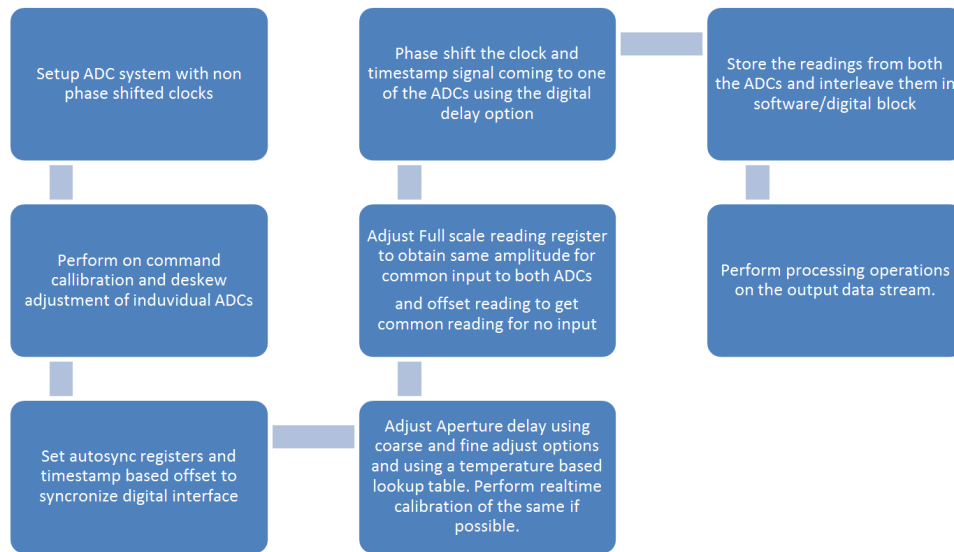


Figure 7. Lab Setup for Interleaving Implementation

Refer to [SLAA643](#) to for a detailed description of the lab setup. The sequence of steps taken in the implementation of the system described in this section is shown in Figure 8:



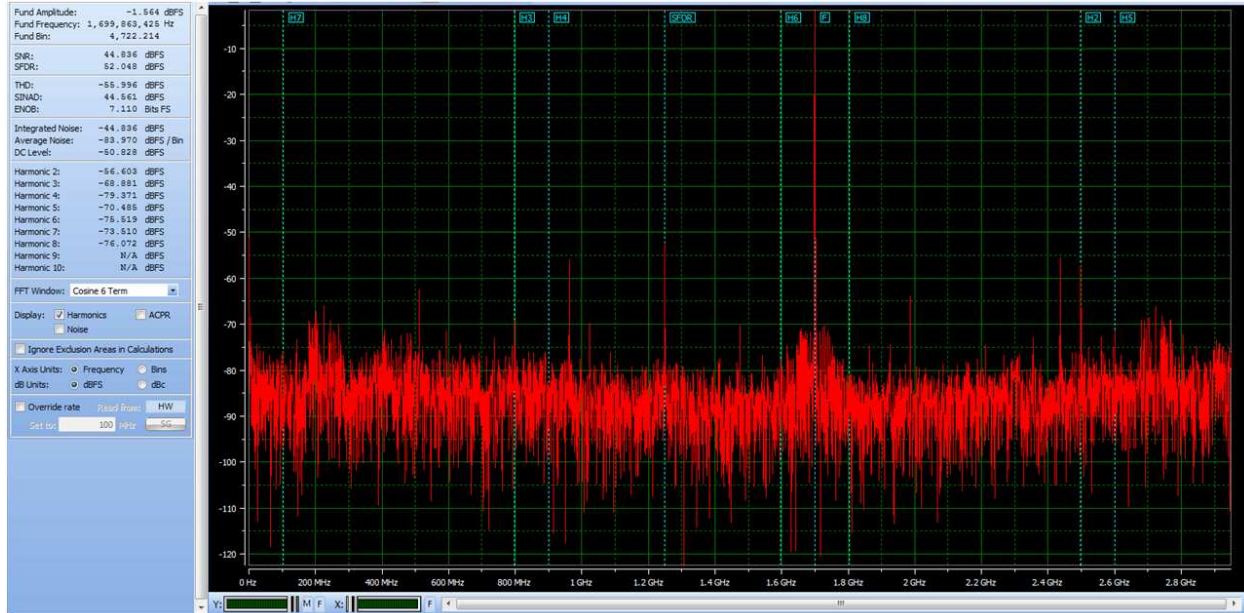
**Figure 8. Sequence of Steps for an Interleaved ADC System**

## 7 Results

The following results were obtained with gain and phase correction on the ADCs.

**Table 1. Results of Interleaved ADC System**

Input Frequency (GHz)	Signal Amplitude (dBFS)	SNR (dBFS)	SFDR (dBFS)	Spur Frequency	SNR ADC 1	SNR ADC 2
1.7	-1.55	44.836	52.048	1.249	44.998	46.189
2.5	-7.9	41.441	42.774	.449	46.879	49.564



**Figure 9. Output for 1.7-GHz Input Waveform**

$$\begin{aligned}
 \text{Spur amplitude} &= \text{carrier power} + 20\log 2\pi f \Delta T \\
 -48.775 &= -1.250 + 20\log(2\pi(1700 \times 106 \Delta T)) \\
 \Delta T &= 393 \text{ fs}
 \end{aligned}
 \tag{10}$$

With a coarse calibration step size of 340 fs, SFDR can be corrected till -50.04 dBFS.

SNR of the ADCs can be improved by using a filtered input signal and periodic timestamp signal. Also, the SNR is deteriorated due to the relay in the clock path on the ADC EVM. Higher SNR (>50 dBFS) is expected with optimum system conditions. Recently released ADCs have higher input bandwidth to provide improved and flat amplitude response for wider bandwidth applications. Refer to <http://www.ti.com/lscs/ti/data-converters/high-speed-adc-greater-10msps-overview.page>.

Phase variation is dependent on temperature and other ambient conditions. Systems can be optimized with calibration over power-resets and temperature variation. A lookup table for temperature versus aperture delay addition can be created to counter variations with temperature.

## 8 Conclusion

The implementation in [Section 6](#) describes a solution with multiple Giga sample ADCs used in an interleaved manner. It describes the possible performance degrading factors and the parameters influencing the same, namely gain mismatch, phase mismatch, and offset mismatch and methods to mitigate them using the available TI solutions. As the lab results show, it is possible to design a wide bandwidth receiver system with reasonable performance. This document provides basic implementations that can be used as a starting point for a wide bandwidth receiver.

## 9 References

1. Razavi, B., *Design Considerations for Interleaved ADCs*, IEEE Journal of Solid-State Circuits, August 2013, pp.1806–1817.
2. Pilsch, M., *From Sample Instant to Data Output: Understanding Latency in the GSPS ADC*, 2013.
3. AN-2132 Synchronizing Multiple GSPS ADCs in a System: The AutoSync Feature ([SNAA073](#)).
4. ADC12D1800RF datasheet ([SNAS518](#)).
5. *Synchronizing the GigaSample ADCs Interfaced With Multiple FPGAs* ([SLAA643](#)).
6. LMK04808 Datasheet ([SNAS489](#)).

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