Application Report
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Clocking Optimization for RF Sampling Analog-to-Digital Converters

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ABSTRACT

In many of today's high-frequency systems, key specifications are achieved with precise optimizations in the device itself as well as all its peripheral blocks. A thorough understanding and well-designed system with all these components in mind is necessary to attain the best results. This is especially true in applications with RF sampling Analog-to-Digital Converters (ADC), where the sampling clock may use high performance synthesizers to generate very noise high-frequency clock signals. These synthesizers require careful design for the best integrated noise which directly impacts the signal-to-noise ratio (SNR) performance of the ADC. This application report helps understand these performance specifications, show how to approach the optimization process, and provides relevant information to help reach the highest performance levels.

1 ADC Signal-to-Noise Ratio Components

The signal-to-noise ratio (SNR) of the ADC is a key specification. A high number for this specification indicates the ADC can better distinguish the desired input signal from the undesired noise that is also captured during sampling. There are three main contributors to the SNR of an ADC, the quantization and thermal noise of the ADC (does not change with input frequency) and the clock jitter (depends on the frequency). Figure 1 shows an example of an ADC thermal noise of 62.5 dBFs and the SNR of the clock (with a jitter, t_{clock_jitter} of 50 fs). The SNR of a clock can be derived from knowing the frequency of the signal and the jitter (discussed in Section 2) with Equation 1:

$$SNR_{clock\_jitter}\ [dBc] = -20 \times \log\left(2\pi \times F_{input} \times t_{clock\_jitter}\right) \quad (1)$$

As the figure illustrates, the high SNR of the ADC is maintained for the low input frequencies, but starts to be dominated by the clock SNR at higher input frequencies.

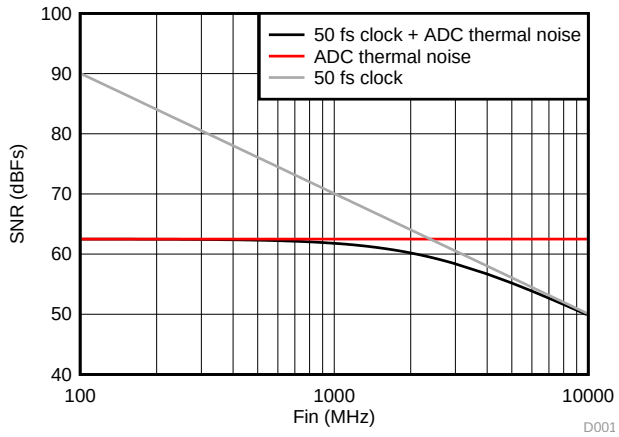

Figure 1. ADC and Clock Jitter Contribution to SNR

Now that the impact of clock jitter to the total SNR when the clock has a jitter of 50 fs is known, look at the impact of lower performance clock (with higher jitter). As Figure 2 shows, the higher the jitter of the clock, the more severe the effect of degradation in SNR from the clock performance at higher ADC input frequencies. Therefore, it is essential to make sure the clock jitter is the lowest possible, and this specification can be adjusted according to different parameters of a high frequency synthesizer clock source to achieve the optimal low jitter value.

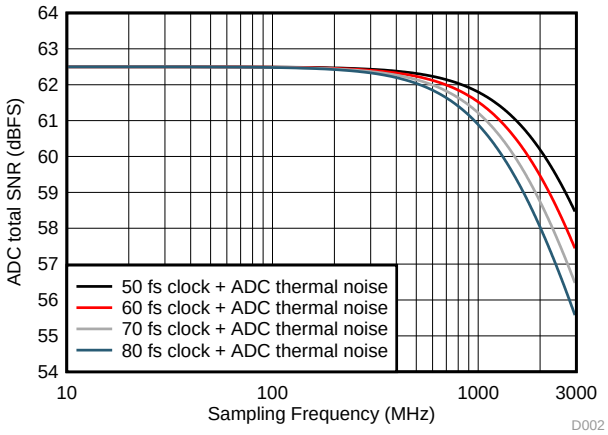

Figure 2. Impact of Different Clock Jitter to Total SNR

2 Understanding Phase Noise and Jitter and SNR

Designing for and finding out the lowest jitter starts from knowing the phase noise of a clock signal from a synthesizer. In the time domain, an ideal sine-wave clock signal looks like the waveform in the bottom-left of Figure 3. Realistically, due to the real world imperfections of components of a frequency synthesizer, there is additional noise which deviates the waveform from its ideal positions. Similarly, the same sine-wave converted to the frequency domain is a single pulse at the frequency of oscillation. The noise addition appears in the form of phase noise (skirts beside the ideal pulse). Low phase noise of a synthesizer suggests that the signal is cleaner, provides better performance, and ultimately has lower jitter (discussed in Section 3) to clock the ADC.

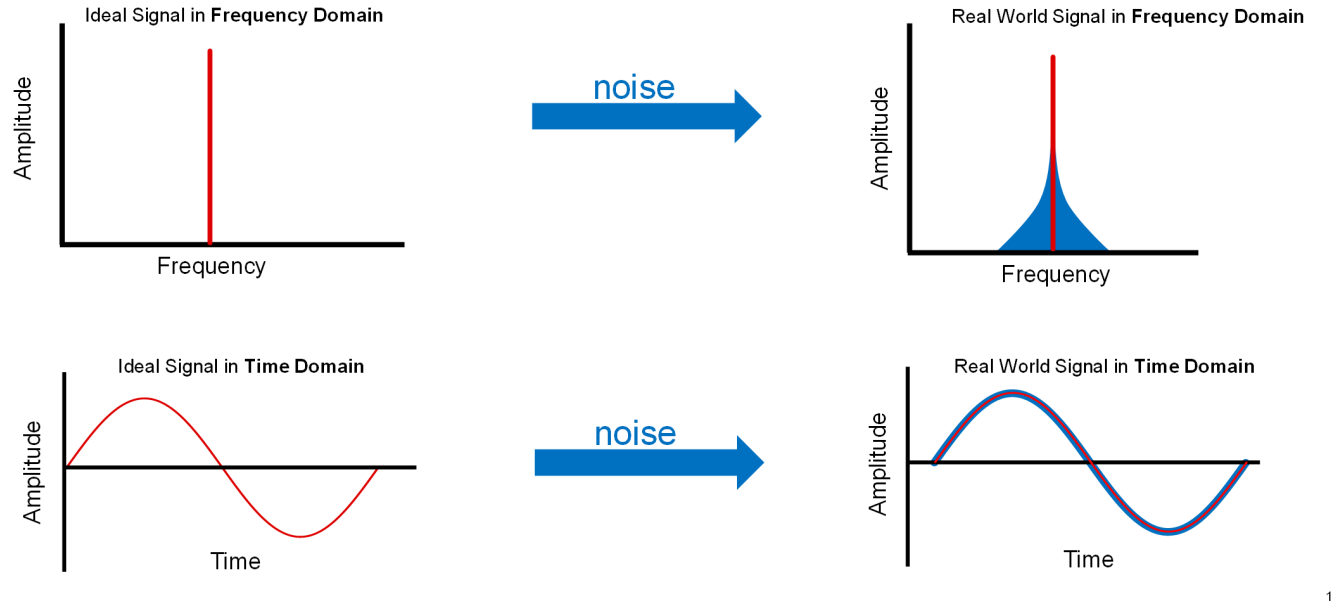

Figure 3. Phase Noise in the Frequency and Time Domain

Phase noise is defined by the ratio of noise (at an offset frequency from the oscillating signal, with a 1-Hz bandwidth) to the signal amplitude of the oscillating signal. Integrated noise is essentially the sum of all the phase noise within a defined range of offset frequencies from the oscillating signal (see Figure 4). Jitter is derived from Equation 2 using the integrated noise and the frequency of the signal:

$$t_{jitter} = \frac{\sqrt{integrated\ noise}}{2\pi f} \quad (2)$$

The integration range selected is important. This is determined by the sampling settings of the ADC. The bottom range (closer to the oscillating signal) is defined by half of [sampling rate] / [FFT size]. For example, at a sample rate of 2949.12 MHz and FFT size of 65536, the integration goes down to 22.5 kHz (see SLYT379 for more information). Thus, the lower this bottom of the integration range, the more the phase noise at lower offsets matter.

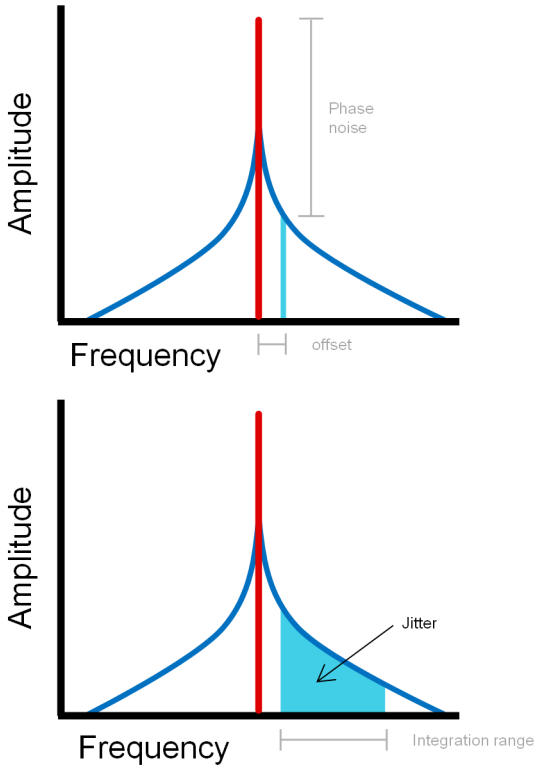

Figure 4. Phase Noise and Jitter Definitions

3 Designing for Lowest Jitter

Now we focus on how to get the lowest possible jitter on the ADC clock source. Figure 5 shows a phase noise plot with output frequency at 2949.12 MHz. The black line is the closed loop (locked) phase noise and the red is the open loop (free running VCO) phase noise. Also, the PLL noise is modeled by a flicker noise component (gray line) and a flat PLL noise floor component (blue line). The sum of the two lines is the PLL noise. The loop bandwidth (where the phase noise starts to roll off) is around 100-kHz offset. If this loop bandwidth is low, the VCO noise pushes into the lower offset phase noise, and if the loop bandwidth is high, it can push the PLL phase noise into the VCO region. Generally, to design a loop filter for the lowest jitter, the point where the PLL noise model intersects the VCO is the optimal point (around 120 kHz in this example). This loop bandwidth is determined by the loop filter components of a clocking source, or in this case, an RF synthesizer (integrated PLL + VCO).

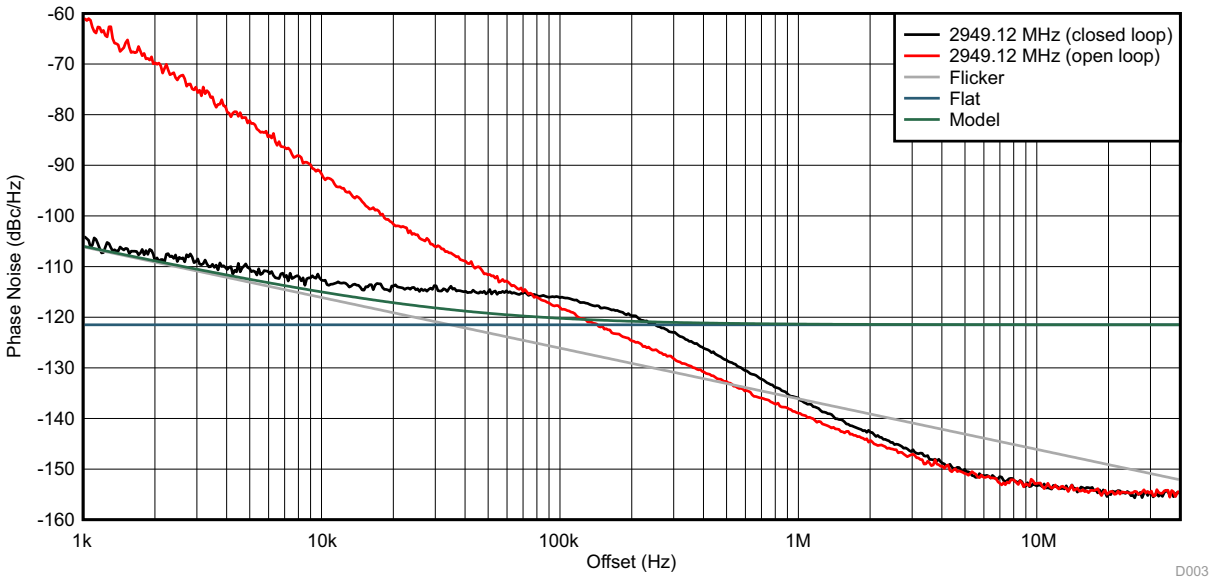

Figure 5. Sampling Clock of 2949.12 MHz With 58 fs Jitter

4 Factors Influencing Jitter

A phase noise of a synthesizer is mainly a combination of the *Phase Locked Loop* (PLL) and the *Voltage Controlled Oscillator* (VCO). The specification on datasheets that can tell you how low a jitter you are capable of achieving is the *Normalized PLL Noise Floor* (PLL Figure of Merit), *Normalized PLL Flicker Noise* (changes by 10 dB / dec), and VCO open-loop phase noise in data sheets. The PLL Figure of Merit and Flicker Noise are described in Equation 3 and Equation 4. From the relation seen in Equation 3, you can see that doubling f_{PD} essentially decreases the [20 × log] component by 6 dB and increases the [10 × log] component by 3 dB, so in total the overall PLL flat noise decreases by 3 dB. This is one of the aspects that improve the phase noise contributed by the PLL.

$$\text{PLL Flat Noise} = \left[\text{PLL Figure of Merit}\right] + 20 \times \log\left(\frac{f_{VCO}}{f_{PD}}\right) + 10 \times \log\left(f_{PD}\right) \quad (3)$$

where

- f_{PD} is the phase detector frequency of the synthesizer
- f_{VCO} is the voltage controlled oscillator frequency

$$\text{PLL Flicker Noise}\left(@\ f_{offset}\right) = \left[\text{Normalized PLL Flicker Noise}\right] + 20 \times \log\left(\frac{f_{VCO}}{1\,\text{GHz}}\right) - 10 \times \log\left(\frac{f_{offset}}{10\,\text{kHz}}\right) \quad (4)$$

In Figure 6, the black line is the original phase noise with a 58 fs jitter. But if the PLL phase noise is worse, as seen in the raised flat portion of the red line, the jitter can go up (78 fs in this example). The VCO phase noise also makes a big difference. Observe the gray line, a degraded VCO phase noise in this case, increased the jitter to 110 fs. By choosing a device that has good performance in both these areas and then designing the loop filter of the synthesizer well for the best phase noise response around the loop bandwidth, the lowest jitter can be optimized, providing the highest SNR clocking for the ADC.

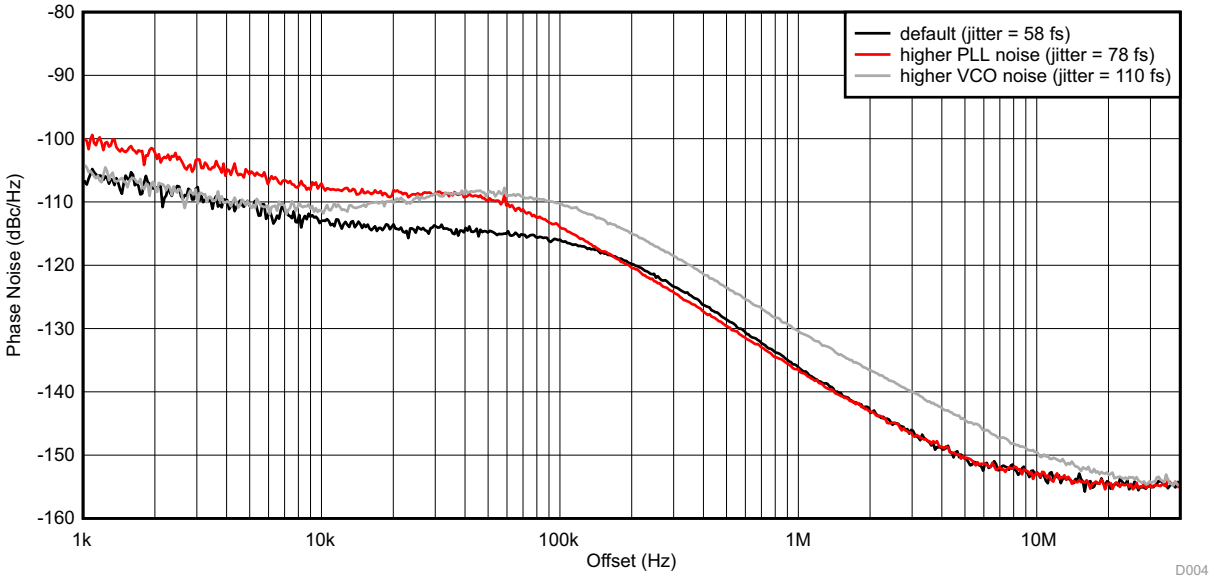

Figure 6. Phase Noise Contribution from PLL and VCO

There are also considerations for improving the jitter of the synthesizer in the signal amplitude, which affects the noise floor and thus the jitter caused by higher offsets. This behavior is observed through Leeson's equation, where the phase noise level floor level changes by output power with a factor (1 / Ps) of the signal source. At some point, the noise floor of the clock source will dominate and there is no further improvement (around 0 dBm from Figure 7). The clock source amplitude should be designed to be at least this level. Consequently, a synthesizer device with a very low noise floor as well as the capability of higher output power to reach this noise floor level is desired. As discussed in the earlier section of integration range for jitter, the higher the upper range, the more of this high offset phase noise will influence the overall jitter.

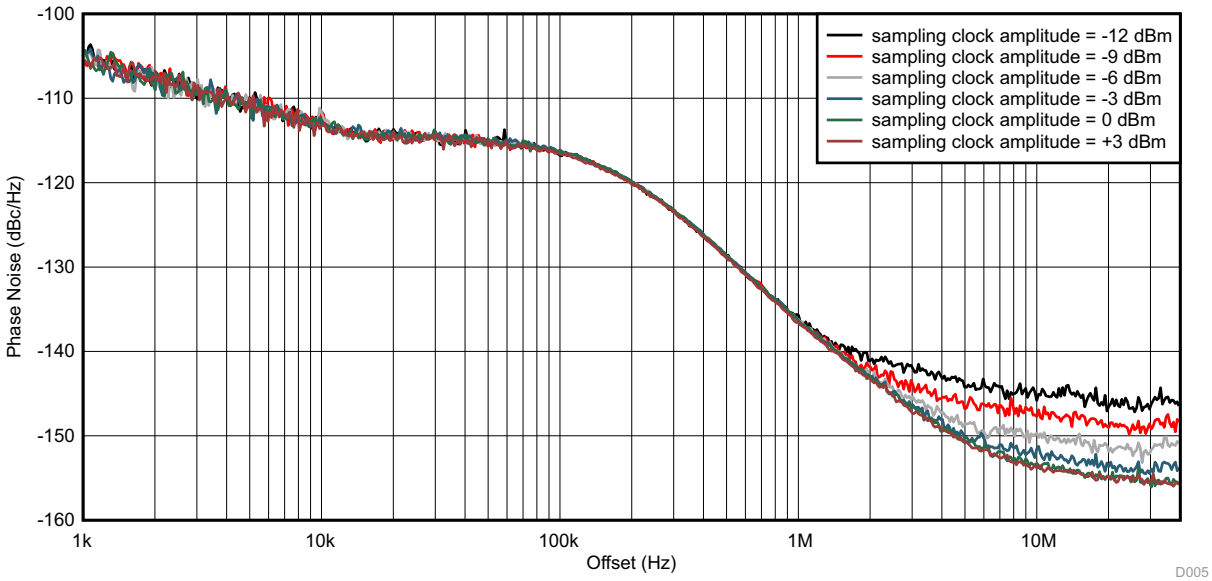

Figure 7. Sampling Clock Amplitude

5 References

- *LMX2582 High Performance, Wideband PLLatinum™ RF Synthesizer with Integrated VCO*, (SNAS680)
- *LMX2592 High Performance, Wideband PLLatinum™ RF Synthesizer with Integrated VCO*, (SNAS646)
- *ADC32RF45 Dual-Channel, 14-Bit, 3.0-GSPS, Analog-to-Digital Converter*, (SBAS747)
- *Optimal Clock Sources for GSPS ADCs Design Guide*, (TIDU870)
- *Maximizing SFDR Performance in the GSPS ADC: Spur Sources and Methods of Mitigation*, (SLAA617)
- *Clock Jitter Analyzed in the Time Domain, Part 1*, (SLYT379)
- *Clock Jitter Analyzed in the Time Domain, Part 2*, (SLYT389)
- *Clock Jitter Analyzed in the Time Domain, Part 3*, (SLYT422)
- *Direct RF Conversion: From Vision to Reality*, (SLYY068)

6 Related Web Sites

RF phase locked loops and synthesizers

- www.ti.com/product/LMX2582
- www.ti.com/product/LMX2592

TI Data Converters

www.ti.com/sc/device/ADC32RF45

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