TB-02 Digital Noise Reduction Techniques for COMBO II
Digital Noise Reduction Techniques for COMBO II™

INTRODUCTION

The COMBO II series of CODEC/Filter devices are highly integrated analog and digital systems on a single chip. Due to the high resolution and low noise requirements of the analog circuitry, care must be taken to minimize the effect of digital noise on analog performance. By understanding the potential problems and taking precautionary measures, the COMBO II will deliver the performance required for high quality voice transmission.

SOURCE OR NOISE

Digital noise is generated both externally and internally in a typical COMBO II application. Since this noise is at very high frequency, it may be under-sampled by the internal analog circuitry and show up as in-band noise or crosstalk.

EXTERNAL NOISE

The use of high speed digital circuitry on the line card produces high frequency noise on the +5V supply which is coupled into the analog circuitry by parasitic capacitances, device non-linearities and finite power supply rejection ratios of the amplifiers. This noise is mixed with the switching frequency of the switched capacitor clocks or the encoder or decoder clocks and may produce frequency components which lie within the voice band. There are a number of ways to minimize external digital noise corruption. First and foremost, 0.1 µF ceramic capacitors must be connected from VCC to GND near the COMBO II device and at each source of the digital noise. It is critical that the leads of the capacitors be kept to an absolute minimum. This means that the VCC and GND board traces from the COMBO II pins and those from the source of the noise meet at the capacitor through holes or solder pads as shown in Figure 1 below. Similar layout rules should be used for the bypass capacitors near the digital noise sources. Ideally the local bypass capacitor should supply all of the transient current required by its logic device.

FIGURE 1

Additionally, it can be useful to isolate the VCC traces to the COMBO II devices from those of the digital circuitry. This is easily accomplished by connecting an electrolytic capacitor (>10 µF) shunted by a 0.1 µF capacitor from VCC to GND near the card connector. The three VCC traces and the three GND traces going to the COMBO II devices, digital circuitry and the card connector should all emanate from the through hole or solder pads of the 0.1 µF capacitors as shown in Figure 2 below.

FIGURE 2

Another technique for reducing external digital noise on VCC is to further decouple the VCC by adding a small impedance, such as a resistor, in series with the COMBO II VCC trace on the backplane side of the 0.1 µF capacitor. There are potential problems with this approach in that, if the impedance is too large, the COMBO II’s supply may increase more slowly than that of the digital circuitry. This can result in COMBO II’s inputs going more positive than it’s VCC potential, increasing the chances of triggering latch-up as described in Technical Bulletin TB-1. A second potential problem is the reduction in the supply voltage at the COMBO II pins as the resistance increases, especially under heavy loading conditions. Generally the series resistance should not exceed 10Ω.

Generally there is far less noise on the VSS supply so simple bypassing with a 0.1 µF capacitor is sufficient. Decoupling VSS with a series resistor is not recommended since the impedance reduces the effectiveness of the Schottky clamping diode which should be connected between VSS and GND as described in TB-1. If decoupling is required, the Schottky diode must be connected on the device side of the impedance, in essence requiring a diode for each COMBO II device rather than one per board.

INTERNAL NOISE

The COMBO II CODEC/Filter are manufactured with National’s high density, high speed M2CMOS process. One characteristic of this process is high digital speeds which induce large current spikes on the power supply and ground lines. In particular, the DX0 or DX1 digital output drivers produce VCC and GND spikes when their outputs change state. These spikes may be sampled by internal analog circuitry and will produce in-band noise. For most parameters there is little effect, but for crosstalk from transmit to receive (CTXR), the effect can be quite large. Under worst case conditions, CTXR can be degraded to as low as 66 dB from a nominal 80 dB. In many applications this level of performance may be perfectly acceptable. In others, however, it may be marginal and methods must be considered for improving CTXR.

Three ways of reducing the effects of internally generated digital noise are: reduce the source of the noise, i.e., the
current spikes, reduce the resulting VCC noise caused by the spikes and, reduce the sensitivity of the device to the VCC noise.

REducing the Source of the Noise

The Dx0 and Dx1 output buffers have the largest effect on device noise performance, and as may be expected, Dx0 and Dx1 loading also has a significant effect. The worst case 66 dB CTXR is experienced with 200 pF on the Dx pin. Therefore, National recommends that, if CTXR levels of 66 dB are not acceptable, the capacitive loading of Dx0 and Dx1 be limited to about 50 pF.

Another technique which can be used in cases where heavy capacitive loading is unavoidable, is to use a small resistor (100Ω) in series with the Dx0 and Dx1 outputs. This reduces the magnitude of the current spikes. The effect of this impedance on timing is minimal but should be taken into account.

In the future, National plans to modify the Dx0 and Dx1 output drivers to reduce the cross-over supply spikes and to control the output dV/dt to reduce the spikes due to capacitive loading.

Reducing the Supply Noise Caused by the Spikes

To reduce the internally generated supply noise each COMBO II should have a 0.1 μF capacitor connected from VCC to GND as close as possible to the device pins. This is essentially the same precaution as recommended for externally generated digital noise, except the focus is on minimizing the distance from the device to the 0.1 μF bypass capacitor. Ideally it should be placed physically on the pins of the COMBO II device. The use of sockets moves the bypass capacitor physically further from the device, and therefore should be avoided. If absolutely necessary, low profile sockets (i.e. Augat) may be used with minimal degradation.

As discussed above, it is critical to minimize the distance and inductance from the device to the bypass capacitor. It follows that larger packages force the capacitor further from the device in the same way that sockets do. Therefore, if CTXR is a critical parameter, it is advisable to use the TP3070V (28-Pin PLCC) or the TP3071J or TP3071N (20-Pin DIP) devices in place of the TP3070U or TP3070N (28-Pin DIP).

Life Support Policy

National’s Products are not Authorized for Use as Critical Components in Life Support Devices or Systems Without the Express Written Approval of the President of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Beyond the precautions described above, additional steps can be taken to minimize performance degradation due to digital noise generated within the COMBO II device. The basic mechanism for the noise sensitivity is the sampling of spike noise produced by Dx0 and Dx1, referenced to BCLK, by analog switches which are referenced to MCLK. It would therefore be expected that the timing relationship between BCLK and MCLK would affect the sensitivity to spiking. This turns out to be the case and, unfortunately, the worst case relationship is when BCLK and MCLK are aligned or nearly aligned.

For best results the timing relationship between MCLK and BCLK should be such that MCLK precedes BCLK by 60 ns–80 ns. This ensures that the analog sampling is complete before digital spikes occur. Under this condition CTXR is typically greater that 80 dB while other timing can produce CTXR as low as 66 dB, especially when MCLK and BCLK are aligned or are nearly aligned as described above.

Near the worst case condition, CTXR measurements vary dramatically with only a few nanoseconds change in the timing between BCLK and MCLK. This results in a severe production problem due to lack of correlation from one reading to the next or from one test system to the next. For correlation and repeatability reasons, the COMBO II devices are tested to a 75 dB CTXR limit with 70 ns delay from MCLK rising edge to BCLK rising edge. This guarantees that the worst case crosstalk will be 66 dB providing “good” supply bypass and mounting techniques are used as discussed above. In the future, National will continue to reduce the sensitivity of the COMBO II to internally generate digital noise.

Summary

Several simple precautions were described which minimize the effects of digital noise on the transmission performance of the COMBO II family of CODEC/Filter devices. In most applications the performance far exceeds the requirements. In the future, improvements to the COMBO II family will further improve this performance.
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal and regulatory requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any damages arising out of the use of TI products in such automotive applications.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Audio</td>
<td>Communications and Telecom</td>
</tr>
<tr>
<td>Amplifiers</td>
<td>Computers and Peripherals</td>
</tr>
<tr>
<td>Data Converters</td>
<td>Consumer Electronics</td>
</tr>
<tr>
<td>DLP® Products</td>
<td>Energy and Lighting</td>
</tr>
<tr>
<td>DSP</td>
<td>Industrial</td>
</tr>
<tr>
<td>Clocks and Timers</td>
<td>Medical</td>
</tr>
<tr>
<td>Interface</td>
<td>Security</td>
</tr>
<tr>
<td>Logic</td>
<td>Space, Avionics and Defense</td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>Transportation and Automotive</td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>Video and Imaging</td>
</tr>
<tr>
<td>RFID</td>
<td></td>
</tr>
<tr>
<td>OMAP Mobile Processors</td>
<td><a href="http://www.ti.com/omap">www.ti.com/omap</a></td>
</tr>
<tr>
<td>Wireless Connectivity</td>
<td><a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a></td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated