DS3695, DS3695A, DS3695AT, DS3695T, DS96172, DS96174, DS96F172MQML, DS96F174MQML

Application Note 847 FAILSAFE Biasing of Differential Buses

Literature Number: SNLA031
FAILSAFE Biasing of Differential Buses

OVERVIEW
Multi-Point bus configurations present two potential problems to the system I/O designer that do not commonly occur in Point-to-Point configurations. The two problems that the I/O system designer should take into account are bus contentsions and the idle bus state. Bus contention occurs when more than one driver is active at a time during which the state of the bus is undetermined. Contentions may occur either by software or hardware errors. The second problem is an unknown bus state when all drivers are OFF. FAILSAFE biasing solves this problem by biasing the bus to a known state when ALL drivers are in TRI-STATE® (OFF). This application note is devoted to the topic of FAILSAFE biasing of differential buses.

INTRODUCTION
FAILSAFE biasing provides a known state when all drivers are in TRI-STATE (Hi-Z, OFF). This is especially important in bus configurations that employ more than one driver (transceiver), and is commonly known as a Multi-Point application (see Figure 2).

Electrical Characteristics Standard TIA/EIA-485 specifies that a maximum of 32 unit loads can be connected to a bus. A transceiver (driver/receiver pair) normally represents one unit load (see Figure 2). The bus is a half duplex bi-directional bus, (as data can flow in both directions), but only one driver should be active at a time. Termination is required (in most cases), and is only located at the two extreme ends of the bus. Note, that the termination shown on the left of Figure 1 also provides a FAILSAFE bias.

BUS STATES
A FAILSAFE biased bus has only two states, HIGH (driven HIGH and FAILSAFE HIGH) and LOW (neglecting the transition region, and bus contentsions). The bus can be driven HIGH or LOW by an active driver, or biased to a known state by external pull up and pull down resistors. These resistors provide the FAILSAFE bias, and the termination configuration is also known as a “power termination”. The two bus states are shown in Figure 2.

In some applications these two states are defined as MARK/SPACE, OFF/ON, or 1/0. The definition of the two states is application dependent. When the signal transitions through the threshold region (±200 mV) the output state of the receiver is undefined. In Figure 2, the line is driven LOW, transitions HIGH, then the driver is disabled. The bus however, remains HIGH due to external FAILSAFE biasing.

Without FAILSAFE biasing, the receiver output would be undefined when all drivers are OFF. The line would settle to only 1 mV–5 mV of each other (|VOA –V OB |, due to the internal input impedance network of the receiver), which is within the receiver’s threshold limits (≤200 mV). If external noise is coupled onto the line, a false transition could occur, causing an error. In an asynchronous application, this false transition could be interpreted as a framing error, false start bit, or cause a false interrupt.

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FIGURE 1. Typical Multi-Point Application
A popular format for low speed data transmission is an asynchronous protocol. A typical format is composed of 12 bits. The start bit initiates the timing sequence. This is detected by a transition from HIGH to LOW. Next are eight data bits, followed by an optional parity bit. Lastly, the line is driven HIGH for one or two bits (stop bits), signifying the end of the character. This format is illustrated in Figure 3. If another character is to be sent, the next start bit initiates the whole process all over again. However, if this was the last character, the line should remain HIGH until the next start bit, but the active driver is disabled. This presents a problem in multi-point applications, because between data transmissions all drivers are OFF. With no active drivers, the line is floating, and receiver outputs are undetermined. There are several solutions to this problem. One is through the use of alternate protocols (software), while the other is a hardware fix. The hardware fix uses external resistors to bias the line HIGH, when all drivers are off. The remainder of the application note describes the hardware method and the selection of component values.

In a Point-to-Point application (see Figure 4), the driver is normally always enabled. In this case the bus has only two states, driven HIGH, and driven LOW. FAILSAFE biasing is not needed, unless the driver's enabling pin is also switched.

### CALCULATING RESISTOR VALUES FOR FAILSAFE BIASING

The external resistors are selected such that they provide at least a 200 mV (maximum receiver threshold) bias across the line, and not substantially load down the active driver. In addition, the following guidelines should be met. The pull up resistor (Ra) and the pull down resistor (Rd) should be of equal value. This provides symmetrical loading for the driver. Termination resistor Rb should be selected such that it matches the characteristic impedance (Zc) of the twisted pair cable. The termination resistor matches the line, Rb = Zc, there will be no reflections. At the other end of the cable, the equivalent resistance of Rc, Ra and Rd should also match the characteristic impedance of the line. In this case Rc is in parallel with Ra plus Rd (Rc/(Ra + Rd)). For this equivalent resistance to be matched to the line Rc must be greater than Zc. Rc is typically 100–200 greater than Zc, but the actual value depends upon the values Ra and Rd. The FAILSAFE bias (Vfsb) is the potential dropped across the line. Note that this equation neglects cable resistance (see appendix), and that Rb is in parallel with Rc (Req = Rb // Rc). Therefore, the FAILSAFE bias is simply a voltage divider between Req, Ra, and Rd. The worst case occurs at Vcc − 5%, Ra and Rd ± % tolerance, and Rc and
Rb – % tolerance. Under the worst case conditions the FAILSAFE bias must be greater than 200 mV for the receiver output to be in a guaranteed state.

Example calculations for selecting FAILSAFE bias resistors:

Note: For this example assume the cable has a characteristic impedance (Zo) of 120Ω.

Step 1  Assume that Rc and Rb are equal and are selected to match Zo.
        Rc = Rb = Zo = 120Ω

Step 2  Calculate the equivalent resistance of Rc//Rb.
        Rc//Rb = 120Ω//120Ω = 60Ω

Step 3  Calculate the Pull up and Pull down resistor values knowing that the FAILSAFE bias is 200 mV, and VCC = 5V.

        Vfsb = VCC (Req/(Ra + Req + Rd))
        solving for R' (defined as Ra + Rd)
        R' = ((Req)VCC/Vfsb) – Req
        R' = ((60Ω)(5V/0.2V)) – 60Ω = 1440Ω

Since Ra and Rd are equal, Ra = Rd = 1440Ω/2 = 720Ω

Step 4  Recalculate the equivalent resistance of Rc//(Ra + Rd).
        Rc//(Ra + Rd) = 120Ω//(720Ω + 720Ω) = 110Ω

Since the equivalent resistance is close (within 10%) to the characteristic impedance of the cable (Zo), no further adjustment of resistor values is required.

However, for the perfectionist, the matched value of Rc can be calculated by setting the following equation to Zo and solving for Rc.

        Zo = Rc // (Ra + Rd)
        ∴ Rc = 131Ω

Now the equivalent resistance (Req = Rc // Rb) becomes 131Ω // 120Ω = 62Ω, which is very close to the original 60Ω. Standard value resistors values can be substituted to ease resistor selection, availability, and cost, before recalculating the FAILSAFE bias potential. Using a 5% tolerance table we find the following standard resistor values:

- Ra = 750Ω, Rb = 120Ω, Rc = 130Ω, Rd = 750Ω

In order to verify that the selected values meet the criteria the following calculations should be completed:

1. Rc//(Ra + Rd) = Zo
   120Ω/(750Ω + 750Ω) = 120Ω

2. Req = Rb//Rc
   120Ω/130Ω = 62Ω

3. Vfsb = VCC (Req/(Ra + Req + Rd))
   5V(62Ω/(750Ω + 62Ω + 750Ω)) = 200 mV

Based on the example shown above, and a twisted pair cable with characteristic impedance of 120Ω, it has been determined that a 750Ω pull up and pull down resistor will provide a FAILSAFE bias of 200 mV. This value could be decreased slightly to provide a greater bias (>200 mV), and to meet the worst case power supply and resistor tolerance conditions. However, the value of Ra and Rd should not be reduced too low in order to minimize loading seen by the driver. This example illustrated that the largest values used for the pull up (Ra) and pull down (Rd) resistors should be 750Ω. The pull resistors should not be decreased substantially. Because when the driver is active (ON), it is required to develop a minimum of 1.5V across the cable termination.

Using low impedance pull resistors further loads down the driver, making the 1.5V differential voltage even more difficult to meet.

Figure 6 illustrates the fully loaded (32 unit loads) TIA/EIA-485 bus with an external FAILSAFE bias network. Note that the FAILSAFE bias (Power Termination) is only located at one end of the bus. The other end employs a single resistor termination. The power termination is commonly located on the Master node of a Master/Slave bus configuration. This assures that the power to the pull up resistor is always on.

Before looking at the driver’s load, the receiver’s input impedance needs to be modeled to understand its effect upon the driver. The TIA/EIA-485 standard specifies a high receiver input impedance and an Input Voltage vs Input Current curve. An input impedance of 12 kΩ or greater is typically required to meet the Vx/Ix curve. A common mistake is to model the receiver’s input impedance as a differential resistance, which is seen between the input pins. The input resistance is correctly modeled as a series resistor to a voltage reference node (AC ground point). The TIA/EIA-485 standard also allows for 32 unit loads to be connected in parallel. Therefore, the driver could see 32 12 kΩ resistors in parallel on each line. This is equivalent to a 375Ω resistor to an internal voltage reference point.
The test circuit shown in Figure 7 models the fully loaded TIA/EIA-485 bus. The 375Ω resistors that model the 32 parallel receiver input impedances, have been changed to 330Ω for two reasons. First, an active driver would also see 31 tri-stated driver leakage currents (I_{OZ}), which is equivalent to 31 times 100 µA or 3.1 mA. This is equivalent to roughly 3 more unit loads. Therefore, 12 kΩ divided by 35(32 + 3) equals 342Ω. This value is further reduced to 330Ω to select standard value resistors. The dashed box represents 32 receiver loads and 31 passive driver leakage loads. The V_{CM}

power supply models the maximum ground shifting specified (allowed) by TIA/EIA-485 (±7V). The differential voltage (VOD), measured across the 62Ω load (120Ω/130Ω), is required to be greater than 1.5V in magnitude by TIA/EIA-485. Test data taken on three popular National TIA/EIA-485 drivers are shown in Table I. With the common mode voltage varied from −7V to +7V, all of the devices meet the 1.5V minimum differential voltage (VOD column).
<table>
<thead>
<tr>
<th>Device</th>
<th>( V_{CM} ) (V)</th>
<th>( I_- ) (mA)</th>
<th>( I_+ ) (mA)</th>
<th>( V_- ) (V)</th>
<th>( V_+ ) (V)</th>
<th>( VOD ) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS3695</td>
<td>0</td>
<td>-41.7</td>
<td>+38.4</td>
<td>3.39</td>
<td>1.44</td>
<td>1.95</td>
</tr>
<tr>
<td></td>
<td>-7</td>
<td>-56.1</td>
<td>+23.5</td>
<td>3.18</td>
<td>1.24</td>
<td>1.94</td>
</tr>
<tr>
<td></td>
<td>+7</td>
<td>-13.4</td>
<td>+69.1</td>
<td>3.78</td>
<td>1.77</td>
<td>2.01</td>
</tr>
<tr>
<td>DS96172/4</td>
<td>0</td>
<td>-43.4</td>
<td>+42.4</td>
<td>3.25</td>
<td>1.14</td>
<td>2.11</td>
</tr>
<tr>
<td></td>
<td>-7</td>
<td>-59.6</td>
<td>+28.0</td>
<td>3.08</td>
<td>0.94</td>
<td>2.14</td>
</tr>
<tr>
<td></td>
<td>+7</td>
<td>-12.0</td>
<td>+70.4</td>
<td>3.47</td>
<td>1.46</td>
<td>2.01</td>
</tr>
<tr>
<td>DS96F172/4</td>
<td>0</td>
<td>-49.5</td>
<td>+45.3</td>
<td>3.67</td>
<td>1.33</td>
<td>2.34</td>
</tr>
<tr>
<td></td>
<td>-7</td>
<td>-63.5</td>
<td>+30.6</td>
<td>3.47</td>
<td>1.14</td>
<td>2.33</td>
</tr>
<tr>
<td></td>
<td>+7</td>
<td>-19.2</td>
<td>+74.2</td>
<td>4.00</td>
<td>1.71</td>
<td>2.29</td>
</tr>
</tbody>
</table>

Note 1: Current into device pin is defined as positive, current out of device pin is defined as negative. \( VOD \geq 1.5V \) (TIA/EIA-485).

**OPEN INPUT FAILSAFE FEATURE**

All of National’s TIA/EIA-485 receivers support the OPEN INPUT FAILSAFE feature. This feature provides a known state (HIGH) on the receiver output for the following cases, which are illustrated in Figure 8. The OPEN INPUT FAILSAFE feature is integrated into the input stage of the device. Normally high value (typically 120 kΩ) bias resistors pull the plus input high, and the minus input low. The value is large enough to properly bias the receiver when the inputs are open (non-terminated).

**VALID OPEN INPUT CASES:**

A. Uterminated Cables—With restrictions on data rate, stub length, and cable length, it is possible to construct an interface without termination resistors. Normally the cable length is very short with respect to the driver’s rise time and the reflections that occur die out long before the next transition. For the idle line, the impedance seen across the receiver input pins is very large (open) and thus the receiver output will be a HIGH state.

B. Unconnected Nodes—In a Multi-Point configuration, up to 32 nodes can be connected to the twisted pair. Termination should only be located at the two extreme ends of the cable. Therefore, if a middle node is disconnected from the cable, the OPEN INPUT FAILSAFE feature will put the receiver output into a stable HIGH state.

C. Unused Channels—If a high integration receiver IC (multi-channel) is being used, and all channels are not required, the unused channel(s) inputs can be left as no-connects. The OPEN INPUT FAILSAFE feature will force the unused channel into a stable HIGH state. This prevents the unused channel picking up external noise and oscillating, thereby increasing the power supply current (I_{cc}).

In all three cases, the impedance seen across the receiver input pins is very large or open, \((\infty)\) in contrast to a low impedance termination resistor of 150Ω or less. For these cases the receiver output will be HIGH. If the termination resistors were connected across the receiver input pins, then the receiver output is undetermined, unless the bus employs FAILSAFE biasing resistors.

**SUMMARY**

External FAILSAFE bias resistors can be used to solve the idle line state problem that commonly occurs in Multi-Point applications using asynchronous protocols. This is a well accepted hardware approach to solving the idle line state problem. In fact many complete INTERFACE standards have accepted this method. Examples include the Differential SCSI-1 and 2 (Small Computer System Interface) specifications, as well as the IPI (Intelligent Peripheral Interface) standard. This application note provides guidance to selecting properistor values that will provide an adequate FAILSAFE bias (V_{f}{\text{s}}b) while minimizing the loading effect on the driver.

**FIGURE 8. Applications of OPEN INPUT FAILSAFE Feature**

![Figure 8](image-url)
APPENDIX

A more elaborate calculation that takes into account the DC resistance of the twisted pair cable is provided in this appendix. (See Figure 9). For this example assume the following:

- \( R_a \) = Pull Up Resistor
- \( R_b \) = Slave End Cable Termination Resistor
- \( R_c \) = Master End Cable Termination Resistor
- \( R_d \) = Pull Down Resistor
- \( R_t \) = Cable DC Resistance
- \( R_{dcr} \) = \( R_e + R_f \)
- \( V_{fsbm} \) = FAILSAFE Bias Potential @ Master end of cable
- \( V_{fsbs} \) = FAILSAFE Bias Potential @ Slave end of cable

and

1. \( R_a = R_d \) for symmetrical loading
2. \( \text{REQ} = \frac{R_c((R_a + R_d))}{(R_a + R_c + R_d)} \)

Note 2: Assume \( V_{CC} = 5V \pm 5\% \).

Note 3: Resistor Tolerance = \( \pm 2\% \).

Note 4: Worst Case occurs at \( V_{CC} \) – 5\%, \( R_a \) and \( R_d \) + 2\%, \( R_b \) and \( R_c \) – 2\%.

The FAILSAFE Bias at the Slave end is simply a voltage divider between the cable DC resistance and the Slave end termination resistor.

\[ V_{fsbs} = \frac{R_b}{R_b + R_{dcr}} V_{fsbm} \]

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