

## **DP83822 Low Power Modes**

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### **ABSTRACT**

This application note will discuss how the DP83822 low power modes work and how to implement each mode. For information regarding expected power consumption, please see the DP83822 Datasheet.

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## 1 Introduction

The DP83822 10/100 Mbps Industrial Ethernet PHY offers a wide range of power saving modes that can be applied individually or in combination with each other depending on the desired operation.

Supported low power modes include:

- Energy Efficient Ethernet – IEEE802.3az
- Wake-on-LAN
  - Magic Packet Detection
  - Magic Packet Detection with Secure-ON
  - Custom Packet Detection
- Low Power Sleep Modes
  - Passive Sleep
  - Active Sleep
- IEEE Power Down
- Deep Power Down

For this application note Passive Sleep, Active Sleep, IEEE Power Down and Deep Power Down will be discussed.

**Table 1. Terminology**

Acronym	Definition
DUT	Device Under Test
EEE	Energy Efficient Ethernet
WoL	Wake-on-LAN
PHY	Physical Layer Transceiver
SMI	Serial Management Interface
NLP	Normal Link Pulse
TX	Transmit – Digital Pins
RX	Receive – Digital Pins
TD	Transmit – Analog Pins
RD	Receive – Analog Pins

## 2 Low Power Sleep Modes

There are two low power sleep modes supported by the DP83822: Active Sleep and Passive Sleep.

This section discusses the principles behind Active/Passive Sleep and implementation of Active/Passive Sleep.

### 2.1 Active Sleep – Principles of Operation

When the DP83822 enters into Active Sleep mode, all internal circuitry is shut-down in the PHY except for the SMI and energy detection circuitry on the TD± and RD± pins. In this mode, the DP83822 sends out NLPs every 1.4 seconds to wake up the link partner. Automatic power-up occurs when a link partner is detected.

### 2.2 Active Sleep – Implementation

Active Sleep is enabled by setting bits[14:12] = 0b110 in the PHY Specific Control Register (PHYSCR, address 0x0011).

### **2.3 Passive Sleep – Principles of Operation**

When the DP83822 enters into Passive Sleep mode, all internal circuitry is shut-down in the PHY except for the SMI and energy detection circuitry on the TD± and RD± pins. In this mode, the DP83822 will automatically power-up when a link partner is detected. No transmission of NLPs occurs in this mode of operation.

### **2.4 Passive Sleep – Implementation**

Passive Sleep is enabled by setting bits[14:12] = 0b111 in the PHY Specific Control Register (PHYSCR, address 0x0011).

## **3 IEEE Power Down**

This section discusses the principles behind IEEE Power Down and implementation of IEEE Power Down.

### **3.1 IEEE Power Down – Principles of Operation**

IEEE Power Down shuts down all PHY circuitry except the SMI and internal clock circuitry.

### **3.2 IEEE Power Down – Implementation**

IEEE Power Down can be activated by either register access or through the INT/PWDN\_N pin when the pin is configured for power-down function.

To enable IEEE Power Down via INT/PWDN\_N pin, the pin will need to be driven LOW to ground.

To enable IEEE Power Down via the SMI, set bit[11] = 1 in the Basic Mode Control Register (BMCR, address 0x0000).

## **4 Deep Power Down**

This section discusses the principles behind Deep Power Down and implementation of Deep Power Down.

### **4.1 Deep Power Down – Principles of Operation**

Deep Power Down shuts down all PHY circuitry except the SMI. In this mode, the PHY PLL is shut-down to further reduce power consumption.

### **4.2 Deep Power Down – Implementation**

Deep Power Down is activated by first enabling IEEE Power Down (from either the SMI or INT/PWDN\_N pin) and then setting bit[2] = 1 in the Deep Power Down Control Register (DPDWN, address 0x0428).

## **5 Conclusion**

This application note provided details on the principles behind each low power mode and the mechanisms to enable each low power mode in the DP83822.

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