AN-984 Power and Thermal Considerations for High Speed Clock Generators
Power and Thermal Considerations for High-Speed Clock Generators

INTRODUCTION
As today’s systems are operating at higher speeds and getting more portable than ever before, figuring the exact amount of the power consumed by them is becoming more critical. More accurate power calculations not only helps for optimized design of power supplies and fans, but also helps to better predict the long term reliability of systems.

Power consumption calculations, if not ignored, have been mostly an art rather than a science for most system designers. There are relatively accurate methods of determining how much power any given component consumes within a system, but due to many first order approximations the amount of the total power consumed becomes less accurate and meaningful. This inaccuracy forces the designers to use large safety factors (margins) when determining the requirements for their power supplies and fans.

Below is a brief discussion on how to calculate the power consumed under dynamic conditions for any given device. Once this value is determined for all the components in a system, other design parameters such as the power supply ratings, airflow and even the system’s failure rate can be better predicted.

In order to look at these components closely, one must look at all the possible sources of power consumption which can be summed as the following:

1. Power consumed by the loads. This power is significant under dynamic conditions and it depends on the loads, voltage swings as well as the toggle frequency of each output.

2. Power consumed due to the internal capacitance of the device, or commonly known as the Cpd. This type of power consumption is often associated with CMOS technology devices rather than bipolar due to their inherently capacitive structures, and higher voltage swings.

This power includes what is drawn from the power supply due to the instantaneous current spikes during output switching. This component is mostly present in CMOS devices since during output transitions, there will be a direct path from the supply to ground.

3. Input leakage power. This source of power consumption is often ignored in most calculations due to the very small amount of input leakage currents in CMOS devices.

These sources are present on all devices. However, depending on the process technology, some of these sources may have a very small effect on the total power consumed. In addition to the technology, loads, frequency of the operation as well as the supply voltage play major roles on how much power is dissipated within each integrated circuit.

THE FORMULA

In an attempt to put all of it together, the following formula can describe the power consumed across any given device:

\[ P_{\text{Total}} = P_{\text{Static}} + P_{\text{Dynamic}} \]

where;

\[ P_{\text{Static}} = (V_{\text{CC}}) \cdot (I_{\text{CC}} \cdot \text{Duty Cycle}) \]

\[ + \left( (V_{\text{CC}} \cdot I_{\text{OL}} \cdot \text{DC}_{\text{LO}}) \cdot n \right) \]

\[ + \left( (I_{\text{OH}} \cdot V_{\text{OL}} \cdot \text{DC}_{\text{LO}}) \right) \]

where DC is the duty cycle and n is number of inputs.

Next is the dynamic power consumed, which as mentioned before, has more than one component and can be given by;

\[ P_{\text{Dynamic}} = \sum (P_{\text{Load}} + P_{\text{Cpd}} + P_{\text{Input}}) \]

Let us look at each component separately. \( P_{\text{Load}} \), or the power consumed across the loads can be derived from the fact that the current through a capacitive load can be given by:

\[ I_{\text{Load}} = C_{\text{Load}} \cdot (dV/dt) \]

where d\( \text{V} \) is the voltage swing across the capacitor \((V_{\text{swing}})\) and dt is the unit of time which is equal to the frequency. Therefore

\[ I_{\text{Load}} = C_{\text{Load}} \cdot V_{\text{swing}}(\text{Load}) \cdot f \]
The reason for such an easy transformation is the fact that the amount of the energy dissipated across the capacitor remains the same no matter how fast or slow it is being charged or discharged. Also since power is the product of current and voltage, the load power becomes:

\[ P_{\text{Load}} = \Sigma (C_{\text{Load}} * (V_{\text{swing}(\text{Loads})} * V_{\text{CC}}) * f) \]

Given that different outputs may be operating at different frequencies, as is most often the case for clock generators, while each one driving a different load, the total load power must be rewritten as the sum of the power consumed across every output, as given below:

\[ P_{\text{Load}} = \Sigma (C_{\text{Load}} * (V_{\text{swing}(\text{Loads})} * V_{\text{CC}}) * f) \]

The next component is the power dissipated due to the internal capacitance of the device. This is also known as the \( C_{pd} \) power which comes from the fact that every device has some internal nodal capacitance which is being charged and discharged at a rate equal or below the highest frequency of the operation. Calculating this power is more important in CMOS devices since its transistors are voltage activated compared to bipolar technologies that are current activated.

This portion of the consumed power can also be written as:

\[ P_{Cpd} = C_{pd} * V_{\text{swing}} * V_{\text{CC}} * f \]

Where \( f \) is highest frequency of operating.

The critical parameter in this equation is the actual value for this internal capacitance \( C_{pd} \). This is due to the fact that \( C_{pd} \) is a function of the frequency and is mostly a measured value.

While JEDEC Standard Committee suggests measurement of this parameter at 1 MHz, some I.C. suppliers can provide plots of this parameter across frequency which helps for more accurate calculations.

Plot 1 is an example of \( C_{pd} \) across frequency for two CGS devices. CGS74B304 is a bipolar octal-divide-by-two buffer while CGS74CT2524 is a quad CMOS driver. Notice the difference between the value of this internal capacitance for Bipolar and CMOS devices across frequency.

Nevertheless, the formula to calculate this power is very similar to the load equation formula where:

\[ P_{\text{Input}} = \Sigma C_{\text{Input}} * V_{\text{swing} \text{input}} * V_{\text{swing} \text{input}} * f \]

For inputs toggling at frequency \( f \). For most practical purposes this component of the total power is often ignored due to its small size which could be about 1 percent of the whole power consumed.

So what does it all mean? What follows are some typical examples of power calculations for comparison across different device technologies. What must be kept in mind is the fact there still exists some margin of inaccuracy and the system designers need to use a guardband of no less than 5% for obtaining the total power consumed within each unit.

**Bipolar** technologies often have much lower internal power dissipation capacitance due to the fact that they use current for biasing as opposed to voltage, as is the case in CMOS devices. This causes the \( C_{pd} \) to be less a function of frequency (as in the Plot 1). In addition, the voltage swings are no more than one \( V_{be} \) for most of the nodes. Therefore, the majority of the consumed power can be found in the supply current as well as the output loads. The total power equation can be written as:

\[ P_{\text{Total}} = \Sigma (P_{\text{Load}} + P_{Cpd}) + P_{\text{Static}} \]

where;

\[ P_{\text{Static}} = (V_{\text{CC}}) * (I_{\text{CC (quiescent)}}) + (R_{\text{LO}} * V_{\text{OL}} + D_{\text{LO}}) + (R_{\text{OH}} * V_{\text{OH}} + D_{\text{OH}}) \]

\[ P_{\text{Total}} = \Sigma (C_{\text{Load}} * V_{\text{swing}} * V_{\text{CC}} * f) \]

\[ P_{Cpd} = C_{pd} * V_{\text{be}} * V_{\text{CC}} * f \]

Here, again \( C_{pd} \) must be provided by the manufacturer, while the rest of the parameters in the equation above are under the designer’s control.

The \( V_{\text{swing}} \) (voltage swing across each output) needs to be calculated and it will depend on design parameters such as the termination scheme used as well as the output buffer characteristics. Below is an example of such a calculation. Here the \( V_{\text{swing}} \) is the actual voltage swing on each output, and it equals to:

\[ V_{\text{swing}} = (V_{\text{HIGH}} - V_{\text{LOW}}) \]

where;

\[ V_{\text{HIGH}} = (V_{\text{CC}} - 2V_{\text{be}}) \]

\[ V_{\text{LOW}} = V_{\text{OL}} \]

Let’s use the CGS74B304 device as an example. In order to avoid any reflections and violation of output drive capabilities (\( \text{I}_{\text{OH}}/\text{I}_{\text{OL}} \)), we will terminate with an equivalent of 200Ω pull-up and 150Ω pull-down resistors.

![FIGURE 1. Calculating Vswing for a Bipolar IC](image-url)
Also, we will use a 50 pF capacitive load while driving a
100MHz line and operating at 5.0V VCC with 50% duty cycle
input running at 100 MHz (outputs of 50 MHz).
We get;
\[ P_{Static} = (5.0V) \times ((20 + 42)/2) \, mA \]
\[ = 155 \, mW \] for supply bias,
and as for the terminations;
\[ = (I_{OL} \times V_{OL} \times DC_{OL}) \]
\[ + (I_{OH} \times V_{OH} \times DC_{OH}) \]
\[ = ((V_{CC} - V_{OL})/R_{pd}) \times V_{OL} \times DC \]
\[ + ((V_{OL}/R_{pd}) \times V_{OH} \times DC) \]
\[ = (((5.0 - 0.4)/200) \times 0.4 \times 0.5) \]
\[ + ((3.6/100) \times 3.6 \times 0.5) \]
\[ = 4.6 + 64.8 \, mW \] per output
so the total static load becomes;
\[ P_{Static} = 155 + 8 \times (69.4) = 710 \, mW \]
and for the dynamic portion
\[ P_{Cpd} = 20 \, pF \times 0.7V \times 5.0V \times 50 \, MHz \]
\[ = 3.5 \, mW \]
also for the loads,
\[ V_{(HIGH)} = (5.0 - 1.4) \, V = 3.6V \]
and
\[ V_{(LOW)} = 0.5V \]
so the average swing voltage becomes;
\[ V_{swing} = (3.6 - 0.5) \times 3.1V \]
So the total load power becomes;
\[ P_{Load} = \Sigma (C_{Load} \times V_{swing} \times V_{CC} \times f) \]
\[ = 8 \times (50 \, pF \times 3.1 \times 5.0V \times 50 \, MHz) \]
\[ = 310 \, mW \]
And ignoring the input dissipation, the total power con-
sumed becomes;
\[ P_{Total} = (\Sigma P_{Load} + P_{Cpd}) + P_{Static} \]
\[ = 710 + 3.5 + 310 = 1024 \, mW \]
The case is a bit simpler for CMOS devices. Here again for
the ease of calculation we will ignore the power that is con-
sumed due to the output rise and fall transitions as well as
the input leakage current.
What makes CMOS device power consumption easier than
dynamic is the fact that Vswing is actually from supply to
ground, that is approximately 5.0V for a CMOS device oper-
ating at 5V VCC. So the total power equation can be written as;
\[ P_{Total} = (\Sigma P_{Load} + P_{Cpd}) + P_{Static} \]
where
\[ P_{Load} = \Sigma (C_{Load} \times V_{CC} \times V_{CC} \times f) \]
and
\[ P_{Cpd} = C_{pd} \times V_{CC} \times V_{CC} \times f \]
so the whole equation for a device with all outputs operating
at the same frequency and driving identical loads can be writ-
ten as
\[ P_{Total} = (I_{Total \, load} \times C_{pd} \times (V_{CC})^2 \times f) \]
\[ + V_{CC} \times I_{CC} \times \text{(quiescent)} \]
\[ + (I_{OL} \times V_{OL} \times DC_{OL}) \]
\[ + (I_{OH} \times V_{OH} \times DC_{OH}) \]
\[ + ((V_{CC}) \times (I_{CC}) \times DC_{pd}) \times n \]
As an example we will use the CGS74CT2524 which is a 1-4
TTL compatible CMOS clock driver. For comparison we use
the same frequencies and loads. That is a 50 MHz input
signal with 50% duty cycle driving 50 pF of load per output
at 5.0V VCC. The total power consumed will be
\[ P_{Total} = ((4 * 50) + 140) \, pF \times ((5.0 \times 5.0) \times 50 \, MHz \]
\[ + 80 \, \mu A \times 5.0V \]
\[ + 4 \times (4.9/200) \times 0.1V \times 0.5 \]
\[ + 4 \times (4.9/100) \times 4.5V \times 0.5 \]
\[ + 1 \times 5.0V \times 1.5 \, mA \times 0.5 \]
\[ = 875 \, mW \]
Although the power consumption between these two cases
appear to differ drastically, we must note that in the CMOS
case we were only driving four outputs versus the eight
used in the B304. If this would have been the case, con-
sumed power would have been;
\[ P_{Total} = (8 \times 50) + 280 \, pF \times ((5.0 \times 5.0) \times 50 \, MHz \]
\[ + 190 \, \mu A \times 5.0V \]
\[ + 8 \times (4.9/200) \times 0.1V \times 0.5 \]
\[ + 8 \times (4.9/100) \times 4.5V \times 0.5 \]
\[ + 1 \times 5.0V \times 1.5 \, mA \times 0.5 \]
\[ = 1746 \, mW \]
In addition, as the toggle frequency increases from 50 MHz
the Cpd value increases more in the CMOS versus the Bipoi-
lar device which remain relatively flat until it seizes to func-
tion properly (refer to Plot 1 and the datasheets for the
specified maximum frequency of the operation).
ECL devices typically consume less current compared to
other technologies as the frequency of the operation reach-
es 100 MHz or beyond. This is due to the fact that in this
technology the transistors do not turn-on completely, and
this allows for design which use a lower internal voltage
"swing".
Additionally, ECL which is another bipolar technology has
less junction or internal capacitance compared to CMOS
devices.
These lower voltage swings, along with lower junction cap-
acitance helps to minimize if not eliminate the dynamic
power consumed due to Cpd.
Since the transistors are either completely turned off or are
operating in the active region, no simultaneous switching
transitions exist from the supply to ground (no power
consumed due to outputs \\text{transitions}).
The critical power component in ECL devices is the power
consumed due to the termination network. Most, if not all
ECL devices require termination networks to minimize signal
reflections as well as getting more predictable DC levels.
The total power consumption formula in the case of the ECL
device scan be written as;
\[ P_{Total} = \Sigma P_{Load} + P_{Static} \]
It can also be written as;
\[ P_{Total} = \Sigma (I_{AVG} \times V_{AVG}) + I_{CC} \times V_{EE} \]
where I_{AVG} is the average current through each output and
V_{AVG} is the average output voltage. Figure 2, below, is an
example of such calculation for an output terminated in parallel
to \\text{VEE}. 

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FIGURE 2. Power Calculations for Parallel Terminated, Single-Ended ECL Device

With a $V_{OH}$ of $-1.035\,\text{V}$ and $V_{OL}$ of $-1.610\,\text{V}$:

\[
I_{AVG} = \frac{1}{50} \left( (-1.035 - (-2.0))/50 + (-1.610 - (-2.0))/50 \right) / 2
\]

\[
I_{AVG} = 14.0\,\text{mA}
\]

\[
V_{AVG} = \frac{1}{2} \left( 1.035 + (-1.610)/2 - 1.3\,\text{V} \right)
\]

Using different termination schemes changes this consumed power. Table I reflects the amount of the current as well as power used per output for thevenin equivalent termination as shown below in Figure 3.

![Figure 3](image)

FIGURE 3. Power Calculations for a Thevenin Equivalent Termination

TABLE I. Comparison of Power Dissipation across Different Termination Resistors

<table>
<thead>
<tr>
<th>$R_T$</th>
<th>$R_1$</th>
<th>$R_2$</th>
<th>$I_{EE,\text{avg}}$</th>
<th>$P_{D,\text{avg}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>90</td>
<td>113</td>
<td>28.2</td>
<td>109</td>
</tr>
<tr>
<td>62</td>
<td>112</td>
<td>140</td>
<td>22.7</td>
<td>87.9</td>
</tr>
<tr>
<td>75</td>
<td>135</td>
<td>169</td>
<td>18.8</td>
<td>72.7</td>
</tr>
<tr>
<td>82</td>
<td>148</td>
<td>185</td>
<td>17.2</td>
<td>66.5</td>
</tr>
<tr>
<td>90</td>
<td>162</td>
<td>203</td>
<td>15.7</td>
<td>60.5</td>
</tr>
<tr>
<td>100</td>
<td>180</td>
<td>225</td>
<td>14.1</td>
<td>54.5</td>
</tr>
<tr>
<td>120</td>
<td>216</td>
<td>270</td>
<td>11.7</td>
<td>45.4</td>
</tr>
<tr>
<td>150</td>
<td>270</td>
<td>338</td>
<td>9.4</td>
<td>36.3</td>
</tr>
</tbody>
</table>

The case for MIXED SIGNALS is a bit more complicated since in most instances both CMOS and Bipolar characteristics are present. Generally Mixed signals are designed such that they use both CMOS and Bipolar internal circuitry for optimizing speed and geometry, while the outputs are mainly of CMOS structure to make them compatible with the outside world.

However, the generic formula can be applied in this case as well, provided that all components of the power equation are calculated and accounted for.

POWER AND TECHNOLOGY

The examples provided previously show that the power consumption is about the same at 50 MHz and 50 pF loads. Hence the designer can look for other factors such as cost, ease of design, and the availability of components.

However, as the frequency and loads increase, the power dissipation does not remain the same across different technologies. The general rule is that CMOS devices consume more power than Bipolar technology as the frequency increases while ECL’s power consumption remains relatively flat given the same operating conditions.

For this reason, ECL is the recommended technology quite often as frequencies reach beyond 100 MHz. But due to the fact that not many components need to operate above and beyond this range, designing a few ECL units on boards populated with CMOS and or Bipolar devices becomes cumbersome and difficult. This makes ECL, an acceptable solution once all the components being used on the board are such. As for Bipolar or CMOS, the choices are about the same, except that in many instances CMOS is easier to design with as well as cheaper to manufacture. For this reason CMOS has become the technology of choice for many clock generators. However this paradigm needs to be reviewed due to higher operating frequencies of today’s systems. Technologies such as GTL (Gunning Transistor Logic) and or LVDS (Low Voltage Differential Signaling) which are bipolar in core, are gaining some attention due to their better noise margins as well as higher bandwidths.

THERMAL CALCULATIONS

OK, so now we know the total amount of power dissipated within each of our components and throughout the boards, and have designed the optimum power supply for the system. Problems such as the long term reliability as well as the required airflow, if any, need to be considered.
From the power, die and junction temperatures can be easily determined, and knowing these temperatures helps to answer the above questions.

Let’s start from a relationship that describes how the power consumed is related to the temperature of the integrated circuits.

The Formula
The formula below allows us to determine the junction temperature of the integrated circuits. Junction temperature is the die junction temperature which is also the temperature that silicon needs to tolerate before irreversible damages such as glassification occurs. This temperature can be given by:

\[ T_J = T_A + P_D \cdot \theta_{JA} \]

Where:
- \( T_J \) is the junction temperature
- \( T_A \) is the ambient temperature
- \( P_D \) is the total power dissipated in Watts
- \( \theta_{JA} \) is the package’s thermal resistance from junction to ambient and is in degrees Celsius per Watts.

In the above equation, after calculating the power, all the parameters are known except the junction temperature which can be easily determined.

The thermal characteristics or the resistance of the package in this case as in the case of \( C_{PD} \), needs to be supplied by the manufacturer of the device. This number is typically a function of the air flow, die size and the package type and size.

Table II, below, has some typical \( \theta_{JA} \) numbers for some common packages as a reference (refer to National Semiconductor Packaging Databook).

As it can be seen, the package type, die size as well as air flow, play a major role in determining the thermal resistance coefficient of each device.

Once this junction temperature has been obtained one must ask how safe this number is and how it will impact the long-term reliability of the device. But before answering these questions let us briefly discuss the factors that can influence this thermal resistance coefficient.

### Table II. Thermal Data across Different Package Type

<table>
<thead>
<tr>
<th>Package Type</th>
<th>( \theta_{JA} ) across Airflow (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drawing No.</td>
<td>Die Size</td>
</tr>
<tr>
<td>20-Pin SOP JEDEC</td>
<td>M20B</td>
</tr>
<tr>
<td>20-Pin Ceramic Wide Body</td>
<td>D20A</td>
</tr>
<tr>
<td>20-Pin SOP EIAJ</td>
<td>M20D</td>
</tr>
<tr>
<td>20-Pin Molded DIP</td>
<td>N20A</td>
</tr>
<tr>
<td>20-Pin PLCC</td>
<td>V20A</td>
</tr>
</tbody>
</table>

### Die Size
Clearly as die size increases, within the same package, there is more area for the heat to be dissipated. This causes the \( \theta_{JA} \) to be inversely proportional with the die size as plot 2, below reflects it.

### Lead Frame Material
The material used in the leads and its frame (what connects the die wire-bound to the outside) has a large effect in the thermal resistance of the device since it also acts as a heat sink.

### Airflow
Another important contributing factor to this thermal resistance. It is obvious that as the air flow increase the thermal coefficient decreases since higher airflow causes more rapid distribution of the ambient within the container, which help to cool the package, as fans do in the real world.

### Mounting
Also important is the path for distribution of the heat generated. There exist a difference between board and socket mounted devices as shown by plot 5. With soldered parts the body comes in contact with the board which acts as a heat sink. While the use of sockets will provide an additional path which will limit faster distribution of head into the board. For this reason the board mounted units have better (lower) thermal resistance.
Mold Compounds
Mold compounds play a major role in heat dissipation since each compound has a unique thermal characteristic. Besides the actual amount used in each package type, the kind material used will impact how much and how fast the heat that is generated by the device will get dissipated through the material used.

Plots below represent such examples.

Plot 3. Thermal Resistance vs Lead Frame Material

Plot 4. Thermal Resistance vs Air Flow

Plot 5. Thermal Resistance vs Board or Socket Mount

Reliability
Going back to the original question of what a safe junction temperature is and how it will affect the long-term reliability of the unit, we need to define terms such as early life, useful life, and wearout life.

But before explaining these terms let's mention briefly what is meant by failure rate. Failure rate is the number of devices which are expected to fail over a period of time. On the other hand, Mean Time Between Failures (MTBF) is the average time that is expected to elapse before a unit is failed and is normally measured in number of hours versus the number of units that is used to measure the failure rate. These two measurements are used quite often interchangeably and are inversely proportional to each other as given below;

\[ \text{MTBF} = \frac{1}{\text{Failure Rate}} \]

Going back to different types of failure rates, infant mortality rate, as shown in the shaded area of Plot 6, is mostly influenced by the system and application. Main contributors are electrical overstress and or excessive mechanical stressing of the units. This type of failure is often discovered during the manufacturing process as well as test and burn-in of the integrated circuits and or systems.

However, the other two types of failures are often discovered during the operation life of the units which could prove very costly and must be minimized.

In order to reduce these rates, we must be able to predict their occurrence and relate them to their operating environment. For this reason, mathematical models that explain failure rate over time are often used.

One such model is the Arrhenius Model (refer to NSC's packaging databook). This model which is well documented and proven over time assumes there exists a linear relationship between the failure rate and time as well as temperature.
This results in an equation that shows the failure rate at a given temperature is a function of another failure at that temperature.

The ratio of these two failure rates, \( F \), is given by below:

\[
F = \frac{X_1}{X_2} = \exp \left[ \frac{E}{K} \left( \frac{1}{T_2} - \frac{1}{T_1} \right) \right]
\]

where:
- \( X_1 \) is the failure rate at junction temperature one
- \( X_2 \) is the failure rate at junction temperature two
- \( E \) is the thermal activation energy (eV)
- \( K \) is the Boltzman constant

What this equation inspries, is the fact that there is a dramatic acceleration effect of the failure rate as the junction temperatures increase. As shown by plot 7.

Therefore, the overall goal of the system designer should be the reduction of the junction temperature of the integrated circuits to achieve the highest reliability of its product.

And as mentioned previously, choosing the right package and the right amount of air flow will determine to reduce this junction temperature which is caused by the total power dissipated within each unit.

In order to design the most cost effective and reliable system, designers need to calculate the power consumption of each component within their system as accurately as possible.

This allows for a better power supply design as well as providing enough airflow for the system to reduce the junction temperatures as much as possible.

Reducing junction temperatures will enhance the reliability and hence the useful life of their designs.

REFERENCES
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