CLC404, CLC522

OA-23 CLC522 Advanced Operating Considerations and Military Specifications

Literature Number: SNOA395
The CLC522 Variable Gain Amplifier is a versatile circuit that can be used in a wide variety of applications. The basic operation and specifications of the CLC522 are described in the datasheet for the CLC522; however, in many more demanding applications, the information contained in the datasheet is insufficient to analyze the expected performance. The purpose of this application note is to provide the additional information needed for analysis in some of these more demanding applications. The application note is a companion to the datasheet, and if you do not have a copy of the datasheet, one should be requested to obtain the full benefit from this application note.

**Frequency Response Determining Elements**

The CLC522 should be thought of as four separate amplifier elements in a single package. These are two very wideband, closed loop, unity gain buffers, a two quadrant multiplier core with gain control linearization, and a wideband current feedback op amp used as a transimpedance output stage. Both the buffer bandwidths and multiplier bandwidth are typically far in excess of the output op amp. It is therefore the frequency response of the output stage that typically sets the overall bandwidth for the CLC522. However, at high \( R_g \) values (low \( A_{v_{\text{max}}} \)), the input buffers are peaking slightly. This allows \( R_f \) to be increased to bandlimit the output amplifier as compensation for this input buffer peaking. Conversely, at very low \( R_g \)'s (high \( A_{v_{\text{max}}} \)), the input buffers start to become the bandlimiting point. In this case, \( R_f \) can be decreased from its nominal 1k value to peak the output amplifier. This partially compensates for the increased rolloff at the input due to heavy loading on the buffer outputs.

This discussion is reflected in plot 4 showing a suggested \( R_f \) vs. \( A_{v_{\text{max}}} \). This plot shows the required \( R_f \) to most closely match the \( A_{v_{\text{max}}} = 10 \), \( R_f = 1k \) typical frequency response when operating with \( V_g = 1.1V \). In addition, plot 6 shows the bandwidth reduction (at various \( A_{v_{\text{max}}} \) settings) for an increased \( R_f \) value. Increasing \( R_f \) will allow \( R_g \) to be increased, for a given desired \( A_{v_{\text{max}}} \), which will allow a higher maximum differential (\( V_{A_{\text{d}_{\text{max}}}} \)) input signal to be applied.

Very little change in the frequency response is observed as \( V_g \) is reduced below +1 volt reducing the CLC522 signal gain from \( A_{v_{\text{max}}} \). Since the frequency response is dominantly determined by the output amplifier, shunting signal away to ground in the 2 quadrant multiplier has little effect on the shape of either the magnitude or phase response (see plots 2, 3, 8, 9, and 10). When the CLC522 is actually being used as an attenuator, however, high frequency feedthrough will alter the shape of the frequency response at high frequencies (see plots 1 and 7).

**Usable Gain Adjustment Range**

The gain of the CLC522 may always be varied from \( A_{v_{\text{max}}} = 0 \) to \( A_{v_{\text{max}}} = 1.85 \cdot R_f/R_g \), the CLC522 can be thought of as an electrical attenuator as the gain control voltage is being reduced below 1V. In situations where a constant maximum output signal voltage is desired, the maximum gain will be used at minimum input while the minimum gain will be used when the maximum input signal is present. This is not to say that the gain is being adjusted to hold a constant output voltage swing. Rather, the input signal is varying over a range of voltages and the CLC522 gain is being adjusted such that the maximum input signal is always being scaled to a desired maximum output voltage. Given the resistor values selected for \( R_f \) and \( R_g \) along with the current limit on the input stage (\( I_{\text{T}_{\text{AIL}}} \)), a maximum attenuation from \( A_{v_{\text{max}}} \) can be computed that satisfies the requirement that the maximum input voltage (at minimum gain) does not cause more than \( I_{\text{T}_{\text{AIL}}} \) to flow in \( R_g \).

From a maximum gain set by \( A_{v_{\text{max}}} = 1.85 \cdot R_f/R_g \), the CLC522 can be thought of as an electrical attenuator as the gain control voltage is reduced below 1V. In situations where a constant maximum output signal voltage is desired, the maximum gain will be used at minimum input while the minimum gain will be used when the maximum input signal is present. This is not to say that the gain is being adjusted to hold a constant output voltage swing. Rather, the input signal is varying over a range of voltages and the CLC522 gain is being adjusted such that the maximum input signal is always being scaled to a desired maximum output voltage. Given the resistor values selected for \( R_f \) and \( R_g \) along with the current limit on the input stage (\( I_{\text{T}_{\text{AIL}}} \)), a maximum attenuation from \( A_{v_{\text{max}}} \) can be computed that satisfies the requirement that the maximum input voltage (at minimum gain) does not cause more than \( I_{\text{T}_{\text{AIL}}} \) to flow in \( R_g \).

It is useful here to discuss the gain range in terms of dB. It is also often useful to consider input and output sinusoidal voltage swings in terms of dBm. The gain from the differential input voltage to the output voltage in terms of dB is given by equation 1.

\[
G_{\text{dB}} = 20 \cdot \log ((V_g + 1) \cdot A_{v_{\text{max}}} / 2) \tag{1}
\]

Converting a sinusoidal voltage from a peak to peak swing into dBm can be done using equation 2.

\[
P_{\text{dBm}} = 10 \log \left( \frac{V_{pp}}{2 \sqrt{2}} \right) \tag{2}
\]
Strictly speaking, this is the power in a 50Ω resistor referenced to 1mW. However, for the purposes of this discussion, a peak-to-peak voltage swing across any resistive load will be computed as in equation 2.

Given a maximum plus and minus current available in $R_g$ ($\pm I_{TAIL}$), this current, times 1.85, is the maximum (when $V_g \geq 1.0$ volt) that is available to feed through $R_f$ in producing a maximum available output pin voltage swing; $V_{opp}(\max) = 2 \times 1.85 \times I_{TAIL} \times R_f$. When the CLC522 gain is being adjusted to hold the output swing relatively constant, the desired maximum $V_{opp}$ must be less than the $V_{opp}(\max)$ shown above if there is to be any gain adjust range. As the gain is reduced from $A_{v\max}$, the available maximum current through $R_f$ is also being attenuated by the same amount that the gain has been attenuated. The gain can therefore only be reduced from $A_{v\max}$ until this attenuation in gain times $2 \times 1.85 \times I_{TAIL} \times R_f$ equals the desired maximum $V_{opp}$. The ratio of maximum available swing, $V_{opp}(\max)$, to the desired maximum output voltage swing, $V_{opp}$, is also the ratio of maximum gain to minimum gain. Equation 3 summarizes this discussion by showing the available gain range before input limiting occurs.

Linear (V/V) gain adjustment range

$$A_{v\max} = 2 \times 1.85 \times I_{TAIL} \times R_f = \beta V_{opp}$$

In log terms, gain adjust range =

$$20 \times \log \left( \frac{2 \times 1.85 \times I_{TAIL} \times R_f}{V_{opp}} \right) \text{ dB}$$

Eq. 3

Note that this gain adjustment range is independent of $R_g$ and hence $A_{v\max}$. This will be the gain adjustment range available from any maximum gain selected for a given $R_f$ and desired maximum $V_{opp}$.

The log form of equation 3 is used in plot 5 for $I_{TAIL} = 1.8$mA given a range of values for $R_f$ swept over a wide range of desired maximum output voltage swings.

A CLC522 design may be done using these results. Given a required gain adjustment range, select an $R_f$ from plot 6 consistent with the desired bandwidth (with some assumption on $A_{v\max}$ at this point), then, entering plot 5 on the y-axis at the desired gain adjustment range go over to the intersection with the selected $R_f$ line and then extend downward to read off the available fixed output swing. If the available $V_{opp}$ is less than or equal to the desired level, using the minimum input voltage coming in, a maximum gain and hence $R_g$ may be resolved (Some iterating at this would be required since plot 6 is parametric in terms of $A_{v\max}$). If the required $R_f$ to get a desired bandwidth along with the gain adjust-ment range requirement leads to a maximum $V_{opp} = (2 \times 1.85 \times I_{TAIL}/\beta)$ that is less than desired, a fixed gain post-amplifier should be used.

**Gain Accuracy Considerations**

The CLC522 is intended to provide an exceptionally well controlled attenuation from $A_{v\max}$ where the full gain adjust range is for a ground referenced $V_g$ from -1 to +1 volt. $V_g$ is actually compared to an internal reference developed from the negative supply voltage. Equation 4 modifies equation 2 to include the effect of the minus supply.

$$A_v = (1 + V_g/(0.2 \times |V_{EE}|)) \times A_{v\max}/2 \text{ V/V}$$

Eq. 4

For $V_{EE} = -5$, equation 4 reduces to equation 2. The effect of DC variations in Vee is to expand or contract the fullscale gain control range. AC variations in $V_{EE}$ will modulate the output dependent upon the input signal present. The PSRR (plot 36) is therefore only for the positive supply voltage since variations in the minus supply will show up at the output dependent on the input signal present. It is critically important, therefore, to keep the minus supply stable and free of high frequency noise.

**Controlling DC Offsets**

With no input signal present, there will always be a residual DC voltage at the output. This offset arises from input stage mismatches, a DC bias current at the 2-quadrant multiplier output, and output op amp DC error terms. Figure 1 shows the DC error model including all of these effects.

Figure 1: DC Offset Model
on the gain adjust voltage, $V_g$. The buffer input bias currents are typically matched to closer than 0.1mA while the two buffer input offset voltages are matched to typically less than 1mV. To take advantage of this excellent bias current match at the buffer inputs (a low offset current), matched DC source impedances should be provided at the two buffer inputs.

The output offset voltage may be improved using the adjustments shown in Figure 2.

![Figure 2: Input and Output Stage DC Offset Adjustments](image)

It will not be possible to completely null the output offset as the gain is adjusted since the $I_{b\text{core}}$ term in Figure 1 will vary non-linearly over the gain adjustment range. However, a first order correction for the DC error terms of Figure 1 may be accomplished by removing any input signal (but retaining the DC source impedance) and making the following adjustments.

To correct for only the errors introduced by the output amplifier, the gain should be first adjusted to a minimum ($V_g = -1$). With no contribution due to the input DC error terms, $R_{p2}$ in Figure 2 may be used to sum a current into the inverting node of the output amplifier to cancel just the output amplifier DC error terms. This adjustment could alternatively be used to introduce a fixed ($V_g$ independent) offset into the output voltage. With the output amplifier's DC level determined by $R_{p2}$ while $V_{p2} < -1$, returning $V_g$ to the maximum expected value (gain) will allow the input DC error terms to be cancelled. With $V_g$ at the maximum value that will be used, $R_{p1}$ in Figure 2 may be adjusted to return the output voltage to the value measured when $V_g$ was at the minimum gain setting. This input adjustment is actually introducing an offset that is cancelling the effect of both the input buffer error terms and the effect of $I_{b\text{core}}$ at the maximum gain setting. The $R_{p1}$ adjustment of Figure 2 could alternatively be used to cancel a fixed DC component in the input signal. For this application, the input should be connected and $R_{p1}$ adjusted to move the AC component to the desired DC level at the output.

Adjusting the input and output stage offsets at the two gain extremes will hold the output DC error at a minimum at these two points in the gain range. The non-linear DC error introduced by the multiplier core will cause a residual, gain dependent, offset to appear at the output as the gain is swept from minimum to maximum. Also, neither the input nor the output offset adjustments described here will improve temperature drift effects.

Generally, a low $R_f$ will reduce the gain for the error current terms at the inverting input of the output amplifier. Note that matching $R_b$ to $R_f$ (in Figure 1) for bias current cancellation in the output op amp will not work for current feedback amplifiers, and, in any case, $R_b$ should always be 20Ω. Due to good matching, the actual errors introduced by the input buffers is relatively minimal - particularly with low, matched, source impedances ($R_{s1} = R_{s2}$). Although not shown in Figure 1, each of the input

![Figure 3: Full CLC522 Noise Model](image)
buffers introduce a very well matched drop of approximately 0.9V from their inputs to output voltage across $R_g$. This common mode voltage level shift to the $R_g$ resistor is of no consequence in normal operation, but should be kept in mind if DC paths are connected for some reason to pins 4 and 5.

**Noise Model**

The complete noise model for a part as flexible as the CLC522 is necessarily somewhat complex. That model, with all of the external resistor noise sources included, is shown in Figure 3.

An optional resistor coming into the inverting pin of the output amplifier ($R_g$) has been included in this model for completeness. This would be the impedance looking back towards either a DC offset adjust network or a separate signal source. Each of the noise voltages and currents in Figure 3 are spot noises (per $\sqrt{\text{Hz}}$). To arrive at an expression for the total output spot noise (in nV/$\sqrt{\text{Hz}}$) each of the noise sources of Figure 3 must be taken to the output by its gain and then squared. The total equivalent output noise is then the square root of the sum of squared contributing elements. See application note OA-12 for a general discussion of computing amplifier noise.

The analysis in equation 5 steps through developing the total output noise voltage from the model of Figure 3. This analysis generates an expression for the total output voltage from the model of Figure 3. This expression is the sum of the noise contributions of the input stage, the output amplifier, and the core current noise term at the inverting input of the output amplifier, $I_{\text{core}}$, is considered.

**Total output spot noise power ($E_{o}^{2}$)**

$$E_{o}^{2} = \left( (1.9 nV)^{2} + (5 pA R_b)^{2} + 4 kT R_b \right) \left[ 1 + \frac{R_l}{R_g} \right]^{2} + 4 kT \left[ 1 + \frac{R_l}{R_g} \right] + \ldots$$

Output amplifier noise terms

$$\ldots + \left[ (14 pA R_g)^{2} + (2.3 nV)^{2} + (1.6 pA R_s_{1})^{2} + (1.6 pA R_s_{2})^{2} + 4 kT \left( R_{s1} + R_{s2} \right) \right] \left[ \frac{1}{2} \left( V_g + 1 \right) \frac{1.85 R_l}{R_g} \right]^{2} \ldots$$

Input stage noise terms

$$\ldots + \left[ 30.5 pA + 12.4 pA + 7.5 pA \left( \frac{l_{\text{rms}}}{\text{mA}} \right) \left( 1 - V_g^{2} \right)^{1.2} \right] R_l^{2}$$

Fixed term + Core current noise

$I_{g\text{rms}}$ is the RMS current in $R_g$ (include DC) in mA

Generally, most of these terms are negligible; with $R_{s1}, R_{s2}, R_b$ relatively low and $R_g = \infty$ and $\sqrt{4kT R_l}$ low relative to $(30.5 pA R_g)$.

$$E_{o}^{2} = \left( (14 pA R_g)^{2} + (2.3 nV)^{2} \right) \left( \frac{1}{2} \left( V_g + 1 \right) 1.85 \frac{R_l}{R_g} \right)^{2} + \left[ 30.5 pA + 12.4 pA + 7.5 pA \left( \frac{l_{\text{rms}}}{\text{mA}} \right) \left( 1 - V_g^{2} \right)^{1.2} \right] \frac{l_{\text{rms}}}{R_g}$$

Eq. 5

The $I_{\text{core}}$ noise term merits additional description. This term is actually modeling the noise injected through the gain adjustment input, $V_g$. At either gain extreme, (for $V_g = \pm 1 V$), this term is zero. The $I_{\text{core}}$ noise current reaches a maximum for $V_g = 0$ which would be at 1/2 of the maximum gain setting. At this $V_g$, $I_{\text{core}}$ shows a peak value that is dependent on the RMS current in the $R_g$ resistor. Noise in the $V_g$ path will modulate the gain for this input signal current. At maximum gain, all signal current is being passed on to the transimpedance stage and the $I_{\text{core}}$ contribution is zero. Similarly, with the gain adjust channel shut off for $V_g < -1 V$, no signal current is passed through the multiplier core and $I_{\text{core}}$ is again zero. The maximum noise contribution through the $V_g$ channel is where exactly half of the signal current is being diverted to ground, at $V_g = 0$. The effect of this increasing $I_{\text{core}}$ with reducing gain is to hold up the output noise through the first 6dB of attenuation from maximum gain. This is, for recommended $R_l$ values, only perceptible for a relatively low $A_{\text{vmax}}$ as can be observed in plot 23 for $A_{\text{vmax}} = 2$ and $A_{\text{vmax}} = 5$.

**Computing Signal to Noise Ratio**

In applications where it is desired to hold a fixed output voltage swing ($V_{\text{opp}}$), it is most meaningful to consider SNR at the output. In this application, the worst case SNR will generally occur at maximum gain, $A_{\text{vmax}}$. It is possible, at lower $A_{\text{vmax}}$ settings, to see a slight degradation in SNR for the first 6dB of attenuation from maximum gain due to the effect of $I_{\text{core}}$ as discussed in the previous section. However, the improved accuracy does not justify the complexity introduced by including this term in the SNR analysis. Therefore, a good approximation is that the worst case output SNR will...
occur at \( A_{v_{\text{max}}} \). This would be when the input is at its minimum in applications that are using the CLC522 to move a very widely varying input range to more limited output range. While SNR will improve as the gain is reduced, harmonic distortion will be getting worse as the input signal range is increasing. Most distortion terms are set by the RMS current in \( R_g \) which will be at a maximum when the gain is at a minimum.

Using some of the operating constraints imposed on the CLC522, it is possible to significantly simplify equation 5 into a relatively simple expression for the worst case output SNR at \( A_{v_{\text{max}}} \).

Continuing the assumptions of equation 5, (that \( R_{s1}, R_{s2}, \) and \( R_b \) are low, that \( R_g' \) is not present, and that the voltage noise of the output amplifier and the contribution of the resistor noise is negligible), and evaluating this expression at \( A_{v_{\text{max}}} \), yields the maximum output spot noise voltage.

\[
E_{\text{o}_{\text{max}}} = \sqrt{\left(14pA R_g\right)^2 + 2(3.2nV)^2} \left(1.85 \frac{R_l}{R_g}\right)^2 + (30.5pa_1)^2 \quad \text{Eq. 6}
\]

In situations where the minimum input voltage \( (V_{\text{imin}}) \), maximum input voltage \( (V_{\text{imax}}) \), and desired output voltage \( (V_{\text{opp}}) \) are known, both \( R_l \) and \( R_g \) will be determined by the gain and maximum differential input voltage constraints (see the discussion of usable gain adjust range). The expression for \( E_{\text{o}_{\text{max}}} \) can then be simplified using these constraints on \( R_l \) and \( R_g \). One assumption that this analysis will make is that resistor values will be set up such that \( \pm I_{\text{TAL}} \) will flow in \( R_g \) when the input is at its maximum peak-to-peak swing. This will make full use of the dynamic range of the CLC522. The discussion of input and output voltage swings are in peak-to-peak, but the current in \( R_g \) is limited in a peak sense. One half of the peak to peak input voltage is therefore used in computing the peak current in \( R_g \). From equation 3 an expression for \( R_l \) may be found by solving for either \( R_l \) or the gain adjust range, \( \beta \).

\[
R_l = \frac{\beta \cdot V_{\text{opp}}}{2 \cdot I_{\text{TAL}}} \quad \text{where} \quad \beta = \text{linear gain adjust range}
\]

\[
\beta = \frac{V_{\text{imax}}}{V_{\text{imin}}}
\]

If it is also assumed that at minimum input we will operate at maximum gain (and neglecting for simplicity the 3Ω that is added to \( R_g \) in setting \( A_{v_{\text{max}}} \))

\[
A_{v_{\text{max}}} = \frac{1.85 \cdot R_l}{R_g} = \frac{A_{\text{opp}}}{V_{\text{imin}}}
\]

The input stage current limit will constrain \( R_g \) as follows:

\[
V_{\text{imin}} \left(\frac{2}{R_g}\right) = I_{\text{TAL}} \quad \text{(recalling that} \quad V_{\text{imax}} \quad \text{is peak-to-peak)}
\]

Solving for \( R_g \) and substituting for \( V_{\text{imax}} = \beta \cdot V_{\text{imin}} \)

\[
R_g = \frac{\beta \cdot V_{\text{imin}}}{2 \cdot I_{\text{TAL}}} \quad \text{Eq. 7}
\]

These three expressions constraining \( R_l \), \( A_{v_{\text{max}}} \), and \( R_g \) may now be substituted into equation 6 to yield

\[
E_{\text{o}_{\text{max}}} = \sqrt{\left(14pA \frac{V_{\text{opp}}}{2I_{\text{TAL}}}\right)^2 + 2(3.2nV)^2} \left(\frac{V_{\text{opp}}}{V_{\text{imin}}}\right)^2 + (30.5pa_1)^2 \quad \text{Eq. 8}
\]

After some algebraic manipulation equation 8 results

\[
E_{\text{o}_{\text{max}}} = \frac{\beta V_{\text{opp}}}{2I_{\text{TAL}}} \sqrt{(21.6pA)^2 + 2 \left(3.2nV \frac{2I_{\text{TAL}}}{V_{\text{imax}}}\right)^2} \quad \text{Eq. 9}
\]

Note that \( \frac{V_{\text{imax}}}{2I_{\text{TAL}}} = R_g \)

and that \( \frac{\beta V_{\text{opp}}}{2I_{\text{TAL}}} = 1.85 R_l \)

This greatly simplified expression for the maximum output spot noise may now be compared to the output signal voltage to get a worst case SNR. This will be done relative to the maximum \( V_{\text{opp}} \). Recognize, however, that in any application the output voltage at any gain setting will be going below this \( V_{\text{opp}} \). Dividing this maximum \( V_{\text{opp}} \) by the computed minimum SNR will tell how far below \( V_{\text{opp}} \) an signal may be discerned from the noise at the output. One way to do this is to convert the output spot noise to an integrated RMS noise voltage by multiplying equation 13 by the square root of the Noise Power Bandwidth - √NPB and dividing this into the RMS output voltage ((\( V_{\text{opp}}/2 \cdot \sqrt{2} \)) for sinusoids). Doing this yields:

\[
\text{Minimum SNR} = \frac{V_{\text{opp}}}{2 \cdot \sqrt{2}} \frac{\beta V_{\text{opp}}}{2I_{\text{TAL}}} \sqrt{(21.6pA)^2 + 2 \left(3.2nV \frac{2I_{\text{TAL}}}{V_{\text{imax}}}\right)^2} \sqrt{\text{NPB}} \quad \text{Eq. 10}
\]

Simplifying equation 9 gives

\[
\text{Minimum SNR} = \frac{I_{\text{TAL}}}{\beta} \sqrt{(21.6pA)^2 + 2 \left(3.2nV \frac{2I_{\text{TAL}}}{V_{\text{imax}}}\right)^2} \sqrt{2\text{NPB}}
\]
It is important to note that the value for $V_{\text{imax}}$ strongly influences the minimum SNR. As $V_{\text{imax}}$ becomes relatively small, the minimum SNR can become rapidly larger. Setting the two noise currents under the radical equal and solving for $V_{\text{imax}}$ will yield a crossover point where the effect of $V_{\text{imax}}$ starts to dominate. Using $I_{\text{TAIL}} = 1.35\text{mA}$, this yields $V_{\text{max}} = 0.57\text{Vpp}$. For $V_{\text{imax}} > 0.57\text{Vpp}$, this second term in the radical rapidly becomes negligible and the achievable minimum SNR reaches a floor set by the 21.6pA term. For $V_{\text{imax}} < 0.57\text{Vpp}$, the minimum SNR will decrease steadily with decreasing $V_{\text{imax}}$. It is also important to note that the input signal is increasing as the gain is reduced below $A_{\text{vmax}}$.

**Example Calculation of Minimum SNR**

Using the results of the previous section, it would be instructive to step through an entire design. As an example, use the following design information:

- $V_{\text{imax}} = 1\text{Vpp}$
- $\beta = 10$ (gain adjustment range, implies $V_{\text{imin}} = 0.1\text{Vpp}$)
- $I_{\text{TAIL}} = 1.35\text{mA}$
- NPB = 50MHz

Then, using equation 10 to get the worst case SNR (in RMS/RMS)

$$\text{Minimum SNR} = \frac{1.35\text{mA}}{\left(21.6\text{pA}\right)^2 + 2 \left(\frac{3.2\text{nV}}{2\left(1.35\text{mA}\right)}\right)^2 \sqrt{2 \times 50\text{MHz}}$$

This result states that when the input signal is ranging up to $0.1\text{Vpp}$ (and the CLC522 is set at a maximum gain of whatever is needed to get to a desired $V_{\text{opp}}$), the input signal can range down as low as $0.1\text{Vpp}/544 = 0.18\text{mV}$ and have an RMS power at the CLC522 output equal to RMS noise power. It is very interesting to note that although the actual value for the desired $V_{\text{opp}}$ will have no impact on the minimum SNR, it will, along with the desired gain adjustment range and $I_{\text{TAIL}}$, determine the required value for $R_{f}$. Continuing this example to determine the $R_{f}$ and $R_{g}$ values, and targeting a $V_{\text{opp}} = 1\text{Vpp}$ (which will set $A_{\text{vmax}} = 10$ to get $1\text{Vpp}$ at the output when $V_{\text{ipp}} = 0.1\text{Vpp}$).

$$R_{f} = \frac{\beta \times V_{\text{opp}}}{\left(2 \times 1.85 \times I_{\text{TAIL}}\right)} = \frac{10 \times 1\text{Vpp}}{\left(2 \times 1.85 \times 1.35\text{mA}\right)} = 2002\Omega$$

(from Eq. 3)

$$R_{f} = \frac{2002 \times 1.85}{10} = 370\Omega$$

(recall that the physical $R_{g}$ resistor must be 3Ω lower to account for the buffer output impedances)

Checking whether the $I_{\text{TAIL}}$ current limit in $R_{g}$ is satisfied

$$I_{\text{gmax}} = \frac{\left(V_{\text{imax}}/2\right)}{R_{g}} = \frac{\left(1\text{Vpp}/2\right)}{370} = 1.35\text{mA}$$

And finally, checking plot 6 for the CLC522 bandwidth that will result for an $R_{f} = 2000$ and $A_{\text{vmax}} = 10$ shows approximately 74MHz. Some means of setting the NPB to 50MHz after the CLC520 will be required to get the above results.

An alternative design approach would control $R_{f}$ to get a desired bandwidth using an assumed $A_{\text{vmax}}$ and plot 6. The only modification to the foregoing analysis is that, with $R_{f}$ given along with the gain adjust range ($\beta$) and $V_{\text{imax}}$, the minimum SNR expression is unchanged but the achievable output voltage is set by the expression used earlier for $R_{f}$.

$$V_{\text{opp}} = \frac{1000 \times 2 \times 1.85 \times 1.35\text{mA}}{10}$$

and the maximum gain has dropped to $\frac{1.85 \times 1000}{370} = 5$.

Going to plot 6 at $R_{f} = 1k$ and $A_{\text{vmax}} = 5$ shows a 220MHz bandwidth.

If it becomes necessary to set $R_{f}$ to achieve a particular bandwidth, and to take whatever $V_{\text{opp}}$ that results, a fixed gain post amplifier can be used to adjust the $V_{\text{opp}}$ to a higher level if desired. It would be a very poor post amplifier that would degrade the SNR from that available at the output of the CLC522.

In summary, when the CLC522 is being used to scale a varying input range to a fixed output range, the minimum SNR at the output will occur at the maximum gain setting since this is the operating condition when the input is at a minimum. From equation 10, this minimum SNR depends only on the maximum current allowed in $R_{g}$ ($I_{\text{TAIL}}$), the desired gain adjust range ($\beta$), the maximum anticipated input signal, the noise power bandwidth, and some constant noise terms associated with the CLC522. This minimum SNR is independent of the desired $V_{\text{opp}}$. The value for the feedback resistor ($R_{f}$) will simultaneously set both $V_{\text{opp}}$, $A_{\text{vmax}}$, and the CLC522 bandwidth. The primary design job is then to make the correct trade-off is getting to a value for $R_{f}$.
Using the Output Amplifier Separately

Although the output op amp is principally intended as a transimpedance stage for the signal current coming out of the gain adjustment stage, it can also be used as an inverting op amp for additional signals. The non-inverting input of this op amp is also available on pin 9. However, this pin should never be used to inject signal or offsets. Pin 9 should always be connected to a good ground plane through a 20Ω resistor. Figure 4 shows an example of how a high frequency signal may be summed into the output (with a gain of -1 in this case) independently of the output signal due to the gain adjusted input on pin 3.

![Diagram](http://www.national.com)

Figure 4: Using the Output Amplifier to Sum in a Separate Signal

The circuit of Figure 4, with \( V_g < -1 \) volt, \( R_t \) set to get \( R_g || R_t = 50\Omega \), \( R_i = 1k \), and a series output 50Ω resistor into a 50Ω load, was used to illustrate the output amplifier performance for plots 27, 30, 31, 32, and 33. These plots show that the output op amp is an exceptional amplifier in and of itself. The output op amp configured as an inverting amplifier offers a small signal bandwidth in excess of 200MHz (for inverting gains \( \leq 2 \)), 2nd & 3rd harmonic distortion powers greater than 60dBm less than the fundamental for output signals \( \leq 20 \)MHz and \( \leq 2 \)Vpp (10dBm) into a 100W load, and a 2-tone 3rd order intercept 35dBm for frequencies \( < 20 \)MHz (defined at a matched 50Ω load).

The output op amp should not be used for inverting gains >5. As this inverting gain is increased beyond this, 2nd order effects will start to limit the bandwidth for signal current from the gain adjust stage. In addition, higher inverting gains will begin to contribute significant errors from the output op amp’s non-inverting input offset voltage and noise.

Predicting Harmonic Distortion (still in development)

The total harmonic distortion present at the output will be a combination of both input stage and output amplifier effects. The output amplifier’s harmonic distortion sets a minimum distortion level that can be expected (see plots 31 and 32). The output amplifier shows exceptional 2nd harmonic distortion but a 3rd harmonic term that increases rapidly with power and frequency. The input stage contributes a 2nd harmonic distortion that depends only on the power level in the \( R_g \) resistor and is relatively independent of the gain setting. In fact the input stage shows a very good match to a 2nd order intercept model. (Some statement here on 3rd harmonic distortion)

**Limits to I/O Range and Overdrive Recovery**

Several factors can limit the input and output voltage ranges. In most cases, the input stage will limit before the output stage has reached its maximum voltage swing. The maximum current available through \( R_t \) is simply \( 1.85 \cdot I_{TAIL} \). As long as \( 1.85 \cdot I_{TAIL} + R_t < V_{omax} \), the input stage will always limit due to \( I_{TAIL} \) before the output amplifier can reach its maximum ± voltage (i.e. \( V_{omax} \)). For the output amplifier to be the limiting case, \( 1.85 \cdot I_{TAIL} < V_{omax} \). With \( I_{TAIL} = 1.8 \)mA and \( V_{omax} = 3.7 \) Volts, \( R_t \) must be >1.1kΩ. Thus far, only the maximum gain case has been considered. This is when the full 1.85*I_{TAIL} is passed on through the multiplier core to the output transimpedance stage. As the gain is reduced from \( A_{vmax} \), and less maximum current is available to \( R_t \), the voltage swing limit will eventually return to the input stage even for high \( R_t \) values. This can be shown by equating the available maximum current through \( R_t \) to the output amplifier’s voltage limit as shown in equation 12.

\[
V_{omax} = 1.85 \cdot I_{TAIL} \cdot R_t \left( \frac{V_g + 1}{2} \right)
\]

**Eq. 12**

Solving for the required \( V_g \) to have an equal input and output limit (note that this is a bipolar limit) -

\[
V_g = \frac{V_{omax}}{1.85 \cdot I_{TAIL} \cdot R_t} - 1
\]

**Eq. 13**

As an example, consider a low \( A_{vmax} \) case with \( R_t = 2k\Omega \), \( I_{TAIL} = 1.8mA \) and \( V_{omax} = 3.7 \) Volts. At \( A_{vmax} \), the voltage swing limit will be set by the output stage to \( V_{omax} \) since \( R_t > 1.1k\Omega \). Solving equation 13 for this example shows that for \( V_g < 0.11 \) Volt the voltage limit will move to the input stage. Once the swing limit has moved to the input, the right side of equation 12 is what is available at the output. Recall that this input limit is simply the differential input voltage that causes \( I_{TAIL} \) to flow in \( R_g \). This discussion can provide another approach to computing the available attenuation from maximum gain for a fixed desired output voltage swing. Substituting a desired \( V_{oppeak} \) into equation 12 in place of \( V_{omax} \), (and recognizing that this peak swing is actually available as a peak-to-peak swing since \( I_{TAIL} \) is bipolar), will yield the minimum \( V_g \) before input stage limiting occurs. If this expression for \( V_g \) is substituted into 20 * log((\( V_g + 1)/2)) \) (which is the log form of attenuation vs. \( V_g \), equation 14 results -

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available attenuation = 20 log \( \left( \frac{V_{\text{peak}}}{1.85 I_{\text{Ttail}} R_f} \right) \) Eq.14

This is simply the earlier expression for gain adjust range, equation 3, with \( V_{\text{opp}}/2 \) replaced by \( V_{\text{peak}} \) and the fraction flipped over to give negative numbers for the maximum attenuation. Output limited overdrives recover much more quickly than input limited overdrives. This can be seen in the typical overdrive recovery waveforms of plots 37 and 38.

An important additional limit to operation is in the \( V_g \) input. \( V_g \) input voltages beyond the control input range of \( \pm 1V \) run the risk of saturating internal nodes which will severely degrade the apparent gain control channel bandwidth as \( V_g \) is brought back into range. This gain control channel saturation can change the loop dynamics in a continuous feedback adjustable gain circuits. If this slowing down of the gain control response is problematic, a limit of \( -2V < V_g < +1.2V \) should be observed to avoid internal saturation on the gain adjust channel.

**RF Specifications**

Several dynamic range characteristics are unique to RF amplifier descriptions. The RF specifications that can be applied to the CLC522 include noise figure, 2-tone, 3rd order intercept, and -1dB compression. While the noise figure is an input referred specification, (with some assumption on source impedance), the intercept and compression specifications are commonly in reference to an output power at a matched 50Ω load. For these RF specifications, then, it will be assumed that a series 50Ω resistor to a 50Ω load is present at the output. The gain that has been previously discussed as a voltage or dB gain from the input pin to the output pin will now be to this matched load instead. Hence, the input to output gain will be cut in half or decreased by 6dB. Also, all of these specifications are assuming purely sinusoidal inputs. For further reference, application note OA-11 defines each of these specifications and describes how to apply them to op amp type amplifiers. In addition, a spreadsheet that will calculate the noise figure and 2-tone spurious levels over a wide range of operating conditions is available from the Comlinear applications department.

**Noise Figure**

The noise figure for a device is a measure of the degradation in Signal-to-Noise ratio in going from the input to the output. The input noise is taken to be the noise power delivered by the source resistor to the input impedance of the amplifier circuit. Figure 5 shows this definition for the CLC522.

\[
\text{Noise Figure } NF = 10 \log \left( \frac{e_o^2}{A_v R_s kT} \right)
\]

where
- \( e_o \rightarrow \) total output noise voltage
- \( A_v \rightarrow \) voltage gain from pin3 \( \rightarrow \) pin 10 in V/V
- \( R_s = R_{s1} = R_{s2} \)
- \( kT = 4\times10^{-21} \text{ (at } 290^\circ\text{K}) \)

This expression for noise figure can then use equation 5 (or the more complete expression for output noise) to compute the noise figure for any particular gain and resistor values. The noise figure discussed here is for a 1Hz bandwidth (i.e. spot noise figure). Plot 24 shows this spot noise figure (for \( R_s = 50\Omega \) and each input terminated to ground in 50Ωs) using equation 15 and the complete expression for total output noise.

**2-tone, 3rd Order, Intermodulation Intercept**

A simple model for an RF amplifier will typically project that 3rd order intermodulation spurious powers will increase 3dBm for every 1dBm increase in two signal powers at two closely spaced frequencies. If the average frequency of the two high power signals is taken to be \( F_0 \), with an equal spacing of DF around this center frequency, the two 3rd order spurious terms will fall at \( F_0 \pm 3DF \).

Assuming equal powers \( (P_o) \) in the two desired signals, equal 3rd order spurious powers \( (P_s) \) will also result. At any particular frequency, \( F_0 \), equation 16 shows how an intercept (IM3) can be defined from a single measurement of \( P_o \) and \( P_s \) (where \( P_o \) and \( P_s \) are powers in dBm at the matched load).
The utility of this estimate of intercept is that given IM3 and equal two tone output signal power levels, the spurious power at the intermodulation frequencies may be predicted as shown in equation 17.

\[ P_s = 3 \cdot P_o - 2 \cdot IM3 \text{ dBm} \]  

**Eq. 17**

or, in terms of how far below the desired signals are,

\[ P_o - P_s = 2 \cdot (IM3-P_o) \text{ dBc} \]  

**Eq. 18**

National application notes OA-11 and OA-22 treat in considerable detail this intercept model for predicting 2-tone intermodulation distortion levels.

The 2-tone intermodulation spurious powers at the output of the CLC522 are a combination of 3rd order distortion mechanisms in both the input stage and the output amplifier. In most cases, the 3rd order distortion in the Rg current will dominate in setting the intermodulation distortion at the output. Since this is a case of cascaded amplifier intermodulation distortion, a single IM3 number for the total amplifier is not applicable. However, separate IM3 values for the input stage and the output amplifier will allow the calculation of the spurious power levels at the output.

Using the two intercepts in plot 27, a total output spurious level may be estimated. Since distortion is coming in at two points in the CLC522, (for a single pair of desired signal frequencies), the distortion introduced at the input will have a fixed (but unknown) phase relationship to the distortion introduced by the output stage. A reasonable estimate would be to assume that these two sources of distortion are in quadrature and will add together as the square root of summed squared voltages. Given a desired two tone power level at the matched load (\( P_o \)), and a gain from input to output, the two contributions to the spurious power at the output (\( P_{so} \)) will be -

\[ P_{so} - 3P_o = 2IM3_o \text{ dBc} \]  

**Eq. 19**

Output amplifier term

\[ P'_{so} = 3P_o - 2 \left(IM3_i + G_{db} - 6 + 10 \log \frac{R_g}{50} \right) \text{ dBm} \]  

**Eq. 20**

Input stage term taken to output

IM3\(_o\) and IM3\(_i\) are taken from plot 27 at the frequency of interest. Note that Gdb is the log gain from the input to output pins (equation 1) and the 6dB term in the expression for \( P_{so} \) accounts for the 6dB loss in going from the output pin to the matched load. Since the input stage distortion really depends on the current in the \( R_g \) resistor, the input power must be converted to a power in \( R_g \). This is the effect of the \( 10 \cdot \log(R_g/50) \) in the expression for \( P_{so} \).

Given these two contributions to the 3rd order spurious power, equation 21 combines these into a typical combined spurious power.

\[ P_{st} = 10 \log \left( \frac{P_{so}}{10^{10}} + \frac{P'_so}{10^{10}} \right) \text{ dBc} \]  

**Eq. 21**

In general, the input stage spurious (\( P_{so} \)) will be the dominate contribution to the output 3rd order spurious power. The input generated spurious will be greater than the output stage spurious as long as the condition shown in equation 22 is satisfied.

\[ P_{so} - 3P_o = 2IM3_o \geq 0 \]  

The output stage will dominate only for high \( G_{db} \). The IM3\(_o\) of plot 27 is appropriate for \( R_f = 1k \). This plot would also apply for additional signals brought into the inverting input of the output amplifier. The value of IM3\(_o\) for other values of \( R_f \) should be adjusted by subtracting \( 10 \cdot \log(R_f/1k) \) from the value determined from plot 27 at the operating frequency of interest. This will approximately account for the change in loop gain in the output amplifier for different values of \( R_f \).

This model for predicting the 3rd order spurious powers only holds for operation in the linear region of the CLC522. The principal limit in operating region is directed at not exceeding \( I_{TAIL} \) at the input for the peak value of the input 2-tone sinusoidal waveform. For equal powers (\( P_o \)) at the matched load, equation 23 computes the peak \( I_{R_g} \) through the gain setting resistor, \( R_g^* \).

\[ \frac{1}{R_g} = 2000 \left[ 0.002 \cdot 10^{ \left( \frac{P_{so} + 6 - G_{db}}{10} \right)} \right] \text{ mA} \]  

**Eq. 23**

Test data on the CLC522 indicates that this model for the output 2-tone spurious power holds well for \( I_{R_g(peak)} < 2.2mA \).

As an example, consider calculating the 3rd order 2-tone spurious power levels for the following set of conditions -

- A\(_{vmax}\) = 20V/V (26dB) to output pin:
- 20dB to matched load
- \( R_f = 2.5k \) to yield enough gain for \( I_{TAIL} \) to get 4V\(_{pp}\)
- \( R_g = 231 \Omega \) to satisfy 1.85 \( \cdot \) \( R_f/R_g = 20 \) (physical \( R_g = 229 \Omega \))
- Attenuation (\( V_g = 0 \)) operating gain to load = 5\(_{dB}\) (14dB)
- \( P_o = 4\text{dBm} \text{ (1V}_{pp}\text{ each tone, 2V}_{pp}\text{ for the 2-tone envelope) } \)
- \( F_o = 20\text{MHz} \text{ (Test frequencies at 20MHz} \pm 100\text{kHz) } \)

From this, various limits to operation should be checked.

- Total output pin voltage swing \( \rightarrow \pm 2\text{V into 100\text{\Omega} } \)
- Peak output current \( \rightarrow 2/100 = 20\text{mA} \)
- Peak slew rate at output \( \rightarrow 2\text{V} \cdot (2\text{mA} \cdot 20\text{MHz}) = 251\text{V/msec} \)
- Peak current in \( R_g \) \( \rightarrow (2/5) / 231 = 1.73\text{mA} \)

All of these are within the operating range of the CLC522. The output 3rd order spurious may now be calculated using the expressions developed previously.
\[ IM3_o = 40\text{dBm} - 10\log(2500/1000) = 36\text{dBm} \]
(from plot 27 adjusted for \( R_f = 2.5k \))

\[ IM3_i = 16\text{dBm} \]
(from plot 27 at 20MHz)

\[ P_{so} = 3\times4 - 2\times36 = -60\text{dBm} \]
(output amplifier term)

\[ P_{so} = 3 \times 4 - 2 \times (17 + 20 - 6 + 6.6) = -63.2\text{dBm} \]
(input amplifier term)

\[ P_{st} = 10\times\log(10^{-60/10} + 10^{-63.2/10}) = -58.3\text{dBm} \]
(combination of input and output spurious contributions)

In this case, the output amplifier is setting the 2-tone spurious level. The delta from the 4dBm single tone power level to the spurious power is 4 - (-58.3) = 62.3dBc. Note also that the 2.5kΩ feedback resistor will drop the bandwidth to 49MHz (from plot 6).

**-1dB Compression**

This performance measure, like 2-tone intercept, is defined for the power at a matched 50Ω load. The plot of input and output -1dB compression (plot 30) is therefore for a power that is across a 50Ω resistor to ground with an additional 50Ω series resistor from the output pin of the CLC522 to this load resistor. The -1dB compression power is tested by sweeping the input power, at a fixed frequency, and observing where the output power is 1dBm less than what the low power gain would predict. This measurement is then repeated over a range of frequencies. The reported -1dB compression power is this actual measured power plus the 1dB it has been compressed.

Again, there is both an input and an output limit that can determine the -1dB compression. The output amplifier’s voltage swing limit will set the -1dB compression point when the available signal current through the multiplier core times \( R_f \) will exceed the swing limit in the output amplifier. For an output limited case, \( R_f \times I_{TAIL} \times (V_g+1)/2 > V_{omax} \). Hence, output limiting can occur principally for higher \( R_f \)'s and at maximum gain settings. For the maximum gain case of plot 30, an output limited compression is obtained for \( R_f = 1.4kΩ \) while an input limited operation is obtained for \( R_f = 900Ω \). When a swing limit has been reached at lower frequencies, either for an output voltage or input \( R_g \) current limit, the output waveform approaches a square wave for a sinusoidal input. At these low frequencies (<40MHz) and for any gain setting, the -1dB compression power at the matched 50W load will be the minimum of -

a. \( 16.8\text{dBm} \) (due to output amplifier voltage swing limits)

or

b. \( 13.1\text{dBm} + 20 \times \log(1.85 \times I_{TAIL} \times R_f \times (V_g+1)/4) \) (input limited)

It is interesting to note that, once \( V_g \) has been reduced to cause the input limit to set the output -1dB compression, the output compression will decrease directly with signal gain. Figure 6 shows this clearly where the output -1dB compression over frequency shifts directly with gain setting when the input limit is setting the available output power.

![-1dB Compression vs. Gain Adjust](http://www.national.com)

**Advanced Applications**

Each of the following applications circuits exploit one or several unique feature in the CLC522. Please contact the Comlinear applications group for additional information on any of these applications.

**Differential Amplier**

The two buffers at the input of the CLC522 provide a high input impedance, matched frequency response path, for implementing a differential amplifier (see Figure 2). Any differential signal impressed across \( R_g \) is transformed into a single ended current signal through \( R_g \). This provides an exceptional differential to single ended conversion right at the input stage. With the added flexibility of being an adjustable gain part, the CLC522 can be used to implement a very wideband differential amplifier. Application note OA-16 discusses this application for both the CLC522 and CLC520.

**Differential Line Equalizing Receiver**

Extending the idea of a differential amplifier to a line receiver, and recognizing that the gain setting element can be used to shape the frequency response, an equalizing receiver can be easily implemented as shown in Figure 7.

The gain setting network shown in figure 12 implements a series of zero/pole pairs that can be placed to compensate the \( 1/\sqrt{f} \) rolloff typically seen in long coax cables. At low frequencies, the gain starts out set by only \( R_{90} \).
The resistor & capacitor values are set such that C3, C2, and C1 short out sequentially – smoothly increasing the gain by placing a decreasing impedance in parallel with $R_{go}$. Additional RC pairs can be added to improve the approximation. In this circuit, the maximum high frequency current in the gain setting network will be set by $R_{g1}||R_{go}$. It is important to check that $I_{T\text{AIL}}$ is not exceeded when a high frequency input differential signal is placed across this $R_{g1}||R_{go}$ minimum impedance.

![Figure 7: Wideband, Equalizing, Differential Cable Receiver with Adjustable Gain](image)

**DAC Transimpedance Interface**

Most high speed DAC’s are complementary current output devices where the output is actually sinking current into the DAC. From a fixed maximum current available, the digital codes act to steer how this total current is split between the two outputs. By pulling these two currents directly out of the CLC522 buffer outputs (pins 4 and 5), the CLC522 can be easily used to perform an adjustable gain complementary current to single ended voltage conversion. An example of this is shown in Figure 8.

![Figure 8: DAC Differential Transimpedance Interface](image)

This circuit actually implements a very wideband multiplying DAC function. Instead of scaling the IT current internal to the DAC, this circuit uses the CLC522’s $V_g$ input to scale the DAC current that goes to the CLC522’s transimpedance stage. It is important to note that for $V_g = 0$ the output is not at zero nor does the output polarity invert as $V_g$ goes < 0V. This is then a multiplying DAC in the sense that $V_g$ can be used to compress the gain from the DAC codes to output voltage swing.

This approach provides an exceptionally low impedance load with no compliance voltage problems at the output of the DAC. The +0.9V DC reference on the buffer inputs compensates for a 0.9V drop from the buffer inputs to their outputs and allows the DAC currents sources to drive into a 0 volt low impedance load. The two 5k resistors to the $+V_{CC}$ supply provide a 1mA bias to compensate part of the internal 1.8mA $I_{T\text{AIL}}$. This increases the maximum value allowed for the DAC output current to 3mA before non-linear internal limiting will occur in the CLC522. $R_g$ should be set to relatively high value but plays no role in setting the signal gain in this case.

**Using the CLC522 as a Feedback Element for Another Op Amp**

One approach to extending the gain adjustment range for the CLC522 is to imbed the adjustable gain stage as the feedback element for either a voltage or current feedback op amp. Figure 9 shows this topology along with some example component values using the CLC404 current feedback op amp.

![Figure 9: Using the CLC522 as the a Feed Element](image)

This circuit offers several advantages and disadvantages (over simply using the CLC522 as an adjustable gain stage) in applications where it is desired to hold a constant peak to peak output swing. The principal advantage for this circuit is that the peak input swing into the CLC522 is constant. This eliminates the gain adjust range limitations discussed earlier. Equation 24 shows the overall transfer function ignoring the bandwidth limitations of the CLC522.
This transfer function shows that the forward gain now depends on the inverse of the gain through the CLC522. Hence, to get high forward gain, the CLC522 needs to be operating as an attenuator. Some of this attenuation is provided by the resistor divider (\( \alpha \)) from the output of the forward op amp. The linear gain adjust characteristic of the CLC522 has been transformed to a 1/x type transfer gain. If \( V_g \) were adjusted to -1, shutting the CLC522 off, the forward path will go open loop and have a gain equal to \( Z(s)/R_c \).

Equation 24 also shows that the loop gain equation has become a purely voltage feedback type characteristic showing a gain-bandwidth product – even when using a current feedback op amp. A current feedback forward stage is preferred, however, to provide superior large signal swing and to allow easy frequency response compensation through adjusting the value of \( R_c \). The input referred noise has been increased since it now becomes the output noise of the CLC522. However, as the input peak to peak signal decreases, the gain is increased by decreasing the CLC522 gain. This will have the effect of decreasing the input referred noise as the input signal level decreases.

**Voltage Squaring Circuit**

Figure 10 shows a way of using the CLC522 to square an input signal voltage. The specific values used in this example will scale the output by a 2X multiple of \( V_i \).

This circuit applies the signal input to both the gain adjust pin and the non-inverting input pin. A wideband dual amplifier, the CLC412, is used to both sum the signal and a correction factor for the \(-V_{EE}\) supply in an inverting summing stage and to invert the signal again to the correct polarity for driving the \( V_g \) input of the CLC522. Stepping through the algebra to get \( V_o/V_i \) yields -

\[
V_o/V_i = 1.85 \cdot (R_f/R_g) \cdot 0.5 \cdot (1 - V_g/(2 \cdot V_{EE}))
\]

Substituting in \( V_g = V_i + 0.2 \cdot V_{EE} \) from Figure 10

\[
V_o = 1.85 \cdot (R_f/R_g) \cdot 0.5 \cdot (1 - V_i/(2 \cdot V_{EE}))
\]

This circuit will square the input voltage for \( V_i > 0 \), but will yield 0V output for \( V_i < 0 \).

**4 - Quadrant Multiplier**

The CLC522 is principally intended as a 2-quadrant multiplier. Although bipolar inputs at either of the two buffer inputs will pass on to the output as bipolar signals, inputs into the \( V_g \) input can only compress the gain for the signal channel inputs. In other words, with a fixed DC signal channel input, bipolar inputs on the \( V_g \) channel do not generate bipolar output signals. However, by summing the non-inverting input buffer signal directly into the inverting input of the output amplifier (in parallel with the internal gain adjusted signal), a 4 - quadrant multiplier can be emulated. Figure 11 shows this application along with the design equations -

\[
V_o = \frac{V_g}{2} \cdot \left( 1.85 \cdot \frac{R_f}{R_g} \right) \cdot \left( \frac{2R_g}{1.85} \right) \text{ scale factor}
\]

http://www.national.com
This circuit is particularly suitable at lower frequencies (< 5MHz). As the frequency increases, unequal delays between the internal and external signal paths reduce its effectiveness. In a mixer application, this translates into a decreased LO suppression at higher frequencies.

Wide Dynamic Range 1/2 Wave Rectifier
If a bipolar signal is applied to the signal inputs of the CLC522 and that same signal is used to toggle a comparator that switches the gain control channel from maximum gain to full attenuation, a simple and effective 1/2 wave rectifier may be implemented. Figure 12 shows an example of this application.

![Figure 12: 1/2 Wave Rectifier](image)

Most diode based rectifier circuits suffer from a signal level dependent frequency response. The circuit of Figure 12 relies upon the polarity of the current into the inverting input of a high speed current feedback clipping amplifier (the CLC501) to switch the CLC522's gain control input from full on to full off. In this case, negative 1/2 cycle of a sinusoidal signal cause the CLC501 to drive to the positive clamp passing those negative 1/2 cycles on to the CLC522 output. Since the input has been connected up to the inverting buffer side, these negative 1/2 cycles are passed to the output of the CLC522 as positive 1/2 cycles.

The signal amplitude range that will produce good rectified outputs depends only on how good the comparator is driving the gain adjust input. In the circuit of Figure 12, the full open loop gain of the CLC501 is available to respond to a switch in the polarity of the current into its inverting node. An alternative high speed voltage controlled comparator could also be used. The speed of operation is primarily limited by how fast the comparator can respond to a change in polarity at its input.

Adjustable Cutoff, Single Pole, Low Pass Filter
By putting the adjustable gain CLC522 inside the loop of an integrator stage, a variable cutoff low pass filter may be implemented. Figure 13 shows the generalized analysis of this technique.

![Figure 13: Tuneable Single Pole Low Pass Filter](image)

This circuit implements an inverting gain stage with a DC gain of \(-R_2/R_1\). Varying \(K\) has the effect of raising and lowering the open loop forward gain which has been given a pure integrator shape by the input voltage feedback op amp. Shifting the open loop gain up and down will vary the closed loop bandwidth when the feedback gain is fixed by \(R_1\) and \(R_2\). A specific example of this circuit is shown in Figure 14.

![Figure 14: Adjustable Bandwidth Amplifier](image)

This particular configuration provides a gain of -2 with a 10MHz cutoff when the CLC522 is at maximum gain (\(V_g = 1\)). As the gain is decreased the bandwidth will decrease directly. For a fixed output voltage swing, \(V_{opp}\), decreasing the bandwidth by dropping the CLC522 gain will increase the voltage swing at the input of the CLC522. Given this desired \(V_{opp}\), the available range of bandwidth reduction, before the input range of the CLC522 is exceeded, will be set by \(2 \times I_{TAIL} \times R_f/V_{opp} = BW_{max}/BW_{min}\) (Please see the discussion of usable gain adjust range).
CLC522 Typical Performance (T_A=25°C, V_cc=±5V, A_v=±10V/V, R_f=100Ω, V_g=1.1, unless noted)

Freq Response vs. Gain (A_v max=2V/V)

Freq Response vs. Gain (A_v max=10V/V)

Freq Response vs. Gain (A_v max=100V/V)

PSRR and CMRR (Input Referred)

Feedback Resistor (R_f) vs. Bandwidth

Gain Flatness & Linear Phase Deviation

Phase vs. Gain Adjustment

Large Signal Frequency Response

Large & Small Signal Pulse Response

Gain Control Settling Time & Delay

Gain Control Channel Feedthrough

Short Term Settling Time
CLC522 Typical Performance (T_a=25°C, VCC=±5V, A_v=+10V/V, R_f=100Ω, V_g=1.1, unless noted)
CLC522 Electrical Characteristics

\( \pm V_{cc} = \pm 5V, R_L = 100\Omega, R_f = 1k\Omega, R_g = 182\Omega, A_{\text{max}} = +10V/V, V_g = +1.1V \)

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**FREQUENCY RESPONSE**

|                      |                     | 165  | 115  | 110  | 120  | 110  | MHz  | SSBW |
|                      |                     | 150  | 95   | 100  | 100  | 90   | MHz  | LSBW |
|                      |                     | 165  | 115  | 110  | 120  | 110  | MHz  |       |
|                      |                     | 0    | 0.1  | 0.1  | 0.1  | 0.1  | dB   | GFPL |
|                      |                     | 0.05 | 0.25 | 0.4  | 0.25 | 0.25 | dB   | GFR  |
|                      |                     | 1    | 1.3  | 1.0  | 1.0  | 1.0  | dB   | GFPH |
|                      |                     | 0.5  | 1.1  | 1.2  | 1.0  | 1.2  | deg  | LPD  |
|                      |                     | -62  | -57  | -57  | -57  | -57  | dB   | FDT  |

**TIME DOMAIN RESPONSE**

|                      |                     | 2.2  | 3.0  | 2.9  | 2.9  | 3.2  | ns   | TRS  |
|                      |                     | 3.0  | 5.0  | 5.0  | 5.0  | 5.0  | ns   | TRL  |
|                      |                     | 12   | 18   | 18   | 18   | 18   | ns   | TSP  |
|                      |                     | 2    | 15   | 15   | 15   | 15   | %    | OS   |
|                      |                     | 2000 | 1400 | 1400 | 1400 | 1400 | V/µsec | FDT  |

**DISTORTION AND NOISE PERFORMANCE**

|                      |                     | -50  | -44  | -44  | -44  | -44  | dB   | HD2  |
|                      |                     | -132 | -129 | -130 | -130 | -129 | dBm/Hz | SNF  |
|                      |                     | 58   | 65   | 62   | 62   | 68   | nV/√Hz | INV  |

**STATIC DC PERFORMANCE**

|                      |                     | 0.04 | 0.1  | 0.1  | 0.1  | 0.1  | %    |     |
|                      |                     | 0.5  | 2.2  | 3.0  | 2.0  | 2.5  | %    |     |
|                      |                     | 15   | 47   | 82   | 38   | 38   | µA   |     |
|                      |                     | 125  | 300  | 600  | ---  | 210  | nA/C |     |
|                      |                     | -0.0 | -0.5 | +0.5,-1.0 | -0.5 | -0.5 | dB   |     |
|                      |                     | 25   | 95   | 120  | 85   | 90   | mV   |     |
|                      |                     | 100  | 350  | 400  | ---  | 360  | µV/C |     |
|                      |                     | 9    | 26   | 45   | 21   | 21   | µA   |     |
|                      |                     | 65   | 175  | 275  | ---  | 125  | nA/C |     |
|                      |                     | 0.2  | 3.0  | 4.0  | 2.0  | 2.0  | µA   |     |
|                      |                     | 5    | 30   | 40   | ---  | 20   | nA/C |     |
|                      |                     | 10   | 40   | 40   | 40   | mV/V |     |
|                      |                     | 70   | 59   | 59   | 59   | 59   | dB   | CMRR |
|                      |                     | 46   | 62   | 63   | 61   | 61   | mA   | ICC  |

**MISCELLANEOUS PERFORMANCE**

|                      |                     | 1500 | 450  | 175  | 650  | 650  | kΩ   | RIN  |
|                      |                     | 1.0  | 2.0  | 2.0  | 2.0  | 2.0  | pF   | CIN  |
|                      |                     | 1.8  | 1.26 | 1.37 | 1.37 | 1.15 | mA   |     |
|                      |                     | -2.2 | -1.2 | -1.4 | -1.2 | -1.2 | V    |     |
|                      |                     | 100  | 30   | 15   | 38   | 38   | kΩ   |     |
|                      |                     | 1.0  | 2.0  | 2.0  | 2.0  | 2.0  | pF   |     |
|                      |                     | 0.1  | 0.3  | 0.6  | 0.2  | 0.2  | Ω    | RO   |
|                      |                     | -4.0 | -3.6 | -3.5 | -3.7 | -3.7 | V    | VO   |
|                      |                     | -70  | -40  | -25  | -47  | -47  | mA   | IO   |

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as Noted. Outgoing quality levels are determined from tested parameters.
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