AN-329 Implementing an 8-Bit Buffer in COPS
Implementing an 8-Bit Buffer in COPS™

Sometimes a COP microcontroller must input and/or output 8-bit data; for instance, when handling ASCII data. In some applications, the processor must also provide temporary storage for 8-bit data before it is output. The COP instruction set and RAM structure lend themselves very nicely to providing a 32 digit, 8-bit buffer for a solution to these applications.

Such a large buffer is possible using a COP440 or a COP444L. The other members of the COP400 family with half as much RAM as these two would provide a 16 digit 8-bit buffer using the techniques described in this example. Four adjacent RAM registers (16 digits each) are required. Referring to Figure 1, registers 4, 5, 6, and 7 are used for the buffer. Each RAM location contains 4 bits, so 2 locations will be used to store a byte of data. But these RAM locations are not adjacent to each other. You will note that the MSD of digit number 0A hex is in RAM location (4, A) while the LSD of the same digit is in RAM location (6, A). The 2 RAM locations CHARM and CHARL are used for temporary storage of an 8-bit value.

In addition, 4 RAM locations are used for buffer pointers: those labelled IPM and IPL are the MSD and LSD of the input pointer, and those labelled OPM and OPL are the MSD and LSD of the output pointer. Each pointer’s function is to store an 8-bit counter whose value ranges from 00 hex thru 1F hex. The input pointer’s value is used for storing the temporary storage buffer contents into the digit with the same number. For example, if the input pointer equals 14 hex, then the contents of CHARM would be stored in RAM location (5, 4) and the contents of CHARL would be stored in RAM location (7, 4). The output pointer’s value is used for retrieving a digit from the buffer and putting it in CHARM and CHARL. For instance, if the output pointer equals 05 hex, then the contents of RAM location (4, 5) would be transferred to CHARM and the contents of RAM location (6, 5) would be transferred to CHARL.

A simple example of one possible application of the buffer is flowcharted in Figure 2. In this example, data is input to CHARM and CHARL, then stored in the buffer. An output device (a printer) is checked to see if it is ready to receive data. If it is, data is brought out of the buffer and put in CHARM and CHARL for output to the printer.

Pages 3 and 4 contain a listing of the subroutines needed to perform the data transfers in the 32-digit, 8-bit buffer.
FIGURE 2. Buffer Example Flowchart

- **DATA READY TO BE INPUT?**
  - **NO**
  - **YES**
    - **BUFFER EMPTY?**
      - **NO**
        - **INPUT DATA TO CHAR**
      - **YES**
        - **PUT CHAR IN BUFFER (USRIP.Chrome)**
        - **INCREMENT IP (USRIP.INCIP)**
          - **NO**
            - **PRINT READY?**
              - **NO**
                - **BUFFER FULL?**
                  - **NO**
                    - **BRING MEM (IP) OUT OF BUFFER (USRIP.MTBH)**
                  - **YES**
                    - **INCREMENT IP (USRIP.INCIP)**
        - **OUTPUT CHAR TO PRINTER**
        - **CHAR = CHAR AND CHARL**
        - **IP = IPM AND IPL**
        - **OP = QPM AND QPL**
BUFFER

;**************************************
;*** 8-BIT RAM BUFFER SUBROUTINES ***
;***
;**************************************

;THESE ARE SUBROUTINES FOR IMPLEMENTING A 32 BYTE
;BUFFER IN A COP440 OR COP444L RAM 9/3/82

01BC .CHIP 444

.TITLE BUFFER

002D CHARM = 2,13 ;TEMPORARY STORAGE BUFFER MSD
002C CHARL = 2,12 ;TEMPORARY STORAGE BUFFER LSD
002F IPM = 2,15 ;INPUT POINTER MSD
002E IPL = 2,14 ;INPUT POINTER LSD
003F OPM = 3,15 ;OUTPUT POINTER MSD
003E OPL = 3,14 ;OUTPUT POINTER LSD
0000 00 CLRA

080 .PAGE 2

MTOC IS A SUBROUTINE THAT TRANSFERS M(OPM) AND M(OPL) TO
CHARM AND CHARL

080 233E MTOC: LDD OPL ;LOAD LSD OUTPUT POINTER
082 50 CAB ;WHICH IS BD
083 233F LDD OPM ;LOAD MSB OUTPUT POINTER FOR B
085 54 AISC 4 ;MAKE BR EQUAL 4 OR 5
086 12 XABR
087 25 LD 2 ;LOAD M(OPM), MAKE BR = 6 OR 7
088 23AD XAD CHARM ;M(OPM) TO CHARM
08A 05 LD ;LOAD M(OPL)
08B 23AC XAD CHARL ;M(OPL) TO CHARL
08D 48 RET

CTOM IS A SUBROUTINE THAT TRANSFERS CHARM AND CHARL TO
M(IPM) AND M(IPL)

08E 233E CTOM: LDD IPL ;LOAD MSD INPUT POINTER
090 50 CAB ;WHICH IS BD
091 233F LDD IPM ;LOAD MSD INPUT POINTER FOR BR
093 54 AISC 4 ;MAKE BR = 4 OR 5
094 12 XABR
095 232D LDD CHARM ;LOAD MSD TEMP STORAGE
097 26 X 2 ;TO M(OPM), MAKE BR = 6 OR 7
098 232C LDD CHARL ;LOAD MSD TEMP STORAGE
09A 06 X ;TO M(OPL)
09B 48 RET

;
COP CROSS ASSEMBLER PAGE: 2

BUFFER

46 .FORM
47 ;INCREMENTS INPUT POINT OR OUTPUT POINTER, ROLLS OVER
48 ;AT 1F HEX
49 09C 2D INCIP: LBI IPL ;POINT TO LSD OF POINTER
50 09D 3D INCOIP: LBI OPL
51 09E 22 SC ;C=1 FOR INCREMENT
52 09F 00 CLRA
53 0A0 30 ASC ;INCREMENT RAM VALUE
54 0A1 44 NOP ;NEGATES SKIP CONDITION
55 0A2 04 XIS ;STORE AND POINT TO (X,F)
56 0A3 00 CLRA
57 0A4 30 ASC ;PROPAGATE CARRY, IF ANY, TO MS
58 0A5 44 NOP
59 0A6 06 X ;STORE
60 0A7 45 RMB 1 ;ROLL OVER AT X'1F
61 0A8 48 RET
62 
63 
64 .END

COP CROSS ASSEMBLER PAGE: 3

BUFFER

CHRL 002C CHARM 002D CTOM 008E * INCIP 009C *
INCOIP 009D * IPL 002E IPM 002F MTOC 0080 *
OPL 003E 003F
NO ERROR LINES
42 ROM WORDS USED
COP 444 ASSEMBLY
SOURCE CHECKSUM = D6A5
INPUT FILE 6:RBUFFC.SRC VN: 5

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