DS3680, DS75451

AN-213 Safe Operating Areas for Peripheral Drivers

Literature Number: SNOA610
Peripheral Drivers is a broad definition given to Interface Power devices. The devices generally have open-collector output transistors that can switch hundreds of milliamps at high voltage, and are driven by standard Digital Logic gates. They serve many applications such as: Relay Drivers, Printer Hammer Drivers, Lamp Drivers, Bus Drivers, Core Memory Drivers, Voltage Level Transistors, and etc. Most IC devices have a specified maximum load such as one TTL gate can drive ten other TTL gates. Peripheral drivers have many varied load situations depending on the application, and requires the design engineer to interpret the limitations of the device vs its application. The major considerations are Peak Current, Breakdown Voltage, and Power Dissipation.

OUTPUT CURRENT AND VOLTAGE CHARACTERISTICS

Figure 1 shows the circuit of a typical peripheral driver, the DS75451. The circuit is equivalent to a TTL gate driving a 300 mA output transistor. Figure 2 shows the characteristics of the output transistor when it is ON and when it is OFF. The output transistor is capable of sinking more than one amp of current when it is ON, and is specified at a \( V_{OL} \approx 0.7 \text{V} \) at 300 mA. The output transistor is also specified to operate with voltages up to 30V without breaking down, but there is more to that as shown by the breakdown voltages labeled BVCES, BVCER, and LVCEO.

OUTPUT TRANSFER CHARACTERISTICS VS INDUCTIVE AND CAPACITIVE LOADS

Figure 3 shows the switching transfer characteristics super-imposed on the DC characteristics of the output transistor for an inductive load. Figure 4 shows the switching transfer characteristics for a capacitor load. In both cases in these examples, the load voltage \( (V_L) \) exceeds LVCEO. When the output transistor turns on with an inductive load the initial current through the load is 0 mA, and the transfer curve switches across to the left \( (V_{OL}) \) and slowly charges the inductor. When the output transistor turns off with an inductive load, the initial current is \( I_{OL} \), which is sustained by the inductor and the transistor curve switches across to the right \( (V_L) \) through a high current and high voltage area which exceeds LVCEO and instead of turning off (shown as dotted line) the device goes into secondary breakdown. It is generally not a good practice to let the output transistor’s voltage exceed LVCEO with an inductive load.

In a similar case with a capacitive load shown in Figure 4, the switching transfer characteristics rotate counter-clockwise through the DC characteristics, unlike the inductive load which rotated clockwise. Even though the switching transfer curve exceeds LVCEO, it didn’t go into secondary breakdown. Therefore, it is an acceptable practice to let the output transistor voltage exceed LVCEO, but not exceed BVCER with a capacitive load.
Figure 3 shows an acceptable application with an inductive load. The load voltage \( V_B \) is less than \( LVCEO \), and the inductive voltage spike caused by the initial inductive current is quenched by a diode connected to \( V_B \).

Figure 6 shows the switching transfer characteristics of a capacitive load which leads to secondary breakdown. This condition occurs due to high sustained currents, not breakdown voltage. In this example, the large capacitor prevented the output transistor from switching fast enough through the high current and high voltage region; in turn the power dissipation of the device was exceeded and the output transistor went into secondary breakdown.

Figure 7 shows another method of quenching the inductive voltage spike caused by the initial inductive current. This method dampens the switching response by the addition of \( R_D \) and \( C_D \). The values of \( R_D \) and \( C_D \) are chosen to critically dampen the values of \( R_L \) and \( L_L \); this will limit the output voltage to:

\[
2 \times V_B \left( \frac{L_L}{R_L + R_D} \right) \leq 0.5
\]

Figure 8 shows a method of reducing high sustaining currents in a capacitive load. \( R_D \) in series with the capacitor \( C_L \) will limit the switching transistor without affecting final amplitude of the output voltage, since the IR drop across \( R_D \) will be zero after the capacitor is charged.

As an additional warning, beware of parasitic reactance. If the driver’s load is located some distance from the driver (as an example: on the enclosure panel or through a con-
necting cable) there will be additional inductance and capacitance which may cause ringing on the driver output which will exceed LVCEO or transient current that exceeds the sustaining current of the driver. A 300 mA current through a small inductor can cause a good size transient voltage, as compared with 20 mA transient current observed with TTL gates. For no other reason than to reduce the noise associated with these transients, it is good practice to dampen the driver’s output.

In conclusion, transient voltage associated with inductive loads can damage the peripheral driver, and transient currents associated with capacitive loads can also damage the driver. In some instances the device may not exhibit failure with the first switching cycle, but its conditions from ON to OFF will worsen after many cycles. In some cases the device will recover after the power has been turned off, but its long term reliability may have been degraded.

POWER DISSIPATION

Power Dissipation is limited by the IC Package Thermal Reactance and the external thermal reactance of the environment (PC board, heat sink, circulating air, etc.). Also, the power dissipation is limited by the maximum allowable junction temperature of the device. There are two contributions to the power: the internal bias currents and voltage of the device, and the power on the output of the device due to the Driver Load.

POWER LIMITATIONS OF PACKAGE

Figure 9 shows the equivalent circuit of a typical power device in its application. Power is shown equivalent to electrical current, thermal resistance is shown equivalent to electrical resistance, the electrical reactance C and L are equivalent to the capacity to store heat, and the propagation delay through the medium. There are two mediums of heat transfer: conduction through mass and radiant convection. Convection is insignificant compared with conduction and isn’t shown in the thermal resistance circuits. From the point power is generated (device junction) there are three possible paths to the ultimate heat sink: 1) through the device leads; 2) through the device surface by mechanical connection; and 3) through the device surface to ambient air. In all cases, the thermal paths are like delay lines and have a corresponding propagation delay. The thermal resistance is proportional to the length divided by the cross sectional area of the material. The Thermal Inductance is proportional to the length of the material (copper, molding compound, etc.) and inversely proportional to the cross sectional area. The thermal capacity is proportional to the volume of the material.

![Figure 8. Capacitive Load with Current Limiting Resistor](image1)

![Figure 9. Thermal Reactance from Junction to Ambient](image2)
National Semiconductor specifies the thermal resistance from device junction through the device leads soldered in a small PC board, measured in one cubic foot of still air. Figure 11 shows the maximum package power rating for an 8 pin Molded, an 8 pin Ceramic, 14 pin Molded and a 14 pin Ceramic package. The slope of the line corresponds to thermal resistance ($\phi_{JA} = \Delta P/\Delta T$).

Figure 11 shows that 14 pin packages have less thermal resistance than 8 pin packages; which should be expected since it has more pins to conduct heat and has more surface area. Something that may not be expected is that the thermal Resistance of the molded devices is comparable to the ceramic devices. The reason for the lower thermal resistance of the molded devices is the Copper lead frame, which is a better thermal conductor than the Kovar lead frame of the ceramic package. Almost all the peripheral drivers made by National Semiconductor are constructed with Copper lead frames (refer to $\phi_{JA}$ on the specific devices data sheet). The difference between the thermal resistance of Copper and Kovar in a molded package is shown in Figure 12.

Another variance in thermal resistance is the size of the IC die. If the contact area to the lead frame is greater, then the thermal resistance from the Die to the Lead Frame is reduced. This is shown in Figure 13. The thermal resistance shown in Figure 11 corresponds to die that are 6000 mil$^2$ in area.

In most applications the prime medium for heat conduction is through the device leads to the PC board, but the thermal resistance can be significantly improved by cooling air driven across the surface of the package. The conduction to air is limited by a stagnant film of air at the surface of the package. The film acts as an additional thermal resistance. The thickness of the film is proportional to its resistance. The thickness of the film is reduced by the velocity of the air.
Most IC devices (such as T2L) operate at power levels well due to variables in assembly and package material. That the 10 outputs could sink 300 mA with a VOL of 1 volt, board it is mounted on. The DS3654 data sheet indicated destroyed in moments, and may even burn a hole in the PC 0.8 watt package. In this example, the device would be de-
dissipate 3 watts (DC and, even more AC), and it is only in a
example, the DS3654 Ten Bit Printer Driver could
dissipate 11 watts. After 15 minutes of operation, the driver succumbs to thermal overload and becomes non-functional. The DS3654 has an internal clamp net-
works to quench the inductive back swing at 60V. At 5 Hz the
device dissipates 2 watts, with transient peaks up to 11
hours. At 15 minutes of operation, the driver succumbs to thermal overload and becomes non-functional. The DS3654
was intended for telephone relay, which in most applications switches 20 times a day.
Peripheral driver will dissipate peak power levels that greatly exceed the average DC power. This is due to the capacity of the die and package to consume the transient energy while still maintaining the junction temperature at a safe level.

**FIGURE 14. Thermal Resistance vs Air Velocity**
The thermal resistance can also be improved by connecting the package to the PC board copper or by attaching metal wings to the package. The improvement by these means is outside the control of the IC manufacturer, but is available from the manufacturer of the heat sink device. If the IC is mounted in a socket rather than soldered to a PC board, the thermal resistance through the device leads will worsen. In most cases, the thermal resistance is increased by 20%; again this is a variable subject to the specific socket type.

The maximum package rating shown in this note corresponds to a 90% confidence level that the package will have thermal resistance equal to or less than the value shown. The thermal resistance varies ±5% about the mean due to variables in assembly and package material.

**CALCULATIONS OF POWER DISSIPATION**
Most IC devices (such as T2L) operate at power levels well below the device package rating, but peripheral drivers can easily be used at power levels that exceed the package rating unknowingly, if the power dissipation isn’t calculated. As an example, the DS3654 Ten Bit Printer Driver could dissipate 9 watts (DC and, even more AC), and it is only in a 0.8 watt package. In this example, the device would be destroyed in moments, and may even burn a hole in the PC board if it is mounted on. The DS3654 data sheet indicated that the 10 outputs could sink 300 mA with a VOL of 1 volt, but it wasn’t intended that all the outputs would be sinking this current at the same time, and if so, not for a long period. The use of the DS3654 requires that the power be calculated vs the duty cycle of the outputs.

The DC power dissipation is pretty obvious, but in another example, a customer used the DS3686 relay driver to drive 6.5h inductive load. The DS3687 has an internal clamp network to quench the inductive back swing at 60V. At 5 Hz the device dissipates 2 watts, with transient peaks up to 11 watts. After 15 minutes of operation, the device might in some circuits negate the effect of the resistors TC. Peripheral output transistors have a positive TC associated with the load generally have a positive. On the other hand, diodes and transistor emitter base voltages have a negative TC which may in some circuits negate the effect of the resistors TC. Peripheral output transistors have a positive TC associated with VOL; while output Darlington transistors have a negative TC at low currents and may be flat at high currents. Figure 15 shows an example of power dissipation vs temperature; note that the power dissipation at the application’s maximum temperature (TA) was less than the power dissipation at lower temperatures. Since maximum junction temperature is the concern of the calculation, then maximum ambient temperature power should be used. The junction temperature may be determined by projecting a line (shown dotted in Figure 15), with a slope proportional to dTA back to the horizontal axis (shown as Tj). If the point is below the curve then Tj will be less than 150°C. Tj must not exceed the maximum junction temperature for that package type. In this example, Tj is less than 150°C as required by a molded package. To calculate the power vs temperature, it is necessary to characterize the device parameters vs temperature. Unfortunately, this information is not always provided by IC manufacturers in the device data sheets. A method to calcu-
late I\textsubscript{CC} vs temperature is to measure a device, then normal-
ize the measurements vs the typical value for I\textsubscript{CC} in the data
sheet, then worst case the measurements by adding 30%. Thirty percent
is normally the worst-case resistor tolerance that IC devices are manufactured to.

FIGURE 16. IC Power Dissipation vs Temperature

CALCULATION OF OUTPUT POWER WITH
AN INDUCTIVE LOAD

For this example, the device output circuit is similar to the
DS3654 (10-Bit Printer Solenoid Driver) and the DS3686
and DS3687 (Telephone Relay Driver) as shown in Figure
17. Special features of the circuit type are the Darlington
output transistors Q1 and Q2 and the zener diode from the
collector of Q1 to the base of Q2. The Darlington output
requires very little drive from the logic gate driving it and in
turn dissipates less power when the output is turned ON and
OFF, than a single saturating transistor output would. The
zener diode (D\textsubscript{Z}) quenches the inductive backswing when
the output is turned OFF.

Device and Load Characteristics Used for
Power Calculation

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<th>Value</th>
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<td>Output Voltage ON</td>
</tr>
<tr>
<td>(V\text{\textsubscript{C}})</td>
<td>Output Clamp Voltage</td>
</tr>
<tr>
<td>(V\text{\textsubscript{B}})</td>
<td>Load Voltage</td>
</tr>
<tr>
<td>(R\text{\textsubscript{L}})</td>
<td>Load Resistance</td>
</tr>
<tr>
<td>(L\text{\textsubscript{L}})</td>
<td>Load Inductance</td>
</tr>
<tr>
<td>(T\text{\textsubscript{ON}})</td>
<td>Period ON</td>
</tr>
<tr>
<td>(T\text{\textsubscript{OFF}})</td>
<td>Period OFF</td>
</tr>
<tr>
<td>(T)</td>
<td>Total Period</td>
</tr>
</tbody>
</table>

\(V\text{\textsubscript{OL}} = 1.5\) V
\(V\text{\textsubscript{C}} = 65\) V
\(V\text{\textsubscript{B}} = 30\) V
\(R\text{\textsubscript{L}} = 120\) Ω
\(L\text{\textsubscript{L}} = 5\) H
\(T\text{\textsubscript{ON}} = 100\) ms
\(T\text{\textsubscript{OFF}} = 100\) ms
\(T = 200\) ms

Refer to Figure 18 voltage and current waveforms corre-
sponding to the power dissipation calculated for this exam-
ple of an inductive load.

\[
P\text{\textsubscript{ON}} = \text{Average power dissipation in device output}
\]

when device is ON during total period (\(T\))

\[
\tau = \frac{L\text{\textsubscript{L}}}{R\text{\textsubscript{L}}} = 41.7 \text{ ms}
\]

\[
I\text{\textsubscript{L}} = \frac{V\text{\textsubscript{B}} - V\text{\textsubscript{OL}}}{R\text{\textsubscript{L}}} = 237.5 \text{ mA}
\]

\[
I\text{\textsubscript{P}} = I\text{\textsubscript{L}} (1 - e^{-\frac{L\text{\textsubscript{ON}}}{L\text{\textsubscript{ON}}}})
\]

\[
I\text{\textsubscript{P}} = 237.5 \text{ mA} (1 - e^{-100 \text{ ms}/41.7 \text{ ms}})
\]

\[
I\text{\textsubscript{P}} = 215.9 \text{ mA}
\]

\[
P\text{\textsubscript{ON}} = V\text{\textsubscript{OL}} \times I\text{\textsubscript{L}} \times \frac{T\text{\textsubscript{ON}}}{T} \left[ 1 - \int_{0}^{\frac{T\text{\textsubscript{ON}}}{2}} e^{-\frac{t}{\tau}} \, dt \right]
\]

\[
P\text{\textsubscript{ON}} = V\text{\textsubscript{OL}} \times I\text{\textsubscript{L}} \times \frac{T\text{\textsubscript{ON}}}{T} \left[ 1 - \frac{\tau}{T\text{\textsubscript{ON}}} (1 - e^{-\frac{T\text{\textsubscript{ON}}}{\tau}}) \right]
\]

\[
P\text{\textsubscript{ON}} = 1.5 \times 237.5 \text{ mA} \times \frac{100}{200} \left[ 1 - \frac{41.7}{100} (1 - e^{-100/41.7}) \right]
\]

\[
P\text{\textsubscript{ON}} = 110.6 \text{ mW}
\]

\[
P\text{\textsubscript{OFF}} = \text{Average power dissipation in device output when}
\]

device is OFF during total period (\(T\))

\[
I\text{\textsubscript{R}} = \frac{V\text{\textsubscript{C}} - V\text{\textsubscript{B}}}{R\text{\textsubscript{L}}} = 291.7 \text{ mA}
\]

\[
t\text{\textsubscript{x}} = \frac{\tau}{n} \left( \frac{I\text{\textsubscript{P}} + I\text{\textsubscript{R}}}{I\text{\textsubscript{R}}} \right)
\]

\[
t\text{\textsubscript{x}} = 41.7 \text{ ms} \times n \left( \frac{215.9 + 291.7}{291.7} \right) = 23.1 \text{ ms}
\]

\[
P\text{\textsubscript{OFF}} = V\text{\textsubscript{C}} \times \frac{t\text{\textsubscript{x}}}{T} \left( I\text{\textsubscript{R}} + I\text{\textsubscript{P}} \right) \left( 1 - e^{-\frac{t\text{\textsubscript{x}}}{\tau}} \right) - I\text{\textsubscript{R}}
\]

\[
P\text{\textsubscript{OFF}} = V\text{\textsubscript{C}} \times \frac{t\text{\textsubscript{x}}}{T} \left( I\text{\textsubscript{R}} + I\text{\textsubscript{P}} \right) \left( 1 - e^{-\frac{t\text{\textsubscript{x}}}{\tau}} \right) - I\text{\textsubscript{R}}
\]

\[
P\text{\textsubscript{OFF}} = 65 \times \frac{23.1}{200} \left( 215.9 \text{ mA} + 291.7 \text{ mA} \right) \times \frac{41.7}{23.1}
\]

\[
(1 - e^{-23.1/41.7}) - 291.7 \text{ mA}
\]

\[
P\text{\textsubscript{OFF}} = 736 \text{ mW}
\]

\[
PO = \text{Average power dissipation in device output}
\]

\[
PO = P\text{\textsubscript{ON}} + P\text{\textsubscript{OFF}} = 110.6 + 736 = 846.6 \text{ mW}
\]

In the above example, driving a 120Ω inductive load at 5 Hz,
the power dissipation exceeded a more simple calculation
of power dissipation, which would have been:

\[
PO = V\text{\textsubscript{OL}} \times (V\text{\textsubscript{B}} - V\text{\textsubscript{OL}}) \times \frac{T\text{\textsubscript{ON}}}{T}
\]

\[
PO = 1.5 \times (30 - 1.5) \times \frac{100 \text{ ms}}{120} \times \frac{200 \text{ ms}}{182.5 \text{ mW}}
\]

An error 460% would have occurred by not including the
reactive load. The total power dissipation must also include
other outputs (if the device has more than one output), and
the power dissipation due to the device power supply cur-
rents. This is an example where the load will most likely
exceed the device package rating. If the load is fixed, the
power can be reduced by changing the period (\(T\)) and duty
rate (\(T\text{\textsubscript{ON}}/T\text{\textsubscript{OFF}}\)).
Figure 18 shows the transient response of a driver similar to a DS75451 driving the lamp characterized in Figures 19 and 20. The equivalent load doesn’t include the reactance of the lamp base to ambient, which has a 250 ms time constant, since 10 ms to an IC is equivalent to DC. The peak transient current was 1 amp, settling to 200 ms, with an 8 ms time constant. Observe the peak current is clamped at 1 amp, by the sinking ability of the driver; otherwise the peak current may have been 1.2 amps. The DS75451 is only rated at 300 mA, but it is reasonable to assume it could sink 1 amp because of the designed force $B$ required for switching response and worst case operating temperature.

Figure 21 shows the transient response of an Incandescent Lamp. Calculation of the energy dissipated by a peripheral driver for the transient lamp current shown in Figure 21 is shown above, and the plot of energy vs time is shown in Figure 22. Figure 22 also includes as a reference the maximum peak energy from Figure 15. It can be seen from Figure 22 that in this example there is a good safety margin between the lamp load and the reference max peak energy. If there were more drivers than one per package under the same load, the margin would have been reduced. Also, if the peripheral driver couldn’t saturate because it couldn’t sink the peak transient lamp current, then the energy would also reduce the margin of safe operation.
FIGURE 22. Energy vs Time for a Peripheral Driver with an Incandescent Lamp Load

CALCULATION OF ENERGY IN AN INCANDESCENT LAMP

\[
\text{Energy} = \int \text{VOL} (I_{R1} + I_{R2}) \, dt
\]

\[
I_{R1} = \frac{V_B - \text{VOL}}{R_1}
\]

\[
I_{R2} = \frac{V_B - \text{VOL}}{R_2} \cdot e^{-\frac{t}{\tau}}
\]

\[
\tau = R_2 C_2
\]

\[
\text{Energy} = \int \text{VOL} (I_{R1} + I_{R2} e^{-\frac{t}{\tau}}) \, dt
\]

Given: \( \text{VOL} = 0.6 \text{V} \)

\( I_{R1} = 0.2 \text{ Amps} \)

\( I_{R1} + I_{R2} = 1 \text{ Amp} \)

A common technique used to reduce the 10 to 1 peak to DC transient lamp current is to bias the lamp partially ON, so the lamp filament is warm. This can be accomplished as shown in Figure 23. From Figure 20 it can be seen that the lamp resistance at 0V is 5.7\( \times \), but at 1V the resistance is 18\( \times \). At 1V the lamp doesn’t start to emit light. Using a lamp resistance of 100\( \times \) and lamp voltage of 1V, \( R_B \) was calculated to be approximately 100\( \times \). This circuit will reduce the peak lamp current from 1 amp to 316 mA.

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