INTRODUCTION

MICROWIRE is a simple three-wire serial communications interface. Built into COPS™, this standardized protocol handles serial communications between controller and peripheral devices. In this application note are some clarifications of MICROWIRE logical operation and of hardware and software considerations.

LOGICAL OPERATION

The MICROWIRE interface is essentially the serial I/O port on COPS microcontrollers, the SIO register in the shift register mode. SI is the shift register input, the serial input line to the microcontroller. SO is the shift register output, the serial output line to the peripherals. SK is the serial clock; data is clocked into or out of peripheral devices with this clock.

It is important to examine the logical diagram of the SIO and SK circuitry to fully understand the operation of this I/O port (Figure 1).

The output at SK is a function of SYNC, EN0, CARRY, and the XAS instruction. If CARRY had been set and propagated to the SKL latch by the execution of an XAS instruction, SYNC is enabled to SK and can only be overridden by EN0 (Figure 2). Trouble could arise if the user changes the state of EN0 without paying close attention to the state of the latch in the SK circuit.

If the latch is set to a logical high and the SIO register enabled as a binary counter, SK is driven high. From this state, if the SIO register is enabled as a serial shift register, SK will output the SYNC pulse immediately, without any intervening XAS instruction.

The SK clock (SYNC pulse) can be terminated by issuing an XAS instruction with CARRY = 0 (Figure 3).

[Diagrams and logic gates are shown in the document.]

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The SIO register can be compared to four master-slave flip-flops shown in Figure 4. The masters are clocked by the rising edges of the internal clock. The slaves are clocked by the falling edges of the internal clock. Upon execution of an XAS, the outputs of the masters are exchanged with the contents of the accumulator (read and overdrive) in such a way that the new data are present at the inputs of the four slaves when the falling edge of the internal clock occurs. The content of the accumulator is, therefore, latched respectively in the four slave flip-flops and bit 3 appears directly on SO.

This means that:
- a) SO will be shifted out upon the falling edges of SK and will be stable during rising edges of SK.
- b) SI will be shifted in upon the rising edge of SK, and will be stable when executing, i.e., an XAS instruction.

The shifting function is automatically performed on each of the four instruction cycles that follow an XAS instruction (Figure 5).

When the SIO register is in the shift register mode (EN0 = 0), it left shifts its contents once each instruction cycle. The data present on the SI input is shifted into the least significant bit (bit 0) of the serial shift register. SO will output the most significant bit of the SIO register (bit 3) if EN3 = 1. Otherwise, SO is held low. The SK is a logic controlled clock which issues a pulse each instruction cycle. To ensure that the serial data stream is continuous, an XAS instruction must be executed every fourth time. Serial I/O timing is related to instruction cycle timing in the following way:

**Figure 4**

**Figure 5. XAS Sequence**

TL/DD/8796–4
FIGURE 6. Serial I/O Timing

To write to device: $t_{w} > t_{\text{setup}}$
To read from device: $t_{r} < t_{SPC} - t_{SR} < t_{SPC}/4$

Where: $t_{w}$ is MICROWIRE write data-in (DI) setup time,
$t_{\text{setup}}$ is device data sheet min data setup time to latch in valid data,
$t_{SPC}$ is system clock (SK) cycle time (Recommended 50% duty cycle),
$t_{r}$ is rise time (10% to 70% bout) of system clock (SK),
$t_{SR}$ is device actual delay time before data-out (DO) valid and
$t_{m}$ is minimum data setup time for controller to shift-in valid data.

FIGURE 7. MICROWIRE Serial Data Exchange Timing
The first clock rising edge of the instruction cycle triggers
the low-to-high transition of SYNC output via SK. At this
time, the processor reads the state of SI into SIO bit 0,
shifting the current bits 0–2 left. Halfway through the cycle
(shown in Figure 6 as the eight clock rising edge), SK is
reset low and the new SIO bit 3 is outputted via SO.

INTERFACING CONSIDERATIONS
To ensure data exchange, two aspects of interfacing have
to be considered: 1) serial data exchange timing; 2) fan-out/
fan-in requirements. Theoretically, infinite devices can ac-
cept the same interface and be uniquely enabled sequen-
tially in time. In practice, however, the actual number of de-
vices that can access the same serial interface depends on
the following: system data transfer rate, system supply re-
quirement capacitive loading on SK and SO outputs, the
fan-in requirements of the logic families or discrete devices
to be interfaced.

HARDWARE INTERFACE
Provided an output can switch between a HIGH level and a
LOW level, it must do so in a predetermined amount of time
for the data transfer to occur. Since the transfer is strictly
synchronous, the timing is related to the system clock (SK)
(Figure 7). For example, if a COPS controller outputs a value
at the falling edge of the clock and is latched in by the
peripheral device at the rising edge, then the following rela-
tionship has to be satisfied:

\[
t_{\text{DELAY}} + t_{\text{SETUP}} \leq t_{\text{CK}}
\]

where \( t_{\text{CK}} \) is the time from data output starts to switch to
data being latched into the peripheral chip, \( t_{\text{SETUP}} \) is the
setup time for the peripheral device where the data has to be
at a valid level, and \( t_{\text{DELAY}} \) is the time for the output to
read the valid level. \( t_{\text{CK}} \) is related to the system clock pro-
vided by the SK pin of the COPS controller and can be
increased by increasing the COPS instruction cycle time.
The maximum \( t_{\text{SETUP}} \) is specified in the peripheral chip data
sheets. The maximum \( t_{\text{DELAY}} \) allowed may then be deriv-
e from the above relationship.

Most of the delay time before the output becomes valid
comes from charging the capacitive load connected to the
output. Each integrated circuit pin has a maximum load of
7 pF. Other sources come from connecting wires and con-
nection from PC boards. The total capacitive load may then
be estimated. The propagation delay values given in data
sheets assume particular capacitive loads (e.g. \( V_{\text{OC}} = 5V, \)
\( V_{\text{OH}} = 0.4V \), loading = 50 pF, etc.).

If the calculated load is less than the given load, those val-
ues should be used. Otherwise, a conservative estimate is
to assume that the delay time is proportional to the capaci-
tive load.

If the capacitive load is too large to satisfy the delay time
criterion, then three choices are available. An external buff-
er may be used to drive the large load. The COPS instruc-
tion cycle may be slowed down. An external pullup resistor
may be added to speed up the LOW level to HIGH level
transition. The resistor will also increase the output LOW
level and increase the HIGH level to LOW level transition
time, but the increased time is negligible as long as the
output LOW level changes by less than 0.3V. For a 100 pF
load, the standard COPS controller may use a 4.7k external
resistor, with the output LOW level increased by less than
0.2V. For the same load, the low power COPS controller
may use a 22k resistor, with the SO and SK LOW levels
increased by less than 0.1V.

Besides the timing requirements, system supply and fan-
out/fan-in requirements also have to be considered when
interfacing with MICROWIRE. For the following discussion,
we assume single supply push-pull outputs for system clock
(SK) and serial output (SO), high-impedance input for serial
input (SI).

To drive multi-devices on the same MICROWIRE, the output
drivers of the controller need to source and sink the total
maximum leakage current of all the inputs connected to it
and keep the signal level within the valid logic “1” or logic
“0”. However, in general, different logic families have differ-
ent valid “1” and “0” input voltage levels. Thus, if devices
different types are connected to the same serial inter-
face, the output driver of the controller must satisfy all the
input requirements of each device. Similarly, devices with
TRI-STATE® outputs, when connected to the SI input, must
satisfy the minimum valid input level of the controller and
the maximum TRI-STATE leakage current of all outputs.

So, for devices that have incompatible input levels or
source/sink requirements, external pull-up resistors or buff-
ers are necessary to provide level-shifting or driving.

SOFTWARE INTERFACE
The existing MICROWIRE protocol is very flexible, basically
divided into two groups:

1) 1AAAAAAAAA....ADDDED.....D

where leading 1 is the start bit and leading zeroes are
ignored.

AAA.....A is device variable instruction/address word.

DDD.....D is variable data stream between controller and
device.

2) No start bit, just bit stream, i.e., ...bbb...b

where b is a variable bit stream. Thus, device has to decode
various fields within the bit stream by counting exact bit po-
sition.

SERIAL I/O ROUTINES
Routines for handling serial I/O are provided below. The
routines are written for 16-bit transmissions, but are trivially
expandable up to 64-bit transmissions by merely changing
the initial LBI instruction. The routines arbitrarily select regis-
ter 0 as the I/O register. It is assumed that the external
device requires a logic low chip select. It is further assumed
that chip select is high and SK and SO are low on entry to
the routines. The routines exit with chip select high, SK and
SO low. GO is arbitrarily chosen as the chip select for the
external device.

SERIAL DATA OUTPUT
This routine outputs the data under the conditions specified
above. The transmitted data is preserved in the microcon-
troller.

```
OUT2:  LBI 0,12 ; point to start of data word
SC
OGI 14 ; select the external device
```
<table>
<thead>
<tr>
<th>Features</th>
<th>DS8908</th>
<th>MM545X</th>
<th>COP472-3</th>
<th>COP430 (ADC83X)</th>
<th>NM93C06A</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>GENERAL</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chip Function</td>
<td>AM/PM PLL</td>
<td>LED Display Driver</td>
<td>LCD Display Driver</td>
<td>A/D</td>
<td>EEPROM</td>
</tr>
<tr>
<td>Process</td>
<td>ECL</td>
<td>NMOS</td>
<td>CMOS</td>
<td>CMOS</td>
<td>NMOS</td>
</tr>
<tr>
<td>( V_{CC} ) Range</td>
<td>4.75V–5.25V</td>
<td>4.5V–11V</td>
<td>3.0V–5.5V</td>
<td>4.5V–0.3V</td>
<td>4.5V–5.5V</td>
</tr>
<tr>
<td>Pinout</td>
<td>20</td>
<td>40</td>
<td>20</td>
<td>8/14/20</td>
<td>14</td>
</tr>
<tr>
<td><strong>HARDWARE INTERFACE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Min ( V_{IH}/Max V_{IL} )</td>
<td>2.1V/0.7V</td>
<td>2.2V/0.8V</td>
<td>0.7V_{CC}/0.8V</td>
<td>2.0V/0.8V</td>
<td>2.0V/0.8V</td>
</tr>
<tr>
<td>SK Clock Range</td>
<td>0–625 kHz</td>
<td>0–500 kHz</td>
<td>4–250 kHz</td>
<td>10–200 kHz</td>
<td>0–250 kHz</td>
</tr>
<tr>
<td>Write Setup Min Data Di</td>
<td>0.3 ( \mu )s</td>
<td>0.3 ( \mu )s</td>
<td>1 ( \mu )s</td>
<td>0.2 ( \mu )s</td>
<td>0.4 ( \mu )s</td>
</tr>
<tr>
<td>Read Data Prop Delay</td>
<td>(Note 4)</td>
<td>(Note 3)</td>
<td>(Note 3)</td>
<td>(Note 3)</td>
<td>(Note 3)</td>
</tr>
<tr>
<td>Chip Enable</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Setup Hold Min</td>
<td>0.8 ( \mu )s</td>
<td>(3)</td>
<td>100 ns</td>
<td>0.2 ( \mu )s</td>
<td>0.4 ( \mu )s</td>
</tr>
<tr>
<td>Max Frequency Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AM</td>
<td>8 MHz</td>
<td>(Note 3)</td>
<td>(Note 3)</td>
<td>(Note 3)</td>
<td>(Note 3)</td>
</tr>
<tr>
<td>FM</td>
<td>120 MHz</td>
<td>(Note 3)</td>
<td>(Note 3)</td>
<td>(Note 3)</td>
<td>(Note 3)</td>
</tr>
<tr>
<td><strong>SOFT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial I/O Protocol</td>
<td>1(D1)...D20</td>
<td>1(D1)...D35</td>
<td>b1...b40</td>
<td>1xx</td>
<td>1AA...DD</td>
</tr>
<tr>
<td>Instruction/Address Word</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>(Note 4)</td>
</tr>
</tbody>
</table>

**Note 1:** Reference to SK rising edge.

**Note 2:** Reference to SK falling edge.

**Note 3:** Not defined.

**Note 4:** See data sheet for different modes of operation.
LEI 8 ; enable shift register mode
JP SEND2
SEND1: XAS
SEND2: LD ; data output loop
XIS
JP SEND1
XAS ; send last data
RC
CLRA
NOP
XAS ; turn SK clock off
OGI 15 ; deselect the device
LEI 0 ; turn SO low
RET

The code for reading serial data is almost the same as the serial output code. This should be expected because of the nature of the SIO register and the XAS instruction.

MICROWIRE STANDARD FAMILY
A whole family of off-the-shelf devices exists that is directly compatible with MICROWIRE serial data exchange standard. This allows direct interface with the COPS family of microcontrollers.

Table I provides a summary of the existing devices and their functions and specifications.

TYPICAL APPLICATION
Fig. 8 shows pin connection involved in interfacing an EPROM with the COP420 microcontroller.

FIGURE 8. NM93C06A COP420 Interface
The following points have to be considered:
1. For NM93C06A the SK clock frequency should be in the 0 kHz–250 kHz range. This is easily achieved with COP420 running at 4 μs–10 μs instruction cycle time (SK period is the COP420 instruction cycle time). Since the minimum SK clock high time is greater than 1 μs, the duty cycle is not a critical factor as long as the frequency does not exceed the 250 kHz max.
2. CS low period following an E/W instruction must not exceed 30 ms maximum. It should be set at typical or minimum spec of 10 ms. This is easily done in software using the SKT timer on COP420.

FIGURE 9. NM93C06A Timing
3. As shown in WRITE timing diagram, the start bit on DI must be set by a "0" to "1" transition following a CS enable ("0" to "1") when executing any instruction. One CS enable transition can only execute one instruction.
4. In the read mode, following an instruction and data train, the DI can be a "don't care," while the data is being outputted, i.e., for the next 17 bits or clocks. The same is true for other instructions after the instruction and data has been fed in.
5. The data-out train starts with a dummy bit 0 and is terminated by chip deselect. Any extra SK cycle after 16 bits is not critical. If CS is held on after all 16 of the data bits have been outputted, the DO will output the state of DI until another CS LO to HI transition starts a new instruction cycle.
6. After a read cycle, the CS must be brought low for one SK clock cycle before another instruction cycle starts.

INSTRUCTION SET

<table>
<thead>
<tr>
<th>Commands</th>
<th>Opcode</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ</td>
<td>100003A2A1A0</td>
<td>Read Register 0–15</td>
</tr>
<tr>
<td>WRITE</td>
<td>110003A2A1A0</td>
<td>Write Register 0–15</td>
</tr>
<tr>
<td>ERASE</td>
<td>101003A2A1A0</td>
<td>Erase Register 0–15</td>
</tr>
<tr>
<td>EWEN</td>
<td>1110000 0 0 1</td>
<td>Write/Erase Enable</td>
</tr>
<tr>
<td>ENDS</td>
<td>111000 0 1 0</td>
<td>Write/Erase Disable</td>
</tr>
<tr>
<td>***WRAL</td>
<td>111000 1 0 0</td>
<td>Write All Registers</td>
</tr>
<tr>
<td>ERAL</td>
<td>111000 1 0 1</td>
<td>Erase All Registers</td>
</tr>
</tbody>
</table>

All commands, data in, and data out are shifted in/out on rising edge of SK clock.
Write/erase is then done by pulsing CS low for 10 ms.
All instructions are initiated by a LO-HI transition on CS followed by a LO-HI transition on DI.
READ—After read command is shifted in DI becomes don't care and data can be read out on data out, starting with dummy bit zero.
WRITE—Write command shifted in followed by data in (16 bits) then CS pulsed low for 10 ms minimum.
ERASE
ERASE ALL—Command shifted in followed by CS low.
WRITE ALL—Pulsing CS low for 10 ms.
WRITE
ENABLE/DISABLE—Command shifted in.

***This instruction is not speced on Data sheet.*
*tE/W measured to rising edge of Sk or Cs, whichever occurs last.
t_E/W measured to rising edge of Si or CS, whichever occurs last.
I/O ROUTINE TO EVALUATE COP494

1 .TITLE E494, "I/O ROUTINE TO EVALUATE COP494"
2 01A4 .CHIP 420
3 0000 .PAGE 0

4 ;THIS IS I/O ROUTINE TO EVALUATE COP494
5 ;
6 ;
7 ;
8 ;RAM VARIABLES DECLARATIONS:
9 000E COMMAND = 0, 14 ;494 8BITS INST/ADDR WORD
10 001C RWDATA = 1, 12 ;494 16BITS R/W DATA BUFFER
11
12 ;RAM VARIABLES DECLARATIONS:
13 0000 00 PON: CLRA ;POWER-ON INIT
14 0001 32 RC ;RESET SK CLOCK
15 0002 4F XAS
16 0003 3F CLRAM: LBI 3, 0 ;CLEAR RAM FROM 7, 0 TO 0, 15
17 0004 00 CLR: CLRA ;
18 0005 04 XIS ;
19 0006 C4 JP CLR ;CONTI CLEAR REG
20 0007 12 XABR ;(A) TO BR
21 0008 5F AISC 15 ;REG 0 CLEARED?
22 0009 600F DONE: JMP C494DR ;Y, DONE CLEAR RAM, CALL 494 D
23 000A 12 XABR ;N, DEC BR
24 000C 04 JP CLR ;CONTI CLEAR REG TILL DONE
25 000D 44 NOP
26 000E 44 NOP
27
28 ;*** START 494 DRIVER SAMPLE CALLING SEQUENCE ***
29
30 C494DR: ;INIT CALLING SEQUENCE
31 00F 3350 OGI 0 ;GO TO DESELECT 494
32 011 3368 LEI 8 ;ENABLE SIO AS S.R.
33
34 013 0D LBI COMMAND ;PRELOAD 494 ERASE REG A3–A0
35 014 7C STII 0C ;PRELOAD 494 ERASE INST
36 015 70 STII 0 ;SELECT REG A3–A0
37 016 690E JSR WI4P4 ;SEND IT
38
39 018 0D LBI COMMAND ;LOAD 494 WHEN REG A3–A0
40 019 73 STII 3 ;PRELOAD 494 WREN INST
41 01A 70 STII 0 ;SELECT REG A3–A0
42 01B 690E JSR WI494 ;SEND IT
43
44 01D 0D LBI COMMAND ;PRELOAD WR REG A3–A0
45 01E 74 STII 4 ;PRELOAD 494 WRITE INST
46 01F 70 STII 0 ;SELECT REG A3–A0
47 020 18 LBI RWDATA ;PRELOAD 494 SAMPLE WRITE DATA
48 021 75 STII 5
49 022 7A STII ON
50 023 75 STII 5
I/O ROUTINE TO EVALUATE COP494

(Continued)

51 024 7A STII 0A
52 025 6900 JSR WD494 ;SEND THEM TO 494
53
54 027 0D LBI COMMAND ;PRELOAD READ REG A3–A0
55 028 78 STII 8 ;PRELOAD 494 READ INST
56 029 70 STII 0 ;SELECT REG A3–A0
57 02A 6908 JSR RD494 ;READ 494 DATA BACK VIA SI
58 02C 44 NOP
59 02D 44 NOP
60
61 0080 .PAGE 2 ;SUBROUTINE PAGE
62 080 32 SETUP: RC ;RESET SK BEFORE SELECT 494
63 081 4F XAS
64 082 3351 OGI 1 ;G0=1 TO SELECT 494
65 084 00 CLR A ;ENSURE SO=1 BEFORE GEN START B
66 085 22 SC ;
67 086 4F XAS ;TURN ON SK CLOCK
68 087 00 CLR A ;GENERATE 494 START BIT
69 088 61 AIS 1 ;
70 089 22 SC ;
71 08A 4F XAS ;SEND IT AS MSB VIA SO
72 08B 0D LBI COMMAND ;FETCH 1ST INST/ADDR WORD
73 08C 05 LD
74 08D 44 NOP ;
75 08E 4F XAS ;SEND IT (MSB OF INST FIRST)
76 08F 0E LBI COMMAND+1 ;FETCH 2ND INST/ADDR NIBBLE
77 090 05 LD
78 091 44 NOP
79 092 4F XAS ;SEND IT
80 093 1B LBI RWDATA ;POINT TO READ/WRITE DATA BUFFER
81 094 48 RET ;RET OF SETUP
82
83 095 00 TWEDLY: CLR A ;VPP WIDTH, TWE>20MS @ 4Us/INST
84 096 5B TWECNT: AIS 11 ;5 SKT LOOPS?
85 097 99 JP . + 2 ;N,CONTI
86 098 48 TWEDONE: RET ;Y,DONE
87 099 41 SKT ;
88 09A 99 JP . -1 ;
89 09B 96 JP TWECONT ;CONTI TWE TIME
90
91 09C 48 RET; RET ;2 CYCLES DELAY
92
93 0100 .PAGE 4 ;
94
95 ;*** START 494 I/O DRIVER SUBROUTINE ***
96
97 100 80 WD494: JSRP SETUP ;ENTRY TO WRITE 494 REG A3–A0
98 101 05 RWLOOF: LD ;R/W 494 16 DATA BITS
99 102 4F XAS ;
100 103 04 XIS ;
SOFTWARE DEBUG OF SERIAL REGISTER FUNCTIONS

In order to understand the method of software debug when dealing with the SIO register, one must first become familiar with the method in which the COPS MOLE™ (Development System) BREAKPOINT and TRACE operations are carried out. Once these operations are explained, the difficulties which could arise when interrogating the status of the SIO register should become apparent.

SERIAL OUT DURING BREAKPOINT

When the MOLE BREAKPOINTS, the COPS user program execution is stopped and execution of a monitor-type program, within the COP device, is started. At no time does the COP part “idle.” The monitor program loads the development system with the information contained in the COP registers.

Note also that single-step is simply a BREAKPOINT on every instruction.

If the COP chip is BREAKPOINTed while a serial function is in progress, the contents of the SIO register will be destroyed.

By the time the monitor program dumps the SIO register to the MOLE, the contents of the SIO register will have been written over by clocking in SI. To inspect the SIO register using BREAKPOINT, an XAS must be executed prior to BREAKPOINT; therefore, the SIO register will be saved in the accumulator.

An even more severe consequence is that the monitor program executes an XAS instruction to get the contents of the SIO register to the MOLE. Therefore, the SK latch is dependent on the state of the CARRY prior to the BREAKPOINT. In order to guarantee the integrity of the SIO register, one must carefully choose the position of the BREAKPOINT address.

As can be seen, it is impossible to single-step or BREAKPOINT through a serial operation in the SIO register.

SERIAL OUT DURING TRACE

In the TRACE mode, the user’s program execution is never stopped. This mode is a real-time description of the program counter and the external event lines; therefore, the four external event lines can be used as logic analyzers to monitor the state of any input or output on the COPS device. The external event lines must be tied to the I/O which is to be monitored.

The state of these I/O (external event lines) is displayed along with the TRACE information. The safest way to monitor the real-time state of SO is to use the TRACE function in conjunction with the external event lines.

CONCLUSIONS

National’s super-sensible MICROWIRE serial data exchange standard allows interfacing to any number of specialized peripherals using an absolute minimum number of valuable I/O pins; this leaves more I/O lines available for system interfacing and may permit the COPS controller to be packaged in a smaller package.
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