1 Introduction

The LM5046 reference board is designed in the telecom industry standard one-eighth brick footprint based on the phase-shifted full-bridge topology. This board is for reference only and is intended to demonstrate the capability of the LM5046. Hardware is not provided for evaluation. Please refer to AN-2115 LM5046 Evaluation Board (SNVA470) for more information.

The performance of the reference board is as follows:

- Input operating range: 36V to 75V
- Output voltage: 12V
- Measured efficiency at 48V: 92% @ 10A
- Frequency of operation: 420kHz
- Board size: 2.28 x 0.89 x 0.4 inches
- Load Regulation: 0.2%
- Line Regulation: 0.1%
- Line UVLO (34V/32V on/off)
- Hiccup Mode Current Limit

The printed circuit board consists of 10 layers; 2 ounce copper outer layers and 3 ounce copper inner layers on FR4 material with a total thickness of 0.12 inches. The unit is designed for continuous operation at rated load at <40°C and a minimum airflow of 300 LFM at full load.

2 Theory of Operation

The Phase-Shifted Full-Bridge (PSFB) topology is a derivative of the classic full-bridge topology. When tuned appropriately the PSFB topology achieves zero voltage switching (ZVS) of the primary FETs while maintaining constant switching frequency. The ZVS feature is highly desirable as it reduces both the switching losses and EMI emissions. Figure 1 illustrates the circuit arrangement for the PSFB topology. The power transfer mode of the PSFB topology is similar to the hard switching full-bridge i.e., when the FETs in the diagonal of the bridge are turned-on (Q1 & Q3 or Q2 & Q4), a power transfer cycle is initiated. At the end of the power transfer cycle, PWM turns off the switch Q3 or Q4 depending on the phase with a pulse width determined by the input and output voltages and the transformer turns ratio. In the freewheel mode, unlike the classic full-bridge where all the four primary FETs are off, in the PSFB topology the primary of the power transformer is shorted by activating either both the top FETs (Q1 and Q4) or both the bottom FETs (Q2 and Q3) alternatively. In a PSFB topology, the primary switches are turned on alternatively energizing the windings in such a way that the flux swings back and forth in the first and the third quadrants of the B-H curve. The use of two quadrants allows better utilization of the core resulting in a smaller core volume compared to the single-ended topologies.
The secondary side employs synchronous rectification scheme, which is controlled by the LM5046. In addition to the basic soft-start already described, the LM5046 contains a second soft-start function that gradually turns on the synchronous rectifiers to their steady-state duty cycle. This function keeps the synchronous rectifiers off until the error amplifier on the secondary side soft-starts, allowing a linear start-up of the output voltage even into pre-biased loads. Then the SR output duty cycle is gradually increased to prevent output voltage disturbances due to the difference in the voltage drop between the body diode and the channel resistance of the synchronous MOSFETs. Feedback from the output is processed by an amplifier and reference, generating an error voltage, which is coupled back to the primary side control through an opto-coupler. The LM5046 evaluation board employs peak current mode control and a standard “type II” network is used for the compensator.
3 Performance Characteristics

Once the circuit is powered up and running normally, the output voltage is regulated to 12V with the accuracy determined by the feedback resistors and the voltage reference. The frequency of operation is selected to be 420 kHz, which is a good compromise between board size and efficiency. Please refer to the Figure 3 for efficiency curves.

Figure 3. Reference Board Efficiency

Figure 4 shows the output voltage during a typical start-up with a 48V input and a load of 12A. There is no overshoot during start-up.

Figure 4. Soft-Start

Figure 5 shows typical transient response on the reference board when the load current is switched from 5A to 10A and back to 5A. There is minimal output voltage droop and overshoot during the sudden change in output current shown by the lower trace.
Performance Characteristics

Figure 5. Transient Response

Figure 6 shows typical output ripple seen directly across the output capacitor, for an input voltage of 48V and a load of 12A. This waveform is typical of most loads and input voltages.

Figure 6. Output Ripple

Figure 7 and Figure 8 show the typical SW node voltage waveforms with a 25A load. Figure 7 shows an input voltage represents an input voltage of 48V and Figure 8 represents an input voltage of 75V.

Figure 7. 48V Switch Node Waveforms

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Conditions: Input Voltage=75V
Output Current=10A
Trace 1: SW1 Node Q2 Drain Voltage Volts/div=20V
Trace 2: SW2 Node Q3 Drain Voltage Volts/div=20V
Horizontal Resolution=1 µs/div

Figure 8. 75V Switch Node Waveforms

Figure 9 shows a typical startup of the LM5045 into a 6V pre-biased load.

Conditions: Input Voltage=48V, Output Pre-Bias=6V
Trace 1 (Channel 1): Output Voltage Volts/div=5V
Trace 2 (Channel 2): SR gate Voltage Volts/Div=5V
Trace 3 (Channel 3): Output Current Amps/div=200mA
Horizontal Resolution=2.0 ms/div

Figure 9. Soft-Start into a 6V Pre-Biased Output

Figure 10 shows the output current de-rating on the reference board at 48V input.

Figure 10. Load Current vs. Air Flow
Figure 11. LM5046 Based Eight Brick Reference Board Schematic
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<th>Designator</th>
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5 PCB Layouts

Figure 12. Top Layer Assembly

Figure 13. Bottom Layer Assembly

Figure 14. Top Layer (Layer 1)

Figure 15. Layer 2
Figure 20. Layer 7

Figure 21. Layer 8

Figure 22. Layer 9

Figure 23. Bottom Layer (Layer 10)
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