LM25088, LM5088

*Improve Power Converter Reliability Using Hiccup-Mode Current Limiting*

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Improve Power Converter Reliability Using Hiccup-Mode Current Limiting

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Introduction

Switch-mode power supplies employ various schemes to protect themselves, and ideally the load, in overload conditions. Depending on whether the power converter automatically recovers and reverts back to normal operation once the overload condition is removed, overload protection schemes can be broadly classified into two categories: non-recoverable protection schemes (fuses, circuit breakers, overload shutdowns) and self-recoverable protection schemes (cycle-by-cycle current limiting and hiccup mode).

The choice of protection scheme depends on the cost, complexity, and applicable safety standards. Non-recoverable schemes, such as the use of fuses, are popular in front-end off-line power conversion, and self-recoverable protection schemes are used typically in back-end DC-DC converters. Often times, both of these types of schemes are implemented together to provide additional redundancy. Non-recoverable schemes are outside the purview of this article. Among self-recoverable protection schemes, cycle-by-cycle current limiting delivers maximum load current into the short circuit, thereby creating a thermal management problem. This complicates component and heat sink selection and if the components are not oversized, it can reduce the reliability of the system. Hiccup-mode protection solves the thermal management dilemma, and therefore improves system reliability and simplifies component selection.

Overview of Self-Recoverable Overload Protection Schemes

Cycle-by-cycle current limiting can be implemented by using peak, valley, or average inductor current information to detect the overload condition and limit the duty cycle. Peak current and valley cycle-by-cycle limiting are relatively simple schemes to implement. For example in a buck converter, a peak current limiting scheme is implemented by sensing the top switch current and, a valley current limiting scheme is implemented by sensing the bottom diode current (or bottom switch in a synchronous case). In peak current limiting, the PWM cycle is terminated (the top switch is turned-off) if the sensed current is greater than a predetermined threshold. In the case of
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valley current limiting, a PWM cycle is initiated if the sensed current is lower than the threshold. At the inception of current limit (soft-short), both of these schemes tend to have a soft-knee i.e. the output voltage drops slowly with increasing current. Figure 1 shows typical inductor current waveforms in peak and valley current limiting schemes and Figure 2 shows the $V_{OUT}$ versus $I_{OUT}$ versus curves for self-recoverable protection schemes, where soft-knee for peak and valley cycle-by-cycle current limiting is illustrated.

Average current limiting converts the power converter from a constant voltage source into a constant current source. In this scheme the response is the same whether it is a soft-short or a hard-short, and thus, it is popularly known as “brick-wall limiting”. Average current limiting is typically implemented with a two-loop feedback system. A voltage amplifier is used to regulate the output voltage and a second current amplifier is used to regulate the average inductor current. Because of its two-loop system, average current limiting is slow to respond in hard-short current conditions. For this reason, it is implemented together with peak/valley cycle-by-cycle current limiting for fast response. This scheme is therefore fairly complex and is often employed in bridge topologies to ensure transformer volt-second balance in overload conditions.

The primary drawback of all three protection schemes is that during overload conditions, the average output current remains at a high level. The power converter, set by the reference to the current limit circuit, is delivering high load current into the load. This results in high power dissipation in the power train components, and all of the energy dumped into the load is not desirable. For example, in a buck converter employing a cycle-by-cycle current limiting mode and since the duty cycle is limited, the top switch is ON for a short period of time and the majority of the load is carried by the buck diode. This increases the power dissipation in the diode compared to normal running conditions.

Foldback current limiting reduces power dissipation during overload conditions. In this scheme, as the output voltage falls during an overload condition, the current limit threshold is also reduced. Thus, it reduces the load current during fault conditions. This reduces power dissipation and eases thermal stresses on the power train components and the load. The main disadvantage of this scheme is that it is not completely self-recoverable. Once the fault is removed, the power converter can potentially enter a latch-up mode while powering constant-current loads.

Figure 1. Inductor Current in Normal and Overload Conditions for Peak and Valley Cycle-by-Cycle Current Limiting Schemes

Figure 2. $V_{OUT}$ vs. $I_{OUT}$ Curves for Various Cycle-by-Cycle Current-Limiting Schemes
Hiccup-Mode Current Limiting

A hiccup-mode current-limiting scheme can overcome all of the previously-mentioned disadvantages, i.e., it can solve the thermal dissipation problem during an overload condition and provide smooth self-recovery once the overload condition is removed. It is a simple scheme to implement and requires few external components when the logic is integrated into the PWM IC. Typically in a hiccup scheme once an overload condition is detected, the power converter is turned off and is forced into sleep mode. At the end of sleep time, a restart attempt is made by soft-starting the converter. If the overload condition persists, this process is repeated. Thus, the converter is in a loop of short bursts of pulses followed by a sleep time in a continuous overload condition, hence the name 'hiccup'. The sleep time reduces the average load current and allows the power converter to cool down.

Two approaches are used typically to enter into sleep mode: by setting the hiccup threshold higher than the cycle-by-cycle current-limit threshold, hiccup is invoked only in hard-short conditions; and by using a counter which triggers hiccup only after counting a number of cycle-by-cycle current-limit events. Although simple to implement, the first approach is risky since hiccup can be invoked in transient load conditions and often requires additional logic to avoid false triggers. The second approach is virtually risk free and flexible in comparison.

Figure 3 illustrates implementation of delayed hiccup-mode current limiting in a LM5088-2 buck controller.

As shown in Figure 3, once an overload condition is detected, the present cycle is terminated and a current source is turned on to charge a capacitor. If the fault persists, the capacitor is charged every cycle; otherwise, the capacitor is discharged. If the voltage across the capacitor is above the predetermined threshold (start sleep-time REF), the SS capacitor is discharged. Thus, the power converter enters into a sleep mode. The hiccup capacitor is then discharged to another threshold (end sleep-time REF) which determines the sleep time. At the end of the sleep time, the soft-start capacitor is released and the soft-start begins. If the over-
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load persists, this cycle is repeated. The number of current-limit cycles required to establish the hiccup mode and sleep time are programmable by the choice of capacitor value. This flexibility allows the system designer to fine-tune the hiccup mode. Shorting the capacitor will result in continuous cycle-by-cycle current limiting.

Figure 4 shows the timing diagram for the delayed hiccup-mode current-limiting scheme. In Figure 4, time period T1 is the delay time during which the persistence of an overload condition is checked by charging the hiccup capacitor to a predetermined value. Once it is established that the overload condition is persistent, the converter is forced into a sleep mode during the time period T2. With the delay time (T1) established, it prevents the converter from entering into sleep mode for load transient conditions. At the end of time period T2, a soft-start cycle is initiated.

Hiccup-mode current limiting, therefore, reduces the average load current during an overload condition. This in turn reduces the power dissipation in the power train and reduces the thermal stress on the components.

Thermal Comparison between Cycle-by-Cycle and Hiccup-Mode Current Limiting

For illustration purposes, let’s consider the LM5088-2, a non-synchronous buck controller with a hiccup-mode overload circuit. The hiccup-mode scheme is as shown in Figures 3 and 4. The LM5088-2 controller requires just one external capacitor to configure the hiccup-mode feature, and if the hiccup pin is grounded, the part operates in a continuous cycle-by-cycle current-limiting mode only.

Let’s further consider the LM5088-2 controller’s evaluation board with the following specifications:

- Frequency = 250 kHz
- Forward drop of buck diode = 0.5V
- Average load current during cycle-by-cycle limiting (I₀) = 10A
- ON time of the top switch in current limit (Tₒ) = 100 ns.
- D = 0.025 and (1-D) = 0.975
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Continuous Cycle-by-Cycle Current Limiting

Conduction loss of the buck diode in continuous current limiting is:

\[ P_{dc\_\_diode} = (1 - D) \times I_o \times V_F = 4.8\,W \]

The typical junction to ambient resistance of a D²Pak Schottky rectifier is about 18 °C/W (with heatsink).

Therefore, the predicted junction temperature at an ambient temperature of 60 °C is:

\[ 60\,^\circ C + 4.8\,W \times 18\,^\circ C/W = 146.4\,^\circ C \]

Hiccup-Mode Current Limiting

For calculation purposes, let's assume 100 cycle-by-cycle current limits before a sleep time of 500 µs is initiated, resulting in a diode duty cycle of 0.076.

Conduction loss of the buck diode in continuous current limiting is:

\[ P_{dc\_\_diode} = (1 - D) \times I_o \times V_F = 0.38\,W \]

Therefore, the predicted junction temperature at an ambient temperature of 29 °C is:

\[ 25\,^\circ C + 0.38\,W \times 18\,^\circ C/W = 32\,^\circ C \]

It should be noted also that the temperature of the PC board is also lowered due to the sleep time.

Figure 5a shows the thermal image of the LM5088 board in peak cycle-by-cycle current limiting and Figure 5b shows the thermal image of the LM5088 board in hiccup-mode current limiting. It can be inferred from the calculations and thermal images that the cycle-by-cycle case is unsustainable since the junction temperature can exceed the rated temperature for the diode. And in prolonged overload conditions, this can reduce the reliability of the power converter. The hiccup-mode scheme, however, keeps the power converter cool and also does not require the components to be derated for elevated temperature. Therefore, hiccup-mode current limiting not only simplifies component selection but also enhances the reliability of the power converter.

Figure 5. Thermal Image of the LM5088 Evaluation Board
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