LMZ35003 Parallel Operation

ABSTRACT

The LMZ35003 is a 7-V to 50-V input, 2.5-A output, integrated power module which integrates a DC/DC converter, shielded inductor and passives in a low-profile, QFN package. For applications requiring greater than 2.5 A, it is possible to parallel multiple LMZ35003 devices by following the recommendations in this paper.

Current Sharing

The LMZ35003 is a peak current mode control device. In peak current mode control, the output voltage is scaled down through a resistor divider and fed into the error amplifier where it is compared to a fixed voltage reference. The output of the error amplifier is proportional to the device’s output current. The output current information is available on pin 2 of the LMZ35003. In a stand-alone application pin 2 is a DNC pin (Do Not Connect), but when paralleling multiple LMZ35003 devices, this pin becomes ISHARE. Connecting the ISHARE pins of multiple LMZ35003 devices together allows current sharing. Other connections must also be made between the devices.

Parallel Operation Connections

When paralleling LMZ35003 devices, several connections must be made between the devices. Figure 1 shows a typical schematic for paralleling two LMZ35003 devices.

Figure 1. Typical LMZ35003 Parallel Schematic
Parallel Connections

- Connect the VOUT pins of all devices together to operate as a single output.
- The VADJ pin of all devices must be connected together to ensure all devices see the same feedback voltage. The output voltage is set by connecting a single $R_{SET}$ resistor between the VADJ connection and VOUT; the other device’s VADJ pins must be left open. To select the $R_{SET}$ value, reference Table 3 of the LMZ35003 (SNVS988) datasheet for a given VOUT and divide $R_{SET}$ by the number of modules being paralleled.
- For proper current sharing, the ISHARE pin (pin 2) voltage of all devices must be equal. Connect the ISHARE pins together directly.
- Connecting the SS/TR pins together ensures that all devices start-up together by sharing the same slow start ramp voltage. The STSEL pins of all devices must be connected to AGND. To change the SS rise time, additional capacitance must be added to the SS/TR connection. The slow start capacitance can be found in Table 6 of the LMZ35003 datasheet and must be multiplied by the number of devices being paralleled.
- The switching frequency of the paralleled devices must be the same to ensure proper current sharing and operation. It is required to drive the RT/CLK pin of all devices with an external clock to ensure they switch at the same frequency. The clock signal must be present before the devices are turned on.
- The INH/UVLO pins of the devices must be tied together. To enable and disable the output voltage, the INH/UVLO pins for all paralleled devices must be controlled at the same time. It is recommended to monitor the input voltage using a voltage supervisor and use the supervisor’s output to drive the combined INH/UVLO pins to insure simultaneous power-up and power down of all devices.

LMZ35003 Parallel Operating Conditions

When paralleling multiple LMZ35003 devices, the input voltage range and output voltage range is the same as for a single device, as specified in the datasheet. The amount of required output capacitance for a single device is 100 µF of ceramic capacitance. When operated in parallel, this amount must be multiplied by the number of devices being paralleled. Paralleled devices must be synchronized to the same frequency. The allowable synchronization frequencies are a function of Vin and Vout and can be found in Figure 27 of the datasheet. Regarding output current, the combined output current must be derated as described in Current Sharing Accuracy.

LMZ35003 Parallel Results

The results and waveforms presented in this report represent two devices in parallel, unless otherwise stated. The waveforms were taken at 24-V input, 5-V output, 25°C ambient temperature, and synchronized to a 500-kHz external clock. The 500-kHz clock was fed to the RT/CLK pin of all devices. Introducing a 180° phase offset can easily achieve 180° out-of-phase operation. It is possible to parallel multiple devices with similar results, as is presented here. However, close attention must be paid to board layout when paralleling multiple devices to ensure clean inter-connecting signals.

ISHARE

The current sharing information is available on pin 2 (DNC) of the LMZ35003. When paralleling multiple LMZ35003 devices, this pin must be connected between devices. In current sharing applications this pin is referred to as ISHARE.

For proper current sharing, the voltage on the ISHARE pin of all devices must be equal. Connect the ISHARE pins of all devices together. The ISHARE connection must be routed in a way to keep this signal as clean as possible. An optional capacitor (≤ 100 pF) can be added to the ISHARE pin of each device to help filter the signal.

Synchronizing to an External Clock

In order to operate the LMZ35003 devices in parallel, it is required to synchronize all devices to an external clock. The clock must be present before input power is applied, or before release of the INH control. All devices must be synchronized to the same frequency, however, the devices can be driven out of phase to reduce ripple voltage and improve transient response.
Undervoltage Lock-Out (UVLO)

The LMZ35003 has a UVLO circuit internal to the device. When paralleling multiple LMZ35003 devices, the INH/UVLO pins of all modules must be connected together and the UVLO threshold must be set externally with a resistor divider from the input voltage. The values of the resistors in the divider can be selected from Table 4 of the LMZ35003 datasheet, however, the resistor values shown in the table must be divided by the number of modules being paralleled. It is recommended to set the UVLO threshold to approximately 80% to 85% of the minimum expected input voltage.

Current Sharing Accuracy

When paralleling multiple LMZ35003 devices, the maximum output current the solution can provide must be calculated using Equation 1. Due to internal variances between devices, the amount of output current must be de-rated to ensure none of the devices operate above the maximum output current of a single device (2.5 A). Figure 3 plots the typical output current per device of two paralleled devices. The X-axis is the total output current of both devices combined.

\[
I_{O\text{UTmax}} = 0.8 \times (n \times 2.5) \text{ (A)};
\]

where \(n\) is the number of LMZ35003 devices being paralleled. (1)

![Figure 2. Typical Current Sharing Accuracy](image-url)
ON and OFF Control

It is recommended to turn-on and turn-off the paralleled devices by use of the Inhibit control. Using a voltage supervisor to monitor the input voltage and control the INH pins is recommended. The INH pins of the paralleled device should be connected together. By controlling the INH pins together, it will avoid the slightly different UVLO turn-on and UVLO turn-off thresholds of the multiple devices. Figure 3 and Figure 4 show the turn-on and turn-off of the output voltage using the INH control.

Figure 3. Start up Waveform (using INH)

Figure 4. Shut Down Waveform (using INH)
Input and Output Voltage Ripple

The input and output voltage ripple waveforms of two paralleled LMZ35003 modules is shown in Figure 5. The operating conditions for this waveform are Vin = 24 V, Vout = 5 V, Iout = 4 A, fsw = 500 kHz, and total Cout = 4 × 47-µF ceramic + 2 × 220-µF polymer tantalum.

![Figure 5. Ripple Voltage](image)

Conclusion

By making the required connections between LMZ35003 devices and synchronizing the devices to the same switching frequency, paralleled devices will operate and behave as a single stand-alone device with increased output current capability. Controlling the turn-on and turn-off through the Inhibit function while a valid input voltage is present will ensure a proper ramp up and ramp down of the output voltage. By following the guidelines included in this paper and the LMZ35003 datasheet (SNVS988), multiple power modules can be paralleled for increased current applications.
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