Inverted SEPIC made SIMPLE

Akshay Mehta, Frank De Stasi

ABSTRACT
There can be quite a few applications that require a conversion from a negative input voltage to a negative output voltage and there are a few ways to go about doing it. The telecom industry is one such example where the rails are usually negative. This design space along with being limited is not well explored. In this application note we will go over the use of an integrated boost regulator in the inverted SEPIC topology to convert a negative input voltage to a negative output voltage.

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1 Introduction
The LM2586 is part of the LM258x family of SIMPLE SWITCHER® boost regulators from Texas Instruments. The internal NPN is capable of handling a voltage of 65V and has a current limit of 4A. The maximum input voltage that the device can handle is 40V. Thus this device makes a good candidate for wide VIN solutions. The design shown here is created for a typical input of -5V and output of -12V at 1A load current, with a common ground between input and output. But it can handle an input voltage range of -5V to -24V. The following sections will talk about the operation.
The basic operation of this circuit is that of an inverted SEPIC topology. The inverted SEPIC is usually used with devices that have a high side switch (e.g., a buck switcher) because it lets a user design for an output voltage that can be higher or lower than the input voltage. The switching device in this topology needs to be able to withstand a voltage of $+V_{IN}$ and $-V_{OUT}$ with respect to ground which limits the use of most DC/DC integrated buck regulators. But since we are working with negative rails, we can use a device with a low side switch such as the LM2586 in the inverted SEPIC topology and reference the device ground to $-V_{IN}$.

When the NPN is turned on, there are two current paths. One path is from ground, through primary inductor $L_1$, the internal NPN, $-V_{IN}$ rail and the input capacitor. The second current path is from ground, the output capacitor, secondary inductor, the coupling capacitor, internal NPN, $-V_{IN}$ rail and the input capacitor. During the on time the switch node is at a voltage of $-V_{IN}$ with respect to ground and the voltage at the other end of the coupling capacitor is $-V_{IN} - V_{OUT}$ with respect to ground. Therefore the coupling capacitor is now charging up to $V_{OUT}$. When the NPN is turned off, the voltages across the two inductors are reversed and the current through them starts ramping down. During the off time the diode, D1, is forward biased. There are two current paths during the off time as well. The first path is from $-V_{OUT}$, secondary inductor $L_2$, diode $D_1$, and output capacitor. The second current path is from ground, primary inductor $L_1$, coupling capacitor, diode $D_1$ and output capacitor. The switch voltage during the off time is $+V_{OUT}$ with respect to ground and the voltage on the other side of the coupling capacitor is a diode drop above ground. Therefore the device chosen has to be able to sustain a total voltage of $V_{IN} + V_{OUT}$ across it.

The distinct advantage of this topology is that the output sees constant current like that in the buck topology. This makes the output ripple much cleaner and smaller. Figure 1 shows the steady state waveform with the secondary inductor current, switch voltage and the output voltage ripple. While Figure 2 shows the design schematic. Reference 1 talks about the actual design equations and component selection.

![Figure 1. -5V IN -12V OUT 300mA I OUT](image-url)
Figure 2. Design Schematic
In this design, the ground of the IC is referenced to the negative input voltage. A current mirror is used to set the feedback current and consequently the regulated output voltage. Use of an ordinary two transistor current mirror would cause the output to have a dependency on the $V_{BE}$ of the transistor. In order to remove that dependency a third transistor, $Q_3$, and resistor $R_{FBE2}$, are connected as shown in the design schematic. From the schematic we can see that the voltage at the upper feedback resistor will be two diode drops below ground, i.e. $-2V_{BE}$. The lower feedback resistor is chosen such that there is 1mA of current flowing through it. Therefore we get,

$$R_{FBB} = \frac{V_{REF}}{0.001}$$  \hspace{1cm} (1)

The reference voltage $V_{REF}$ for the LM2586 is 1.2V. Therefore $R_{FBB}$ is set to be 1.2kΩ. An additional resistor, $R_{FBE2}$, is connected between ground and the common base of the two transistors. This resistor helps pull more current from ground to FB and that current gets added to the current flowing through the upper feedback resistor. This current can be realized as

$$I_{RBE2} = \frac{V_{BE}}{R_{BE2}}$$  \hspace{1cm} (2)

Without this resistor, $R_{FBE2}$, the current flowing through the upper feedback resistor would be

$$I_{RFBT} = \frac{V_{OUT} - 2 \cdot V_{BE}}{R_{FBT}}$$  \hspace{1cm} (3)

With the addition of this resistor, this current is now re-written as

$$I_{RFBT} = \frac{V_{OUT} - 2 \cdot V_{BE}}{R_{FBT}} + \frac{V_{BE}}{R_{FBE2}}$$  \hspace{1cm} (4)

From Equation 4 we can observe that the value of $R_{FBE2}$ will affect the output voltage. If it is set to be exactly half of the upper feedback resistor, $R_{FBT}$, then we could get an output voltage that would not depend on the transistor's $V_{BE}$. Therefore when $R_{FBE2}$ is set to $R_{FBT}/2$, we get

$$I_{RFBT} = \frac{V_{OUT} - 2 \cdot V_{BE}}{R_{FBT}} + 2 \cdot \frac{V_{BE}}{R_{FBT}}$$  \hspace{1cm} (5)

This can be written as

$$I_{RFBT} = \frac{V_{OUT}}{R_{FBT}}$$  \hspace{1cm} (6)

We set the feedback current to be 1mA. Therefore setting $I_{RFBT}$ to 1mA, we can find the required value for $R_{FBT}$.

$$R_{RFBT} = \frac{V_{OUT}}{I_{RFBT}}$$  \hspace{1cm} (7)

The two PNP s forming the current mirror should have very close matching so as to get a well-matched current and consequently lesser variation in $V_{OUT}$. The best way to ensure that is to find a device that has two PNPs packaged together. This way the two $V_{BE}$s will change together with temperature. Another note to keep in mind is that while laying out the board, the transistors should be kept away from the high current paths.
3 Test Results

The following scope plots and efficiency data were taken on the custom PCB. Figure 3 shows the line regulation at $I_{\text{OUT}}$ of 400mA. Because of the modified current mirror, there is very little variation on the output with input voltage.

![Figure 3. Line Regulation, $I_{\text{OUT}} = 400\, \text{mA}$](image)

Figure 4 shows the efficiency of the design with respect to the load current and different $V_{\text{IN}}$s.

![Figure 4. Efficiency Vs. $I_{\text{OUT}}$, $V_{\text{OUT}} = -12V$](image)
Figure 5 shows the load regulation of the design with the input voltage set to -12V.

Because of a relatively high switch current limit of 4A, the LM2586 can allow high output currents. Figure 6 shows the max load that the device can drive vs. the input voltage it is operating at.
As mentioned before, one advantage of the inverted SEPIC is that the output sees constant current. This means that the RHP zero is eliminated in this topology. This makes the design a little easier to compensate and the resulting load transient response would be faster. Figure 7 shows the result of a 200mA to 1A load transient at the output.

![Figure 7. Load Transient \( V_{IN} = -12V, V_{OUT} = -12V, I_{OUT} = 200mA \) to 1A](image)

Figure 7 shows the startup behavior of the design. In certain systems inrush currents shown aren't tolerated. In order to reduce the inrush currents a longer softstart is desired. To add more softstart time an external circuit can be added. Please refer to application note titled Soft-start Using Constant Current Approach to learn more about this.

![Figure 8. Startup \( V_{BI} = -12V, V_{OUT} = -12V, I_{OUT} = 500mA \)](image)
### Conclusion

Thus we see that just by adding a few external components, a SIMPLE SWITCHER® boost regulator like the LM2586 could be used in an inverted SEPIC topology to obtain a negative output from a negative input. The showcased design has good line regulation and load transient response.

### References

1. Designing DC/DC converters based on ZETA topology
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