ABSTRACT

The LP8860-Q1 device is an automotive LED driver with boost converter to support infotainment display, automotive cluster, and lighting applications. In order to support a wide range of application conditions for automotive, LP8860-Q1 offers various settings for boost compensation with EEPROM registers. This document provides additional details for several device EEPROM registers, expanding on descriptions in the LP8860-Q1 data sheet.

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# Boost Compensation Registers of LP8860-Q1

## Table 1. Boost Compensation Registers

<table>
<thead>
<tr>
<th>EEPROM addr(Hex)</th>
<th>Bit</th>
<th>Name</th>
<th>Data Sheet Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>70</td>
<td>5</td>
<td>BOOST_EN_IRAMP_DELAY</td>
<td>Boost current ramp delay enable (for adjusting conversion ratio/stability, 35% of period)</td>
</tr>
<tr>
<td>71</td>
<td>6:5</td>
<td>BOOST_SEL_IND</td>
<td>Boost artificial current ramp peak value, A/s. Select value higher than ( I_{RAMP _ GAIN} = 1.2 \times 0.5 \times \frac{(V_{OUT _ max} - V_{IN _ min})}{0.7 \times L \times 60000} ), where ( V_{IN}, V_{OUT} ) are boost input and output voltage, ( L ) - inductance, H. 25-mΩ ( R_{SENSE} ) is suggested</td>
</tr>
<tr>
<td></td>
<td>4:3</td>
<td>BOOST_SEL_IRAMP</td>
<td></td>
</tr>
<tr>
<td>74</td>
<td>7:6</td>
<td>BOOST_LLCC_SEL</td>
<td>Light load comparator control. Selects boost PFM entry threshold (compensator current)</td>
</tr>
<tr>
<td>5:4</td>
<td></td>
<td>BOOST_SEL_JITTER_FILTER</td>
<td>Boost jitter filter selection</td>
</tr>
<tr>
<td>3:2</td>
<td></td>
<td>BOOST_SEL_I</td>
<td>Boost PI compensator control: integral part</td>
</tr>
<tr>
<td>1:0</td>
<td></td>
<td>BOOST_SEL_P</td>
<td>Boost PI compensator control: proportional part</td>
</tr>
<tr>
<td>75</td>
<td>7:6</td>
<td>BOOST_OFFTIME_SEL</td>
<td>Boost time off selection</td>
</tr>
<tr>
<td>5:4</td>
<td></td>
<td>BOOST_BLANKTIME_SEL</td>
<td>Boost blank time selection</td>
</tr>
</tbody>
</table>

### 1.1 EEPROM Address 0x70[5] - BOOST_EN_IRAMP_DELAY

Boost artificial current ramp (\( I_{RAMP} \)) is disabled for the first 35% of period for every switching cycle when the bit is high. This gives more margin of boost compensator current from given minimum available compensator current decided by boost design. This can be useful at low switching frequency (a few hundred kHz) where required compensator current is higher than high switching frequency; hence, low switching frequency tends to have less current margin from minimum available compensator current.

![Figure 1. Boost \( I_{RAMP} \) Delay Function](image)

**Recommended setting:** Enable this function for low switching frequency (100 kHz to 600 kHz) monitoring boost output waveform. If boost output waveform is stable and reaches target voltage at maximum load condition, this function is not needed.
1.2 **EEPROM Address 0x71[6:3] – BOOST_SEL_IND, BOOST_SEL_IRAMP**

Boost artificial current ramp ($I_{RAMP}$ shown in Figure 1) peak value, A/s. For a peak current mode boost converter without a artificial current ramp, sub-harmonic oscillation occurs with a duty cycle > 50%. By adding a current ramp greater than the down slope of the inductor current, the oscillation can be damped. Use Equation 1 to calculate required $I_{RAMP\_GAIN}$:

$$I_{RAMP\_GAIN} = 1.2 \times 0.5 - \frac{(V_{OUT\_max} - V_{IN\_min})}{(0.7 \times L \times 60000)}$$

where
- $L$ : Inductance

**Recommended setting:** Select 20% or a little higher value than calculated value from Table 2.

<table>
<thead>
<tr>
<th>BOOST_SEL_IRAMP[1:0]</th>
<th>BOOST_SEL_IND[1:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>00</td>
<td>130</td>
</tr>
<tr>
<td>01</td>
<td>88</td>
</tr>
<tr>
<td>10</td>
<td>56</td>
</tr>
<tr>
<td>11</td>
<td>37</td>
</tr>
</tbody>
</table>

1.3 **EEPROM Address 0x74[7:6] – BOOST_SEL_LLC**

BOOST_SEL_LLC is a light load comparator control — it selects boost PFM entry threshold. The load current of entering PFM is a function of the LLC setting, the slope of artificial current ramp, and inductor current ramp. Lower current value sets PWM operation threshold to lighter load.

- 00 = 5 $\mu$A (boost switches from PFM to PWM early at light loads)
- 01 = 10 $\mu$A
- 10 = 15 $\mu$A
- 11 = 20 $\mu$A (boost operates in PFM mode to higher loads)
Recommended setting:
- High LLC setting: efficiency ↑, chance of audible noise ↑ (high \(V_{\text{OUT}}\) ripple by PFM mode switching)
- Low LLC setting: efficiency ↓, chance of audible noise ↓ (low \(V_{\text{OUT}}\) ripple by PWM mode switching)
- For automotive applications, audible noise matters more than efficiency; therefore, lowest LLC is recommended.

1.4 **EEPROM Address 0x74[5:4] – BOOST_SEL_JITTER_FILTER**

EEPROM Address 0x74[5:4] is a low pass filter added on the internal FB signal to filter out noise to improve output switching jitter:
- 00 = bypass
- 01 = 300 kHz
- 10 = 60 kHz
- 11 = 30 kHz

**Recommended setting:** Use default value (may vary with EEPROM versions). Higher setting (lower frequency) can lower phase margin of AC loop.

1.5 **EEPROM address 0x74[3:2] – BOOST_SEL_I**

EEPROM address 0x74[3:2] controls the DC gain of loop control. The higher setting increases DC gain and loop bandwidth to improve transient response but lower phase and gain margin of loop:
- 00 = 1
- 01 = 2
- 10 = 3
- 11 = 4

**Recommended setting:** Use default value (01b), which is an optimal value from simulation and IC validation. Figure 3 shows a simplified diagram of phase-gain graph and may not apply for all frequency ranges.

![Figure 3. Boost Compensation – I Term](image-url)
1.6  EEPROM Address 0x74[1:0] – BOOST_SEL_P

EEPROM Address 0x74[1:0] controls the proportional term of the loop compensation. The lower setting increases loop bandwidth by moving the internal zero to the lower frequency:

- 00 = 1
- 01 = 2
- 10 = 3
- 11 = 4

Lower bandwidth by high P setting will also cause slower boost response and potentially higher voltage ripple during transition time (external noise, load change, boost SW itself).

*Figure 4. Boost Compensation – P Term*

**Recommended setting:** Use default value (01b), which is an optimal value from simulation and IC validation. Figure 4 shows a simplified diagram of phase-gain graph and may not apply for all frequency ranges.
1.7 **EEPROM Address 0x75[7:6] – BOOST_OFFTIME_SEL**

EEPROM Address 0x75[7:6] sets the off time of every boost switching period to control the maximum duty ratio of boost:

- 00 = 131 ns
- 01 = 68 ns
- 10 = 38 ns
- 11 = 24 ns

**Recommended setting:** An off-time that is too high limits boost duty ratio, which limits conversion ratio. Calculate required boost duty ratio at target switching frequency, and select off-time to make possible duty ratio higher than required value.

Example: $V_{\text{IN}} = 9 \text{ V}$, $V_{\text{OUT}} = 35 \text{ V}$, switching frequency = 2.2 MHz

- Required duty ratio = $(35 - 9) / 35 = 74.3\%$
- T of 2.2 MHz = 454 ns
- If setting is 00b = 131 ns, maximum duty ratio = $(454 - 131) / 454 = 71.1\%$, so this setting cannot be selected.
- If setting is 01b = 68 ns, maximum duty ratio = $(454 - 68) / 454 = 85\%$, so this setting can be selected; however, actual efficiency will be less than 100\%, and this increases the required duty ratio, so a shorter off-time setting (38 ns) is a safer choice.

TI recommends using 1 step shorter off-time setting than calculated value. However, avoid using minimum off-time setting (24 ns). This setting often makes violates the conditions of maximum duty ratio of boost, and the operation can be unstable.

1.8 **EEPROM Address 0x75[5:4] – BOOST_BLANKTIME_SEL**

EEPROM Address 0x75[5:4] sets the minimum on-time of every boost switching period to control the minimum duty ratio of boost:

- 00 = 162 ns
- 01 = 88 ns
- 10 = 63 ns
- 11 = 40 ns

**Recommended setting:** Blank time that is too high limits lowest output voltage. Calculate the minimum required boost duty ratio at target switching frequency and select blank-time value to make possible duty ratio lower than required value.

Example: $V_{\text{IN}} = 18 \text{ V}$, $V_{\text{OUT}} = 25 \text{ V}$, switching frequency = 2.2 MHz

- Required duty ratio = $(25 - 18) / 25 = 28\%$
- T of 2.2 MHz = 454 ns
- If setting is 00b = 162 ns, minimum on duty ratio = $162 / 454 = 35.7\%$, so this setting cannot be selected.
- If setting is 01b = 63 ns, minimum on duty ratio = $63 / 454 = 13.9\%$, so this setting can be selected.

Avoid using minimum blank-time setting (40 ns). This short blank time may cause wrong boost current sensing during transient period. 63 ns or 88 ns are good enough for most of application conditions.
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