Two Parallel, Synchronous, Four-Switch Buck-Boost Converters With Droop Method for Higher Power

Hongjia Wu, Daniel Li, Kim Nielson, Vijay Choudhary, Gautam Hari

ABSTRACT

The synchronous, four-switch buck-boost controller LM5176 is widely used in automotive start-stop systems, industrial personal computers (PC), and a variety of other applications. Paralleling two LM5176 converters is an appealing way to meet a larger power requirement while providing many other benefits, such as enhanced modularity, design flexibility, minimized component ratings, and so forth. The benefits, however, can only be effective if the load currents of each module are equally shared, which is the fundamental difficulty of paralleling supplies.

In this application report, a droop method based current sharing architecture is presented. With a very simple extra circuit, the effect of load sharing can be greatly improved. Test results show that with ±2% voltage drop, the current error is within ±1.2% at full load while all the other indexes, including load transient, startup and output ripple are satisfactory.

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1 Introduction

The LM5176 is a synchronous, four-switch, buck-boost DC/DC controller capable of regulating the output voltage at, above, or below the input voltage. The wide input voltage range of 4 V to 55 V (60-V maximum) makes the controller suitable for automotive start-stop systems, industrial PCs, battery backup systems, point-of-sale (POS) terminals, and a variety of other applications.

One single LM5176 converter can deliver power greater than 200 W because of its synchronous switching topology; however, at a higher power, the increased switching and conduction losses can eventually overwhelm a single converter due to excessive board heating. This overheating makes it necessary to parallel power stages to distribute heat sources, which at the same time provides many other benefits: enhanced modularity, design flexibility, and minimized component ratings. These benefits, however, can only be effective if the load currents of each module are equally shared.

Different load sharing implementations are discussed in many literatures, and there is often a tradeoff between complexity and accuracy. Active current sharing, which results in the most accurate load-sharing results, relies on an elaborate negative feedback loop design. And when it comes to automatic master-slave selection, the circuit can be even more sophisticated. See *Paralleling Power – Choosing and Applying the Best Technique for Load Sharing* (Balogh 2003) and *Two Parallel, Synchronous Four-Switch Buck-Boost Converters With Master Slave Method for Higher Power* for further details.

In this application report, a droop method based current sharing architecture is presented. With a very simple extra circuit, the load sharing can be greatly improved. Test results show that with ±2% voltage drop, the current error is within ±1.2% at full load while all the other indexes, including load transient, startup and output ripple are satisfactory.

2 Droop and its Realization

2.1 *What Droop is and why Droop Helps*

A power supply can be modeled as an ideal voltage source in series with a source impedance as shown in Figure 1 and Figure 2. According to Figure 2, the output *I-V* characteristic curve of a LM5176 converter is easily drawn as Figure 3, where Vo(0) represents the output voltage at no load and Vo(Ix) indicates the output voltage when the load equals full load Ix.

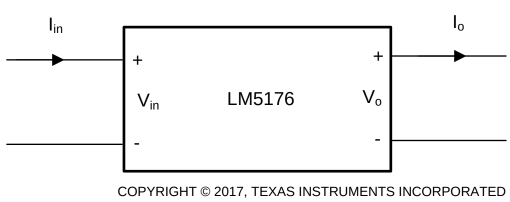

Figure 1. LM5176 Converter as Power Supply

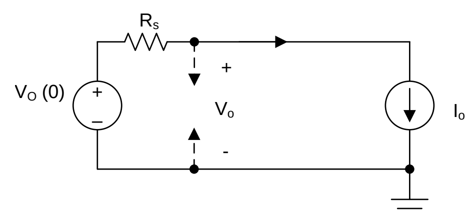

Figure 2. Equivalent Model (Single)

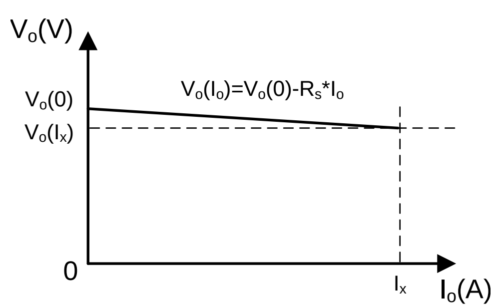

Figure 3. Output *I-V* Characteristic Curve of LM5176 Converter (Slope Exaggerated)

Similarly, for two parallel LM5176 converters, the corresponding equivalence and *I-V* curve will be like Figure 4, Figure 5, and Figure 6.

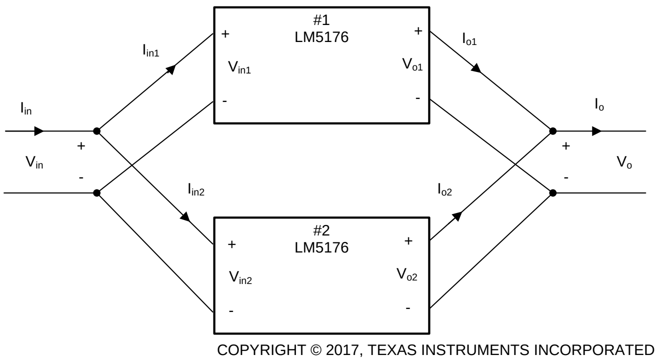

Figure 4. Two Parallel LM5176 Converters as Power Supply

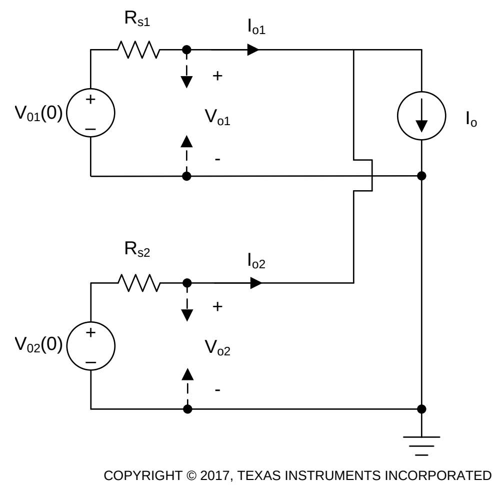

Figure 5. Equivalent Model (Two Parallel)

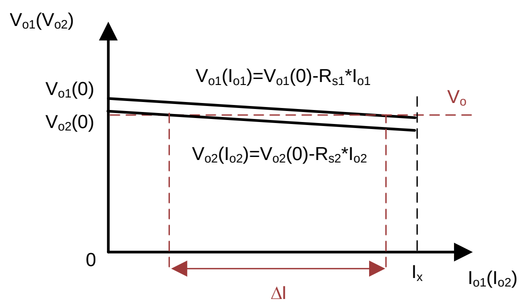

Figure 6. Output *I*-*V* Characteristic Curve of Two Parallel LM5176 Converters (Slope Exaggerated)

Figure 6 explains clearly why loads are not equally shared if power supplies are simply stacked up. It can be observed that although the difference between $V_{o1}(0)$ and $V_{o2}(0)$ is very small, the two *I*-*V* curves can never completely overlap. Therefore, to achieve the same output voltage V_o, there will be two different output currents and the gap between them are up to the slope of the curve, that is, the voltage drop from no load to full load. Due to good load regulation performance, the slope is often very shallow, leading to a considerable ΔI between two parallel supplies.

The droop method got its name from the fact that the output voltage is made to slightly decrease with increasing load current. With careful design, a little sacrifice of load regulation can get equally-distributed load currents in return. Figure 7 shows the output *I*-*V* curve of two parallel supplies with a steeper slope and thus a narrowed ΔI.

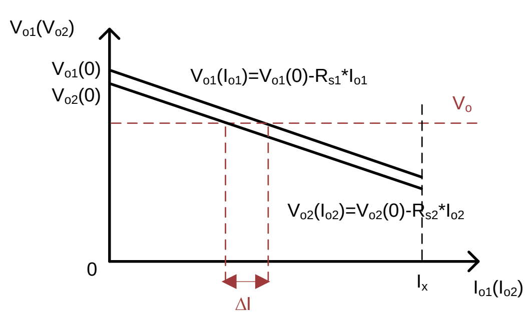

Figure 7. Two Parallel Power Supplies With Droop (Slope Exaggerated)

2.2 Schematic Realization

There are many different ways to implement a larger internal source resistor and a steeper slope. Simply placing a resistor in series achieves this effect but is not practical because of the associated power loss.

A more flexible and attractive way is to sum the information of output current and output voltage and compare the sum with a reference voltage through an error amplifier. While this approach can be implemented in many different ways, Figure 8 illustrates an intuitive version.

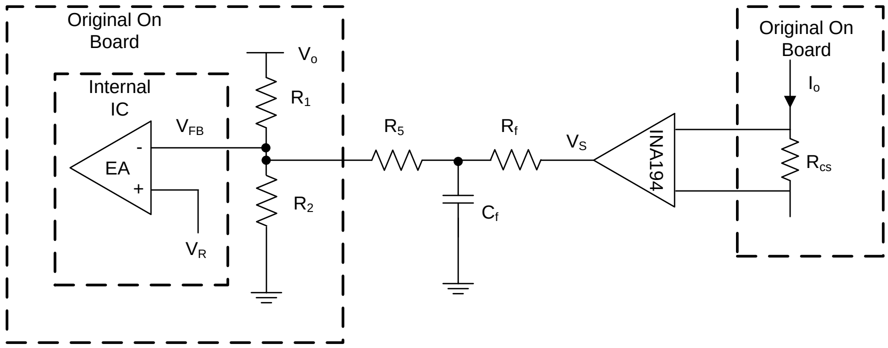

Figure 8. Voltage Feedback Modulation With Output Current Information

As Figure 8 indicates, EA is located on the internal IC, R_1 and R_2 represent the resistor divider on the board and R_{cs} is the current-sensing resistor that is also originally there if the average output current limit function is activated for the LM5176. The only components added are the current-sense amplifier INA194, the filter network R_fC_f, and a resistor R_5.

The voltage across R_{CS} is amplified by the INA194 current-sense amplifier and filtered by the R_fC_f filter to eliminate switching frequency ripple. Using coupling resistor R_5, a current is injected into the FB pin to adjust the output voltage lower as output current is increased. Other gain values can also be selected by choosing different kinds of current-sense amplifiers – the INA-series in particular has gain settings of 20 V/V, 50 V/V, and 100 V/V. Alternative gain values provide a wide selection for the current-sense resistor, making it possible to minimize the power dissipation. The ratio of R_1 and R_2 sets the initial voltage assuming zero current injection at the feedback node. The ratio of R_1 and R_5 sets the gain or level of voltage adjustment for a given amount of current injection into the FB node.

According to Equation 1, the node current equation for the FB pin is:

$$\frac{V_o - V_R}{R_1} + \frac{V_s - V_R}{R_5} = \frac{V_R}{R_2} \quad (1)$$

And the voltage level of the output of INA is:

$$V_s = A \times R_{cs} \times I_o$$

where

- A is the gain of the current-sense amplifier. (2)

Substituting V_s in Equation 1 with Equation 2, derives the final expression for V_o:

$$V_o = (1 + \frac{R_1}{R_2} + \frac{R_1}{R_5}) \times V_R - \frac{R_1}{R_5} \times A \times R_{cs} \times I_o \quad (3)$$

Given V_R = 0.8 V, R_{cs} = 2 mΩ, and setting the voltages from no load to 20-A full load as 12.25 V and 11.75 V, the corresponding values can be calculated: R_1 = 280 kΩ, R_2 = 20 kΩ, R_5 = 1.12 MΩ. Meanwhile, choose R_f = 1 kΩ and C_f = 1µF to filter the high-frequency ripple in the output current. Table 1 lists all the component parameters for the droop circuit.

Table 1. Component Parameters for Droop Circuit

VR (V)	Rcs (mΩ)	Vo(0) (V)	Vo(20 A) (V)	A (V/V)	R1 (kΩ)	R2 (kΩ)	R5 (MΩ)	Rf (kΩ)	Cf (µF)
0.8	2	12.25	11.75	50	280	20	1.12	1	1

Figure 9 shows the final architecture of two parallel LM5176 converters with an extra droop circuit.

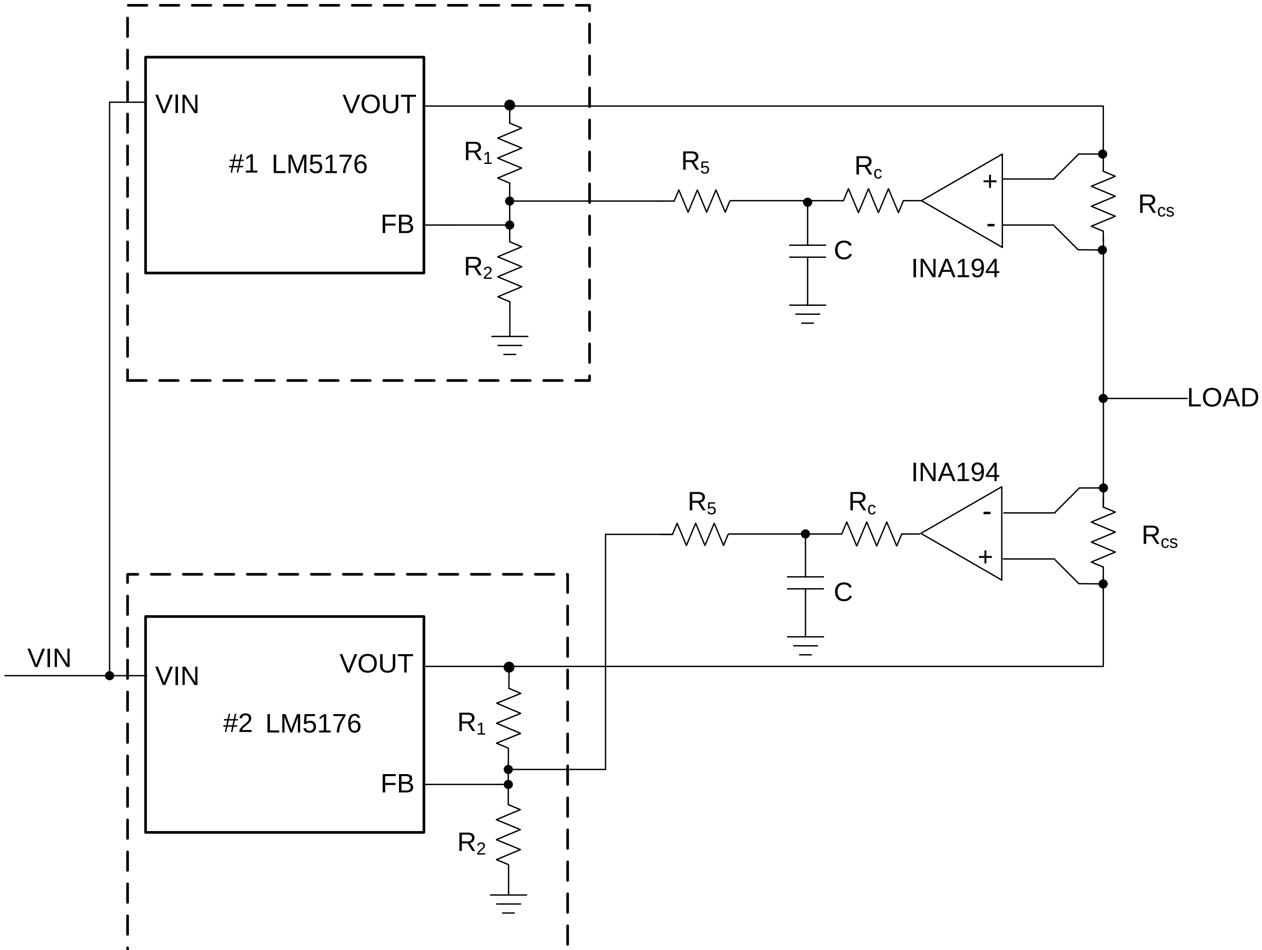

Figure 9. Two Parallel LM5176 Converters With Extra Droop Circuit

3 Test Results

3.1 Output I-V Curve

Figure 10 and Figure 11 present the *I-V* curves of two separate boards before paralleling. Observe that output voltage of each board drops from 12.25 V at no load to 11.75 V at 20-A full load, which is in accordance with the calculation result. With different input voltages, the curves are slightly different.

Figure 10 and Figure 11 show the output *I-V* curves of two separate boards before paralleling.

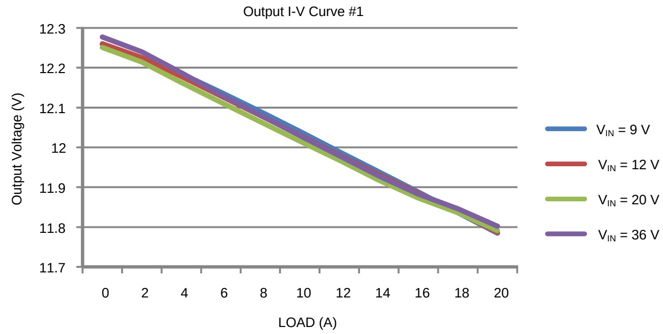

Figure 10. Output *I*-*V* Curve of Board One Before Paralleling

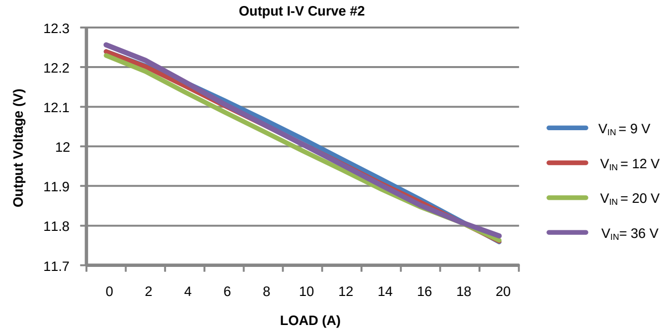

Figure 11. Output *I*-*V* Curve of Board Two Before Paralleling

Figure 12 shows the load regulation for the whole system after these two converters are in parallel, which is almost the same as two separate curves. Figure 13 shows how load is distributed with increasing output current. At 40-A full load, the gap between two phases is only 0.5 A, which indicates that with ±2% voltage droop, the current error is within ±1.2%.

Figure 12 and Figure 13 show output *I*-*V* curve and load distribution of the parallel power.

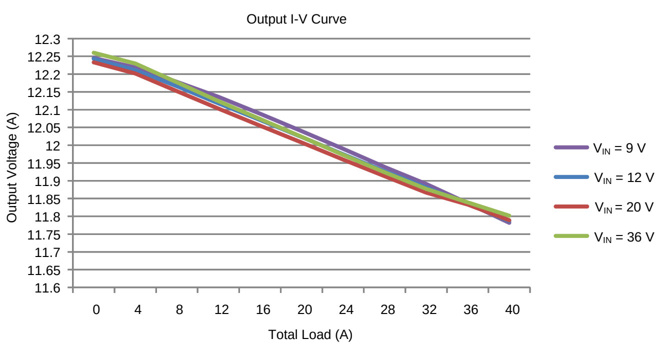

Figure 12. Output *I*-*V* Curve of Parallel Power

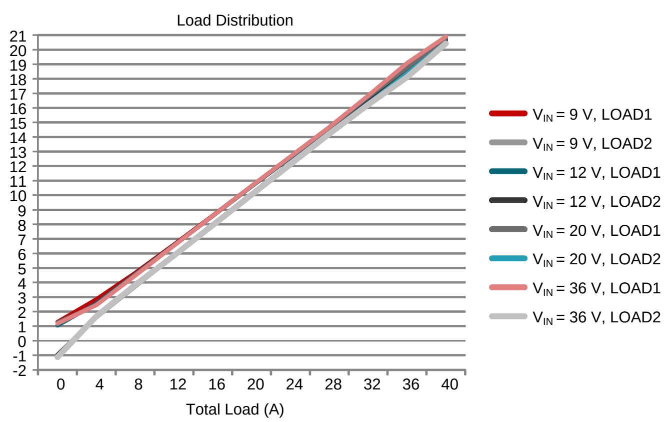

Figure 13. Load Distribution of Two Phases

3.2 SYNC Operation

The RT/SYNC pin of the LM5176 can be used to synchronize the PWM controller to an external clock. The clocks for two parallel LM5176 converters can be either in-phase or 180° out of phase. With in-phase clocks, the current distribution condition will be more visualized.

Figure 14–Figure 17 show the 4 SW nodes and inductor current waveforms in 36-V buck, 12-V buck boost, and 9-V boost region, respectively. Each operation region is stable and the inductor current waveforms of the two phases nearly overlap, indicating equally-distributed load currents.

Figure 14 and Figure 15 show switch nodes and inductor currents in 36-V buck region with 40-A load.

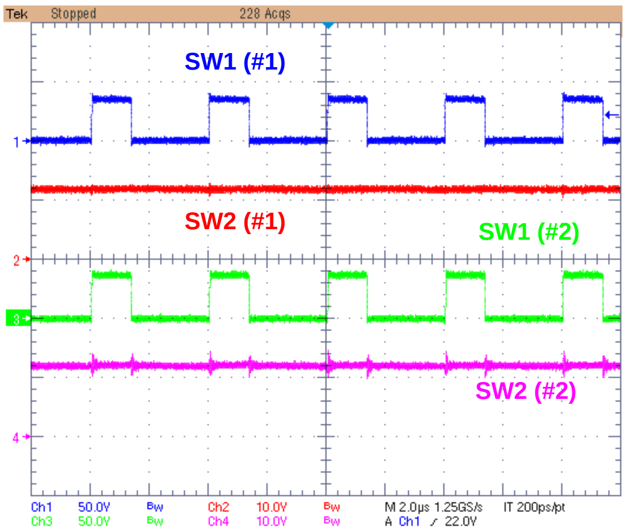

Figure 14. Four Switch Nodes in 36-V Buck Region With 40-A Load

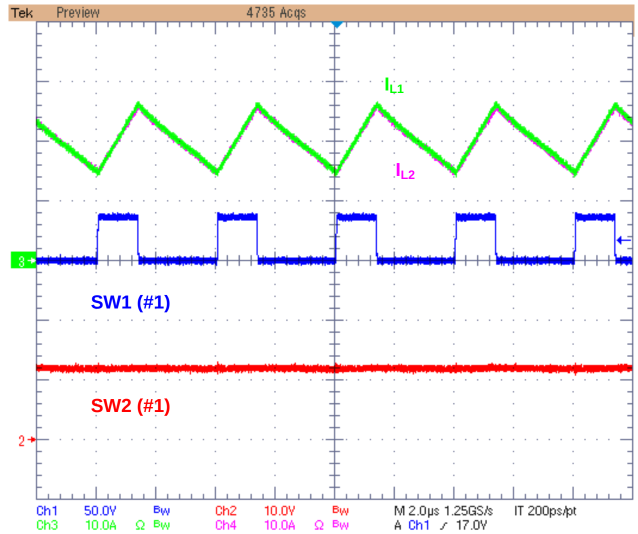

Figure 15. Inductor Current Waveforms in 36-V Buck Region With 40-A Load

Figure 16 and Figure 17 show switch nodes and inductor currents in 12-V buck-boost region with 40-A load.

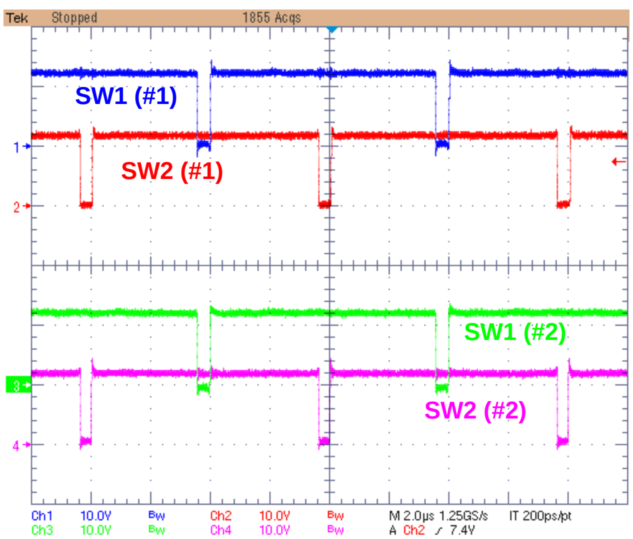

Figure 16. Four Switch Nodes in 12-V Buck-Boost Region With 40-A Load

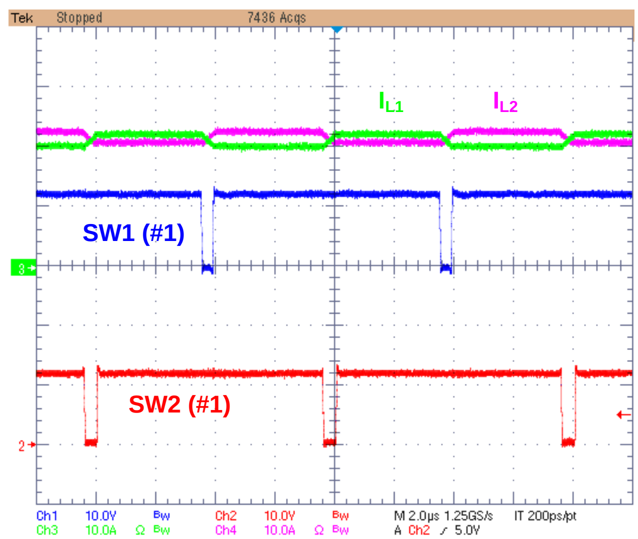

Figure 17. Inductor Current Waveforms in 12-V Buck-Boost Region With 40-A Load

Figure 18 and Figure 19 show switch nodes and inductor currents in 9-V boost region with 40-A load.

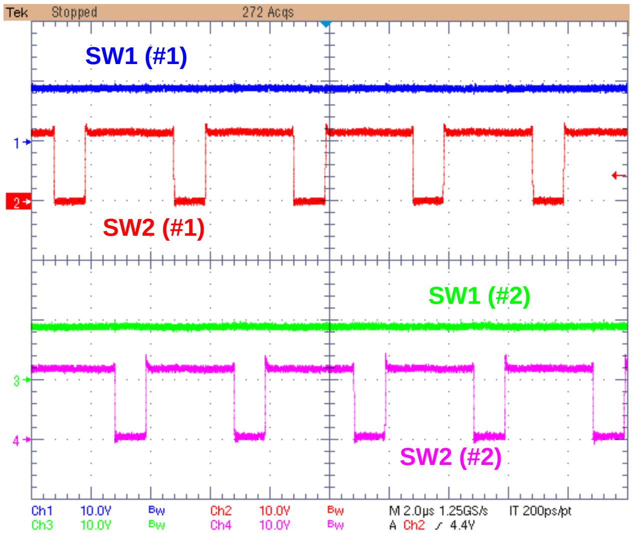

Figure 18. Four Switch Nodes in 9-V Boost Region With 40-A Load

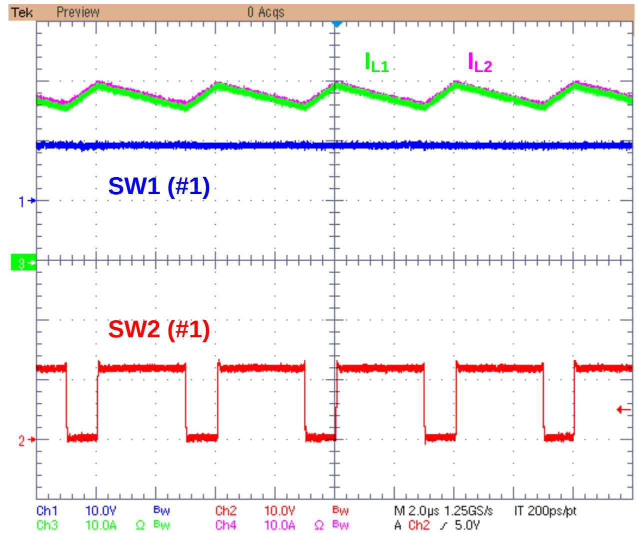

Figure 19. Inductor Current Waveforms in 9-V Boost Region With 40-A Load

Figure 20–Figure 23 show the load transient waveforms in 36-V buck, 12-V buck boost, and 9-V boost region, respectively. Because output voltage is made to vary with load, there are visible voltage steps for 0-, 20-, and 40-A load conditions.

Figure 20 and Figure 21 show load transient in 36-V buck region with 20-A to 40-A and 0-A to 40-A load step.

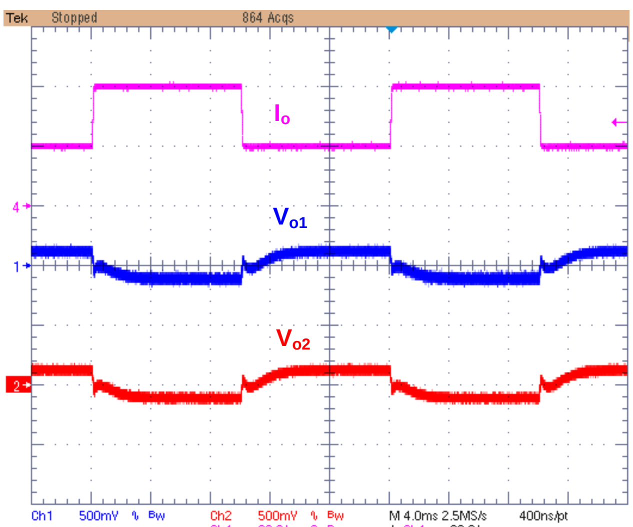

Figure 20. Load Transient in 36-V Buck Region With 20-A to 40-A Load Step

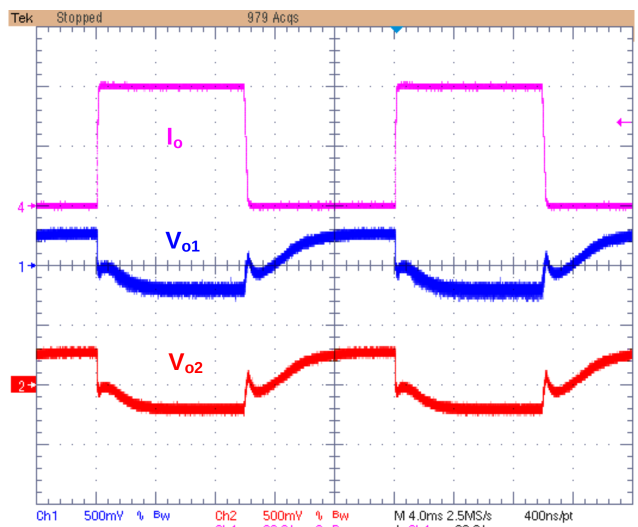

Figure 21. Load Transient in 36-V Buck Region With 0-A to 40-A Load Step

Figure 22 and Figure 23 show load transient in 12-V buck-boost region with 20-A to 40-A and 0-A to 40-A load step.

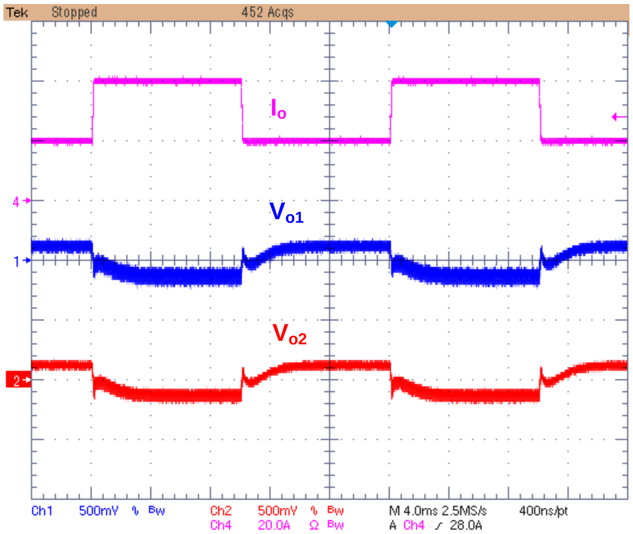

Figure 22. Load Transient in 12-V Buck-Boost Region With 20-A to 40-A Load Step

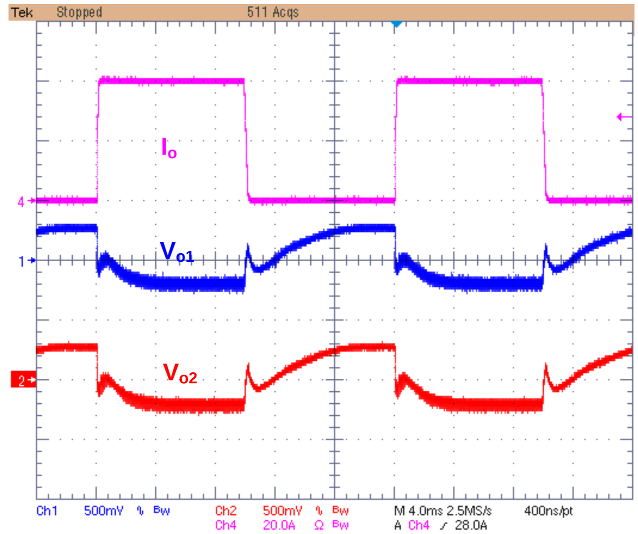

Figure 23. Load Transient in 12-V Buck-Boost Region With 0-A to 40-A Load Step

Figure 24 and Figure 25 show load transient in 9-V boost region with 20-A to 40-A and 0-A to 40-A load step.

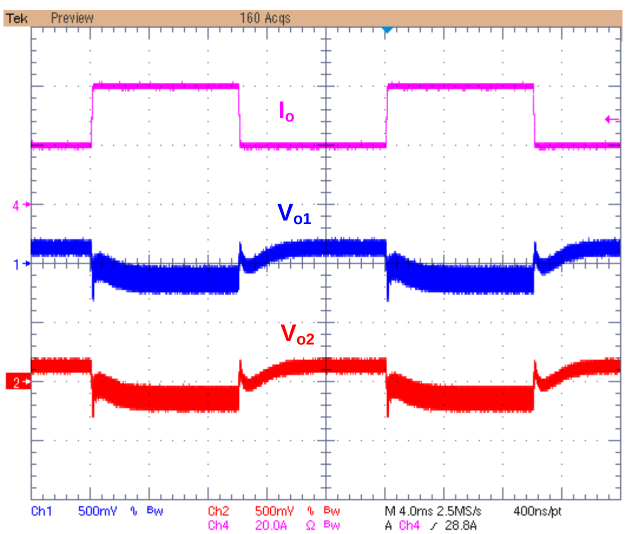

Figure 24. Load Transient in 9-V Boost Region With 20-A to 40-A Load Step

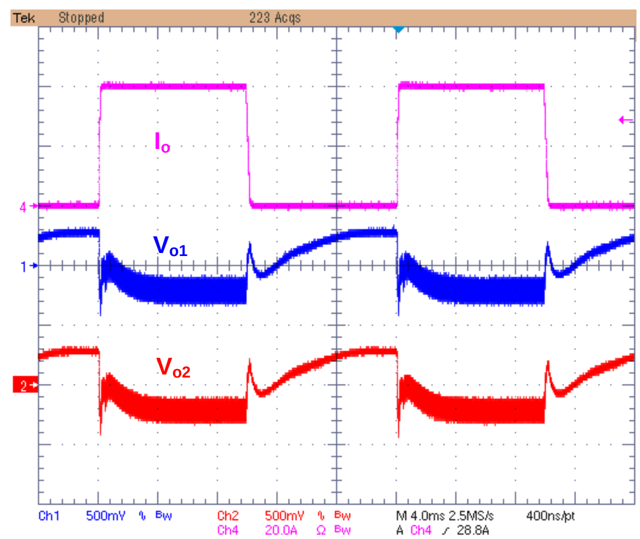

Figure 25. Load Transient in 9-V Boost Region With 0-A to 40-A Load Step

Figure 26–Figure 31 are the output ripple waveforms in 36-V buck, 12-V buck boost, and 9-V boost region, respectively.

Figure 26 and Figure 27 show output voltage ripple in 36-V buck region with no load and 40-A load.

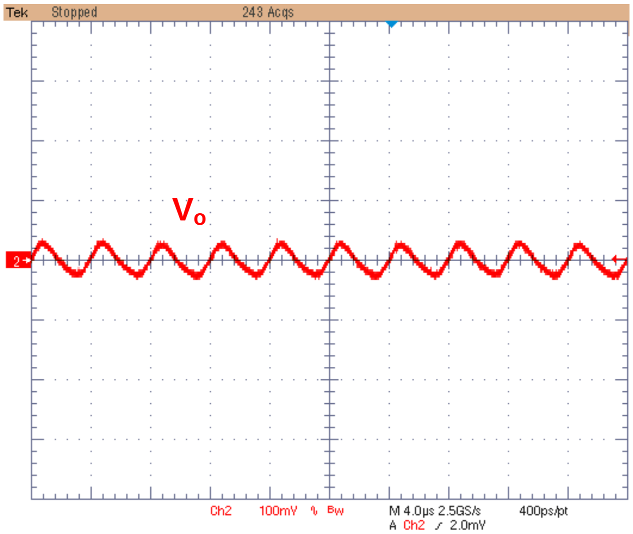

Figure 26. Output Voltage Ripple in 36-V Buck Region With No Load

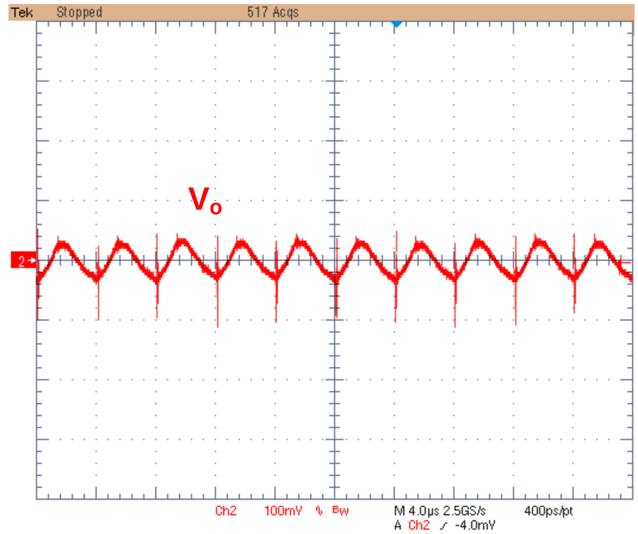

Figure 27. Output Voltage Ripple in 36-V Buck Region With 40-A Load

Figure 28 and Figure 29 show output voltage ripple in 12-V buck-boost region with no load and 40-A load.

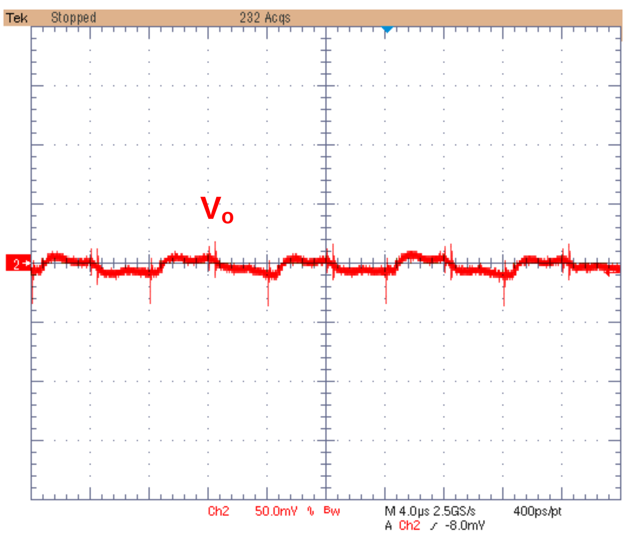

Figure 28. Output Voltage Ripple in 12-V Buck-Boost Region With No Load

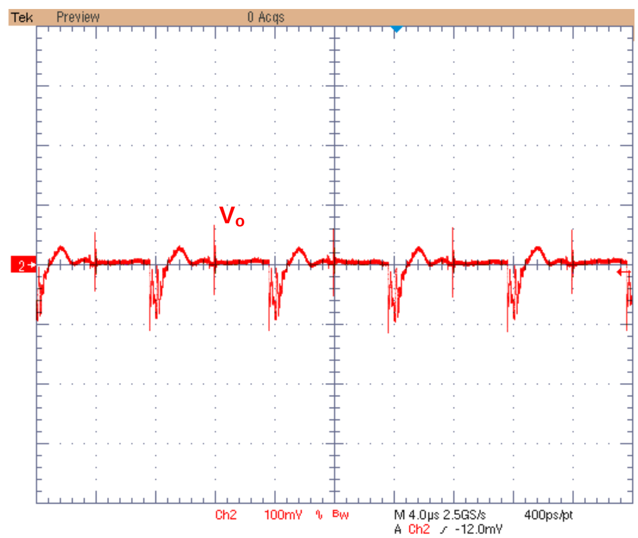

Figure 29. Output Voltage Ripple in 12-V Buck-Boost Region With 40-A Load

Figure 30 and Figure 31 show output voltage ripple in 9-V boost region with no load and 40-A load.

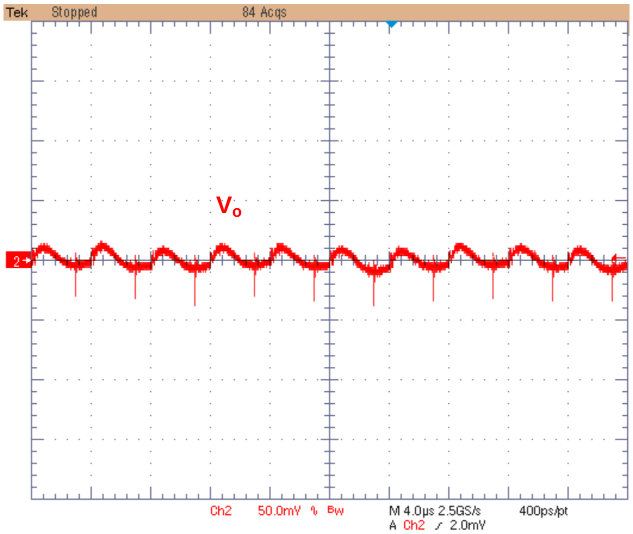

Figure 30. Output Voltage Ripple in 9-V Boost Region With No Load

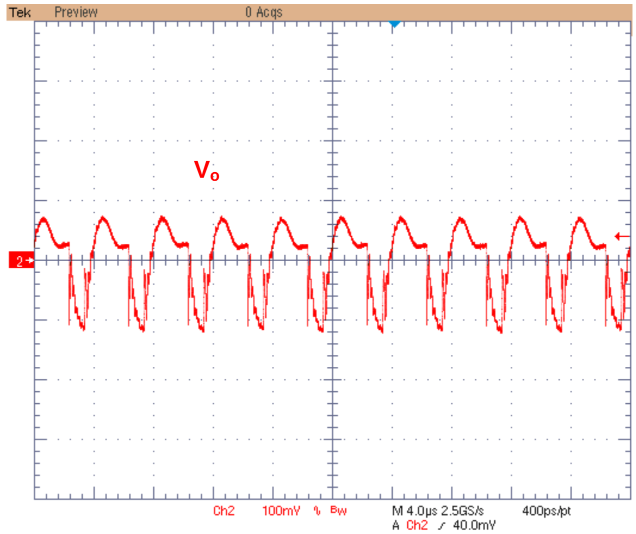

Figure 31. Output Voltage Ripple in 9-V Boost Region With 40-A Load

Figure 32–Figure 37 present the start-up waveforms in 36-V buck, 12-V buck boost, and 9-V boost region, respectively. Because every two boards are not exactly the same, there is always sequential order during startup, which explains the reason that for a certain period of the start-up process, the loads are not equally distributed.

Figure 32 and Figure 33 show 40-A start-up in 36-V buck region.

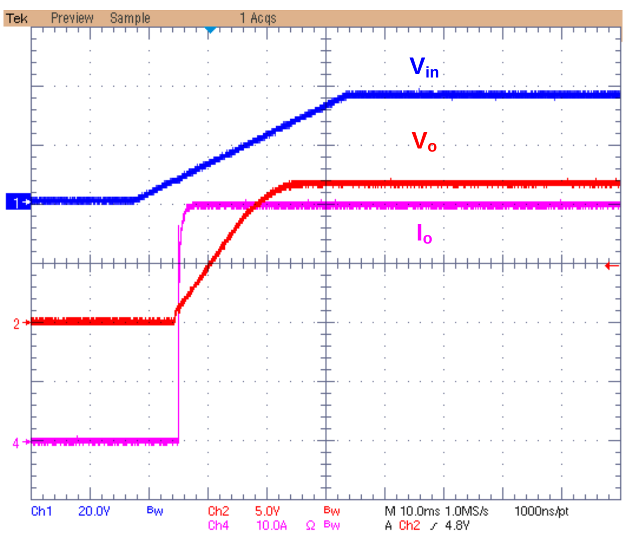

Figure 32. 40-A Start-Up in 36-V Buck Region Total Output Current Waveform

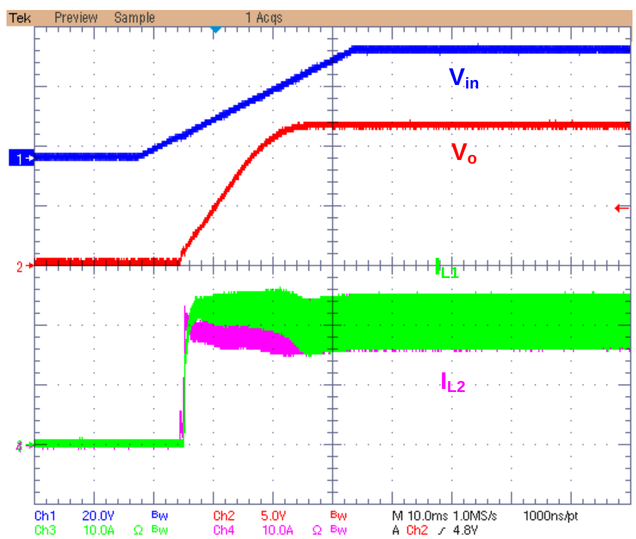

Figure 33. 40-A Start-Up in 36-V Buck Region Two Phase Inductor Currents

Figure 34 and Figure 35 show 40-A start-up in 12-V buck-boost region.

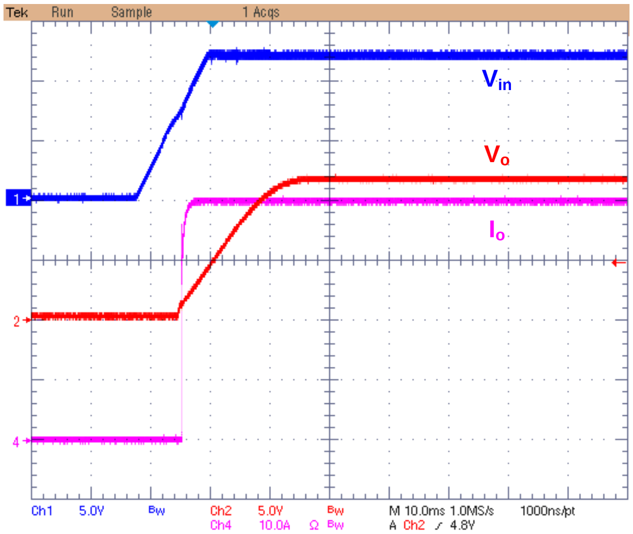

Figure 34. 40-A Start-Up in 12-V Buck-Boost Region Total Output Current Waveform

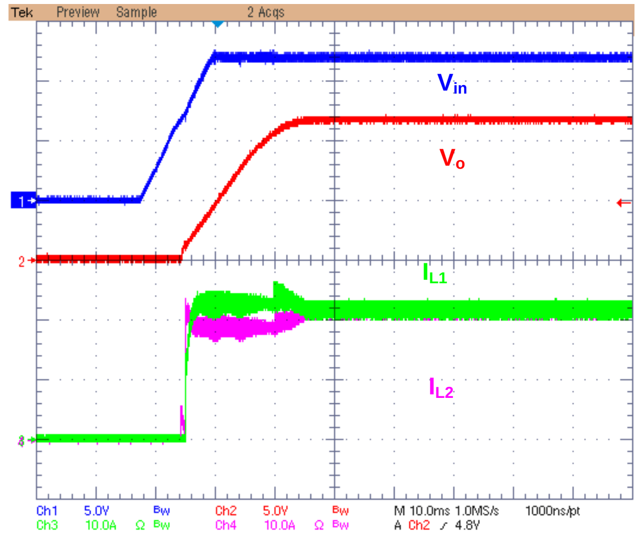

Figure 35. 40-A Start-Up in 12-V Buck-Boost Region Two Phase Inductor Currents

Figure 36 and Figure 37 show 40-A start-up in 9-V boost region.

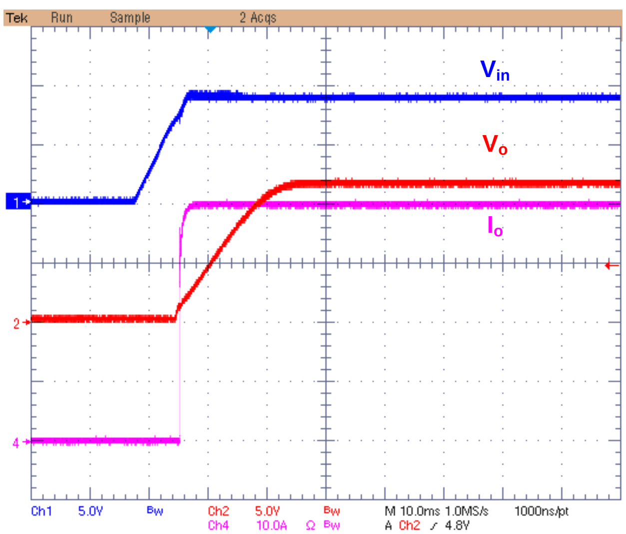

Figure 36. 40-A Start-Up in 9-V Boost Region Total Output Current Waveform

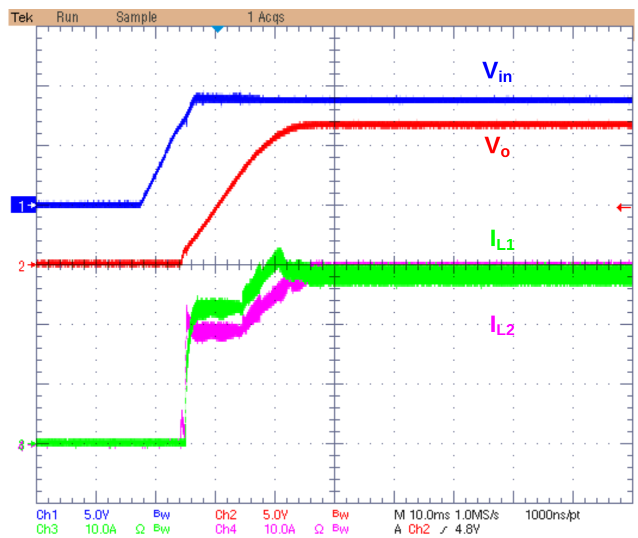

Figure 37. 40-A Start-Up in 9-V Boost Region Two Phase Inductor Currents

Due to the parallel structure of two LM5176 converters, the heat sources are also distributed. With 600CFM air flow, Figure 38–Figure 40 show the 40-A load thermal condition in 36-V buck, 12-V buck boost, and 9-V boost, respectively.

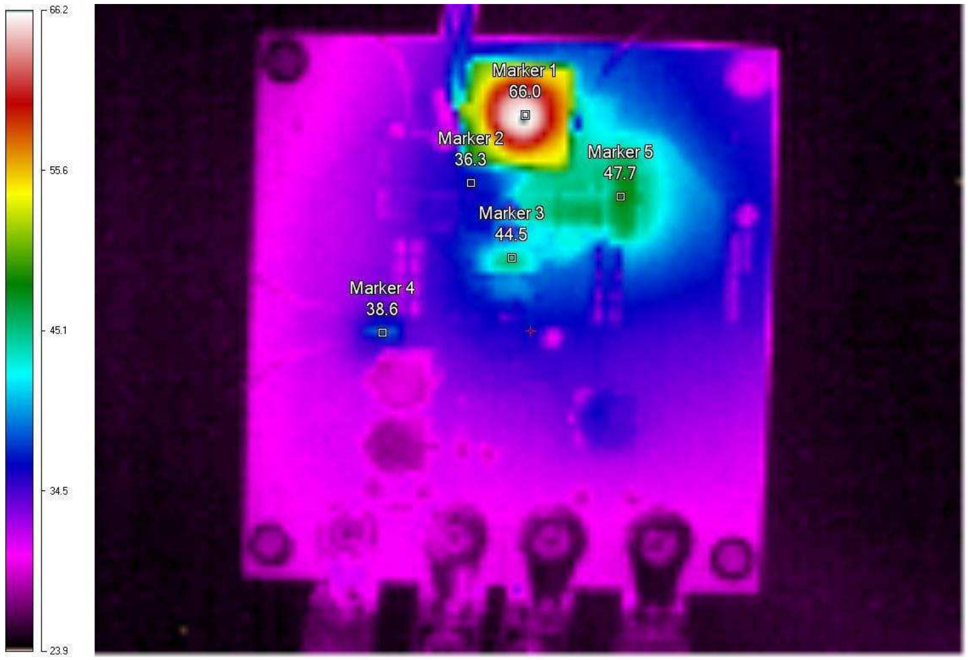

Figure 38. 40-A Load Thermal Condition in 36-V Buck Region

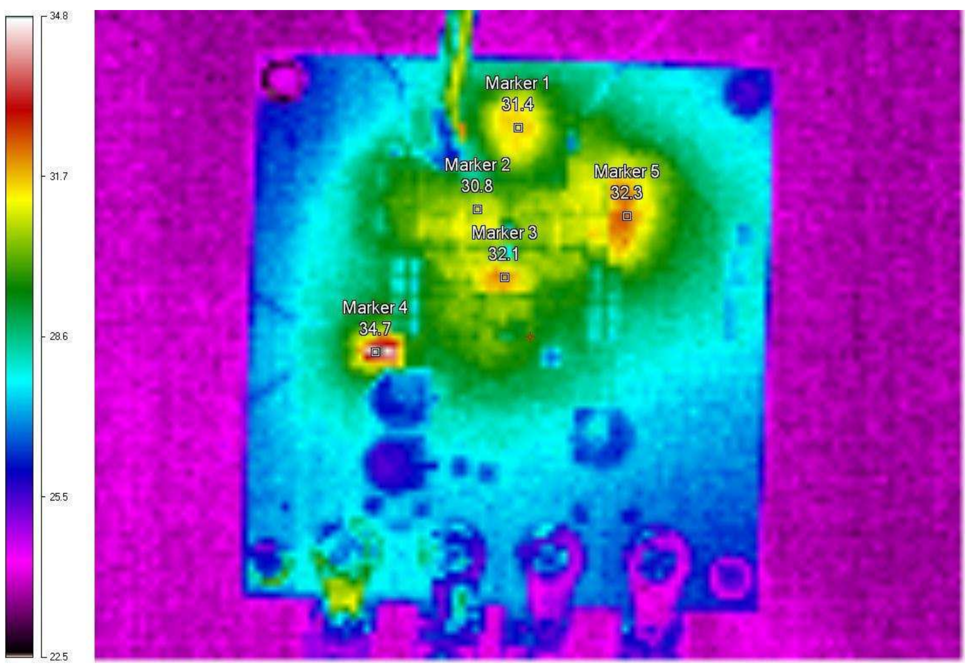

Figure 39. 40-A Load Thermal Condition in 12-V Buck-Boost Region

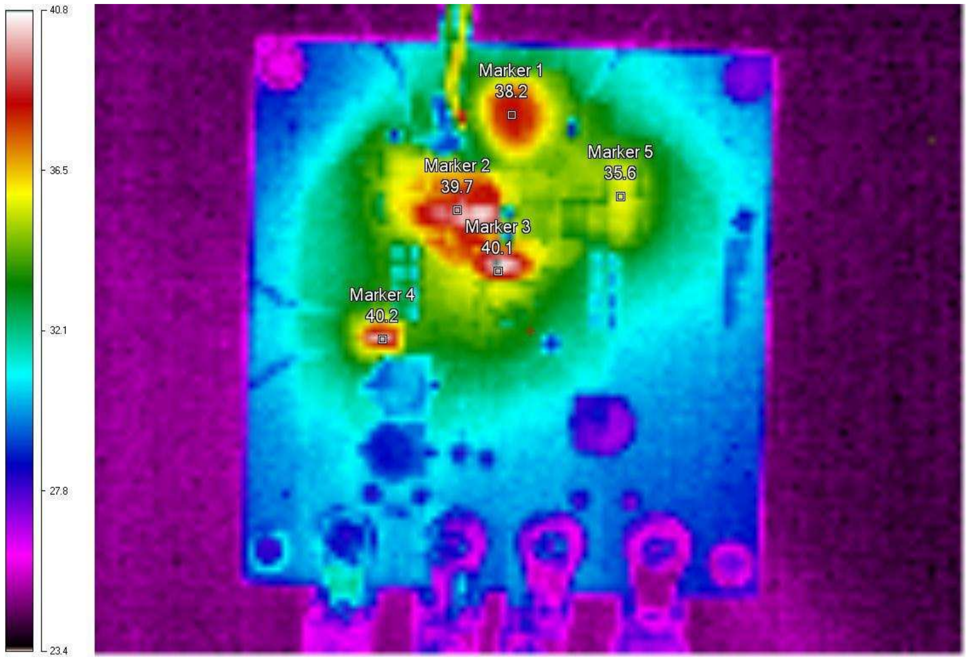

Figure 40. 40-A Load Thermal Condition in 9-V Boost Region

3.3 *Interleaved Operation*

As previously mentioned, two LM5176 converters can also be configured as 180° out of phase, that is, interleave architecture. Interleave architecture provides a better solution for smaller output voltage ripple.

To show the discrimination with in-phase operation, Figure 41– present the 4 SW nodes and inductor current waveforms in 36-V buck, 12-V buck boost, and 9-V boost region, respectively.

Figure 41 and Figure 42 show switch nodes and inductor currents in 36-V buck region with 40-A load.

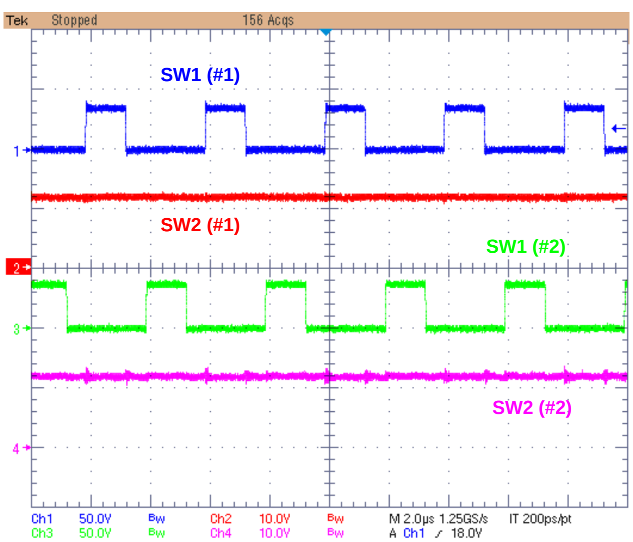

Figure 41. Four Switch Node in 36-V Buck Region With 40-A Load

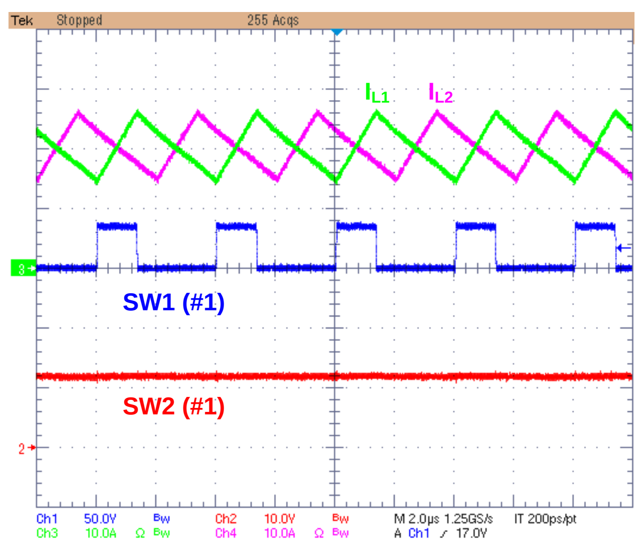

Figure 42. Inductor Current Waveforms in 36-V Buck Region With 40-A Load

Figure 43 and Figure 44 show switch nodes and inductor currents in 12-V buck-boost region with 40-A load.

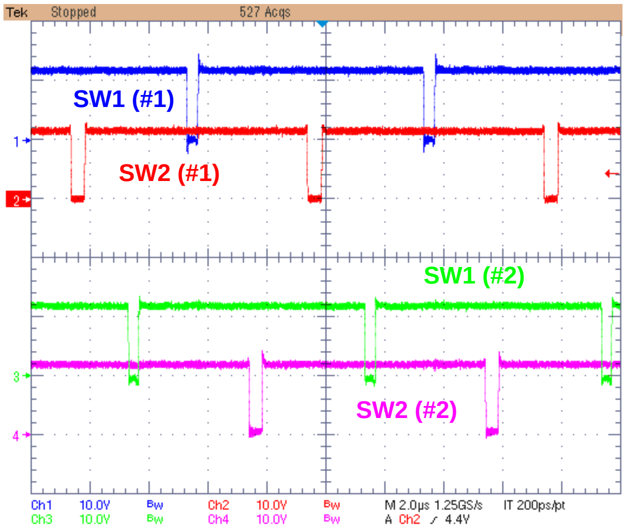

Figure 43. Four Switch Nodes in 12-V Buck-Boost Region With 40-A Load

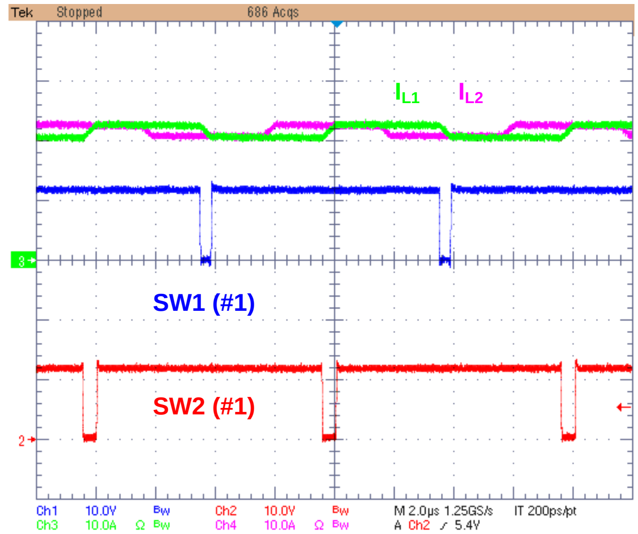

Figure 44. Inductor Current Waveforms in 12-V Buck-Boost Region With 40-A Load

Figure 45 and Figure 46 show switch nodes and inductor currents in 9-V boost region with 40-A load.

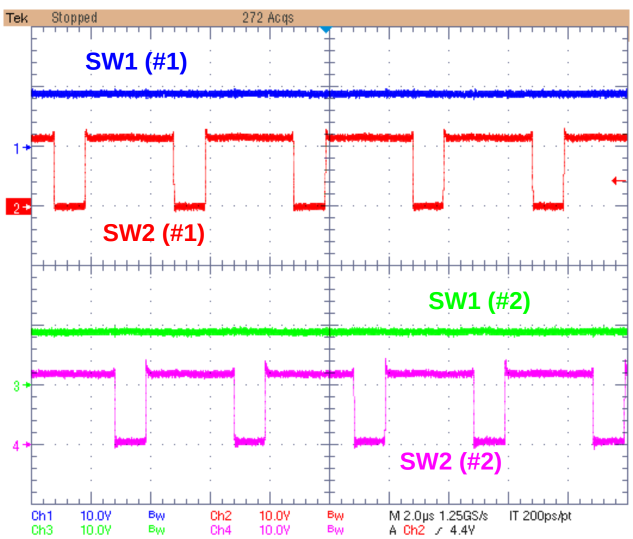

Figure 45. Four Switch Nodes in 9-V Boost Region With 40-A Load

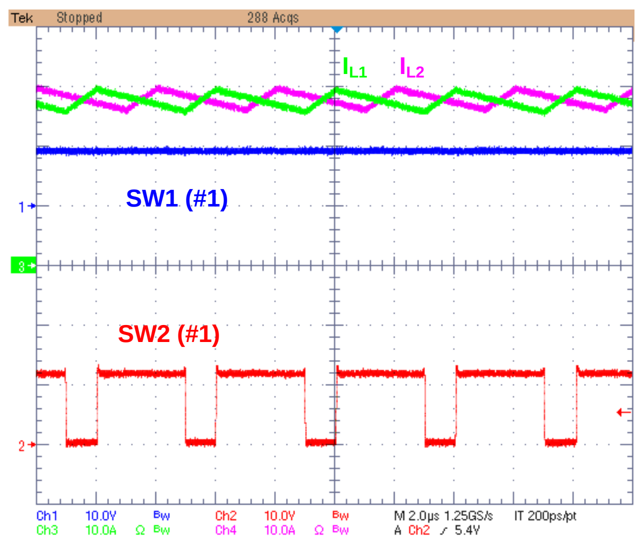

Figure 46. Inductor Current Waveforms in 9-V Boost Region With 40-A Load

Figure 47–Figure 52 show the output ripple in 36-V buck, 12-V buck boost, and 9-V boost region, respectively. Compared with Figure 26–Figure 31, the amplitude of output voltage ripple is reduced while the frequency is doubled.

Figure 47 and Figure 48 show output voltage ripple in 36-V buck region with no load and 40-A load.

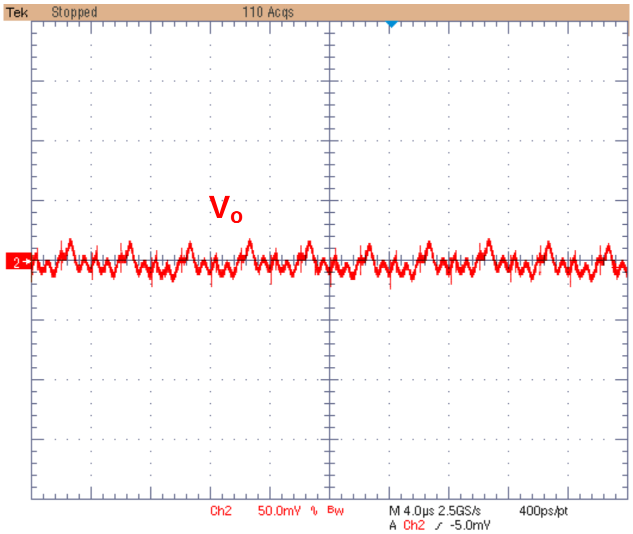

Figure 47. Output Voltage Ripple in 36-V Buck Region With No Load

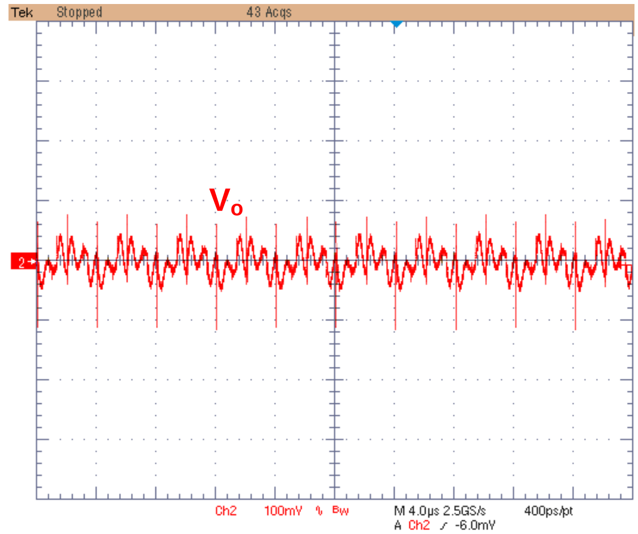

Figure 48. Output Voltage Ripple in 36-V Buck Region With 40-A Load

Figure 49 and Figure 50 show output voltage ripple in 12-V buck-boost region with no load and 40-A load.

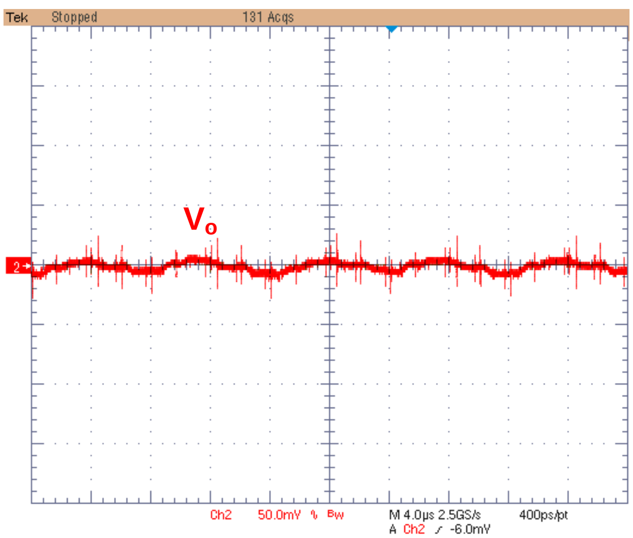

Figure 49. Output Voltage Ripple in 12-V Buck-Boost Region With No Load

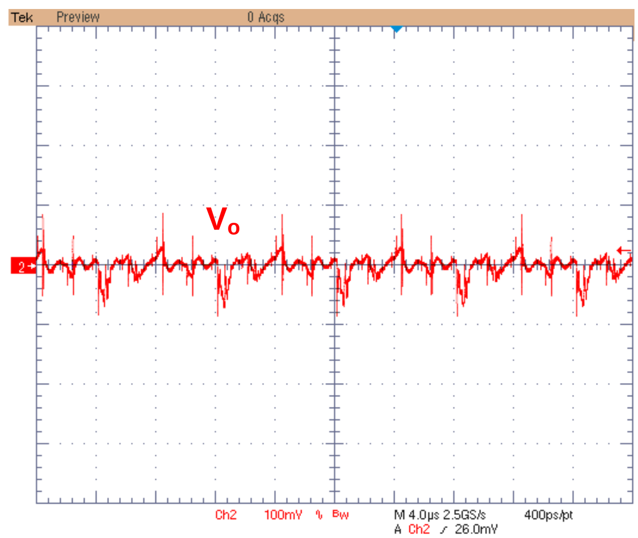

Figure 50. Output Voltage Ripple in 12-V Buck-Boost Region With 40-A Load

Figure 51 and Figure 52 show output voltage ripple in 9-V boost region with no load and 40-A load.

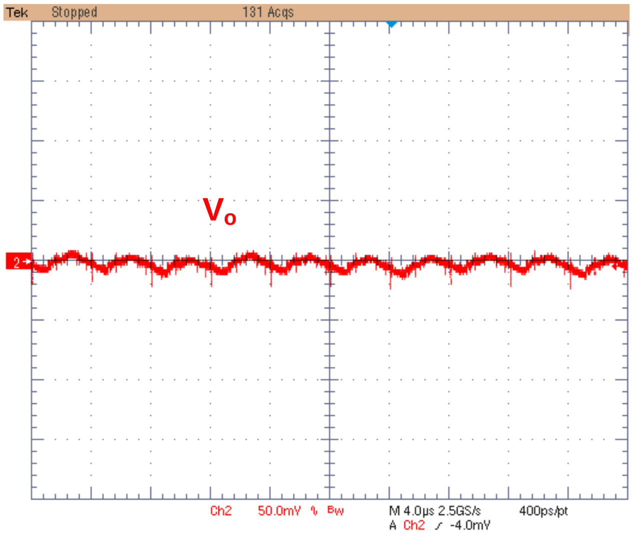

Figure 51. Output Voltage Ripple in 9-V Boost Region With No Load

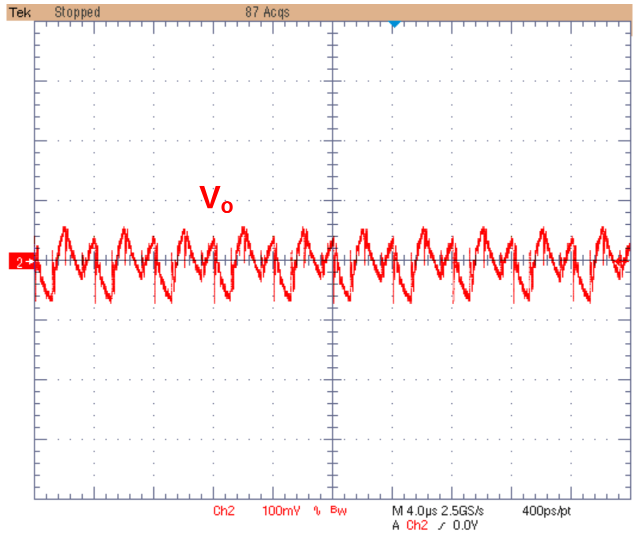

Figure 52. Output Voltage Ripple in 9-V Boost Region With 40-A Load

4 Conclusion

Unequal load distribution is the fundamental difficulty of parallel power supplies. In this application report, a droop method based current sharing architecture is presented. With a simple extra droop circuit, two LM5176 converters can share equal currents with ±1.2% error at full load while the voltage drop is within ±2%. Experiment results for parallel LM5176 converters with 480-W capability were presented. This provides an attractive solution for high-power applications.

5 References

1. Texas Instruments, LM5176 55-V Wide VIN Synchronous 4-Switch Buck-Boost Controller Data Sheet
2. Laszlo Balogh, Paralleling Power--Choosing and Applying the best technique for load sharing