ABSTRACT

This application report summarizes the necessary steps to setup the direct memory access controller (DMA) to transfer data between the SCI and the data RAM of the microcontroller, freeing the CPU during the entire message transmission. Detailed code examples are provided as guidelines for the different setup steps.

Project collateral and source code discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/spna213.
1 Introduction

The DMA controller is used to transfer data between two locations in the memory map in the background of CPU operations. This application report demonstrates how to use the DMA to free CPU cycles while transmitting SCI messages. The example was designed to be run on the LAUNCHXL2 series of launchpads and will transmit an incremented number totaling 1890 characters using SCI2 in multi-buffered mode. SCI2 is included in the debug interface USB connection and can be monitored with a standard terminal.

2 Basic Steps to Setup a DMA SCI Transfer

In order to use the DMA for data transfer between the SCI and the device data RAM, the module needs to be setup properly. The following bullets show the basic steps that need to be performed to do this. Each item is discussed in detail in the following sections of this document. In the example, this is completed by the scidmaInit function.

- Initialize the desired SCI
- Enable DMA
- Enable SCI DMA transfer interrupts (optional interrupt mode)
- Initialize DMA transfer group
- Set data transfer base address
- Setup transfer direction in the configuration RAM (TCR)
- Trigger DMA transfers
- Get transfer ready notification
2.1 DMA Configuration With scidmaInit()

Configure the DMA for the most efficient transfers allowed by the system and your application. Here is an example of the DMA configuration with SCI2 in multi-buffer mode for a transmission. Before scidmaInit is called, scInit and linsci2enableMBUFF should be called to configure SCI2 for multi-buffer mode. The DMA reads 32 bits at a time from the data RAM incrementing the address, writing 32 bits of data to the transmit buffer without incrementing the address. The SCI transmits one byte at a time until all 4 bytes have been transmitted, then signals that it is ready for more data either with a ready or request signal to the desired controller - in this case the DMA. Then, the DMA transfers the next 4 bytes until the entire message has been sent and sets a complete flag in the data RAM for the CPU to know when it is ready to send another message.

```c
/* Populate dma control packets structure */
g_dmaCTRLPKT.CHCTRL = 0;    /* channel control */
g_dmaCTRLPKT.ELCNT = 1;      /* element count */
g_dmaCTRLPKT.ELDOFFSET = 0;  /* element destination offset */
g_dmaCTRLPKT.ELSOFFSET = 0;  /* element source offset */
g_dmaCTRLPKT.FRDOFFSET = 0;  /* frame destination offset */
g_dmaCTRLPKT.FRSOFFSET = 0;  /* frame source offset */
g_dmaCTRLPKT.PORTASGN = 4;   /* port b */
g_dmaCTRLPKT.RDSIZE = ACCESS_32_BIT; /* read size */
g_dmaCTRLPKT.WRSIZE = ACCESS_32_BIT; /* write size */
g_dmaCTRLPKT.TTYPE = FRAME_TRANSFER; /* transfer type */
g_dmaCTRLPKT.ADDMODERD = ADDR_INC1; /* address mode read */
g_dmaCTRLPKT.ADDMODEWR = ADDR_FIXED; /* address mode write */
g_dmaCTRLPKT.AUTOINIT = AUTOINIT_OFF; /* autoinit */
```

Note that the peripheral bus does not allow for 64-bit unaligned accesses. When in multi-buffer mode, the largest accesses possible to the SCI TDx registers is 32 bits. Care should be taken to account for CPU endianness as the SCI has the register formatted in little endianism.

2.2 DMA SCI Transmit With scidmaSend()

Every time scidmaSend is called, it completes the control packet with the addresses and number of bytes to transfer.

```c
/* Populate dma control packets structure */
g_dmaCTRLPKT.SADD = (uint32_t)source_address; /* source address */
g_dmaCTRLPKT.DADD = (uint32_t)(4*(linREG->TDx)); /* destination address */
g_dmaCTRLPKT.FRCNT = strlen(source_address)/4+8; /* frame count */
```

Then scidmaSend calls the dmaSetCtrlPacket to update the dma module. Once this is complete, the scidmaSend configures the DMA to start the transfer freeing the CPU to do other work until the entire message has been transmitted. A flag has been added to the scidmaSend to prevent it from starting a new message until it is finished with the last message.
/** @fn void scidmaSend(char *source_address)
 * @brief Initialize the SCI and DMA to transfer SCI data via DMA
 * @note This function configures the SCI to trigger a DMA request when the SCI TX is complete.
 * @This function configures the DMA for SCI2 in single buffer or multi-buffer mode.
 * In single buffer mode
 * the DMA moves 1 Byte to the SCI2 transmit register when the request is set.
 * In multi-buffer mode
 * the DMA moves 4 Bytes to the SCI2 transmit buffer when the request is set.
 */
void scidmaSend(char *source_address)
{
#if ((__little_endian__ == 1) || (__LITTLE_ENDIAN__ == 1))
    uint8 dest_addr_offset=0; /* 0 for LE */
#else
    uint8 dest_addr_offset=3; /* 3 for BE */
#endif
/* Wait for the DMA to complete any existing transfers */
while(DMA_Comp_Flag != 0x55AAD09E);
/* Reset the Flag to not Done*/
DMA_Comp_Flag = ~0x55AAD09E;
/* - Populate dma control packets structure */
g_dmaCTRLPKT.SADD = (uint32)source_address; /* source address */
if (((scilinREG->GCR1 >> 10U) & 1U) == 0U) { /* SCI2 multi-buffer mode */
    g_dmaCTRLPKT.DADD = (uint32)(&(scilinREG->TD))+dest_addr_offset;
    g_dmaCTRLPKT.RDSIZE = ACCESS_8_BIT; /* read size */
    g_dmaCTRLPKT.WRSIZE = ACCESS_8_BIT; /* write size */
    g_dmaCTRLPKT.FRCNT = strlen(source_address); /* frame count */
} else {
    g_dmaCTRLPKT.DADD = (uint32)(&(linREG->TDx));
    g_dmaCTRLPKT.RDSIZE = ACCESS_32_BIT; /* read size */
    g_dmaCTRLPKT.WRSIZE = ACCESS_32_BIT; /* write size */
    g_dmaCTRLPKT.FRCNT = strlen(source_address)/4+8* /* frame count */
}
/* - setting dma control packets for transmit */
dmaSetCtrlPacket(DMA_CH0,g_dmaCTRLPKT);
/* - setting the dma channel to trigger on h/w request */
dmaSetChEnable(DMA_CH0, DMA_HW);
/* Enable TX DMA */
scilinREG->SETINT = (1 << 16);
} /* scidmaSend */
3 HALCoGen Example

3.1 Introduction

This example demonstrates how to use the DMA to transfer a message to the SCI in multi-buffer mode for transmission. Without the DMA the CPU would have to move data to the SCI after every buffer sized bytes. With the DMA the CPU is free for the entire message transmission.

Project collateral and source code discussed in this application report were developed using HALCoGen 04.02.00 for the LaunchXL2 launchpad. This code was written to be easily ported to any HALCoGen project by copying sys_main.c, notification.c and sci.c. When generating a HALCoGen project, select any Hercules device, enable the drivers for the desired SCI, enable the necessary VIM channels such as 40 (DMA BTCA) and configure the desired SCI settings.

On the LaunchXL2, SCI2 is the only SCI that supports multi-buffer transfers and is routed to the USB debug connector as XDS110 Class Application/User UART (COM#). Configure the terminal for a baud rate of 115.2 Kbps, 8 data bits, 1 stop bit, no parity, no flow control. Below is the expected output.

![Figure 1. HALCoGen LaunchXL2 SCI2 Configuration 115200bps 81NN](image-url)
HALCoGen Example

scidmaSend Example - DMA to transfer single byte from RAM to the SCI

scidmaSend Example - DMA to transfer four bytes from RAM to SCI

scidmaSend Example Complete, 1890 characters sent

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