Disabling the Internal Oscillator on the VC5503/C5506/C5507/C5509/C5509A DSP

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ABSTRACT
This application report contains information and examples on how to disable the internal clock oscillator on the TMS320VC5503, TMS320VC5506, TMS320VC5507, TMS320VC5509, and TMS320VC5509A DSPs to minimize power consumption. The document contains an overview of how the internal clock oscillator operates, and how to disable it as part of the IDLE power-down feature. It also discusses how to wake up the oscillator from an IDLE power down.

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1 Overview of IDLE Operations

A critical component of power conservation is minimizing the power used when an application is in an idle or low-activity state. The DSP incorporates low-activity power management through the implementation of user-controllable IDLE domains. These domains are sections of the device that can be selectively enabled or disabled under software control. When disabled, a domain enters a very low-power idle state in which memory contents are still maintained. When the domain is enabled, it returns to normal operations. The various domains include the central processing unit (CPU), direct memory access (DMA), peripherals, external memory interface (EMIF), and the clock-generation circuitry. For maximum power conservation, the IDLE power-down feature is most commonly used. This feature stops the CPU, DMA, and EMIF domains, except for the internal oscillator with external crystal resonator that is connected to pins X1 and X2/CLKin. This is shown in Figure 1.

![Figure 1. Internal System Oscillator External Crystal](image)

There is a distinction between clock-generation circuitry and the internal oscillator. The clock-generation circuitry refers to the phase-lock loops (PLLs) that are within the DSP. The phase-lock loops provide clock signals to the various internal peripherals and digital signal processor (DSP) core.

The internal oscillator is the input clock source to the clock-generation PLLs. The internal oscillator is not the crystal resonator, but is the circuitry inside the DSP that drives the crystal to oscillate. By turning off the oscillator, you can further reduce the amount of current consumed. This document outlines, step by step, how to turn OFF the internal oscillator using software as part of the IDLE power-down feature.

The DSP includes two independent clock generators that are sourced by the internal oscillator: the DSP clock generator and the universal serial bus (USB) clock generator. Both clock generators are similar in operation and functionality. The DSP clock generator supplies the clock that is used by the CPU, and all of the other peripherals inside the DSP. The USB clock generator supplies the clock needed to operate the USB peripheral.
The TMS320VC5509 USB clock generator consists of a digital phase lock loop (DPLL) as shown in Figure 2.

Figure 2. TMS320VC5509 USB Clock Generator
The C5506, C5507, and C5509A USB clock generators consist of an analog phase locked loop (APLL) as well as a DPLL. Figure 3 shows a diagram of the internal oscillator and its relationship to the clock generators.

![Diagram of internal oscillator and clock generators](image)

**Figure 3. TMS320VC5506/C5507/C5509A USB Clock Generator**

Each clock generator also incorporates an IDLE mode for power conservation. It can be placed in its IDLE mode by turning off the CLKGEN IDLE domain in the IDLE configuration register (ICR). When the clock generator is idled, the output clock is stopped and held high. The IDLE status register (ISR) indicates which domains are currently idled, and the ICR indicates which domains will be active the next time the IDLE instruction is executed. Please note that the TMS320VC5506/C5507/C5509A USB APLL is not part of the USB CLKGEN and cannot be IDLEd. To idle the USB PLL, you have to switch to the USB DPLL from the APLL and then enter IDLE. For details on this procedure, see Using the USB APLL on the TMS320VC5506/C5507/C5509A (SPRA997).

The DSP and USB clock generators are independent. If an IDLE instruction turns off the DSP clock generator, the USB module can keep running and vice versa. If either the DSP clock generator or the USB clock generator are idled using the IDLE power-down feature, the internal clock oscillator remains active. To disable the internal clock oscillator, both the DSP clock generator and the USB clock generator must be enabled before the IDLE power-down sequence can be initiated. This is also true for the case where a system does not incorporate a USB port or interface.

2 **Disabling the Internal Oscillator**

Figure 4 shows a complete block diagram and step-by-step details on how to disable the internal clock oscillator for the TMS320VC5509. Figure 5 shows the same procedure for the TMS320VC5506/C5507C/C5509A. Please note that if the on-chip emulation is used on the TMS320VC5506/C5507C/C5509A, you must disconnect the emulator for the device to go into IDLE properly. If the emulator is left connected, the DSP will not go into IDLE.
Attached with this document is a sample assembly program that demonstrates the oscillator disable process for Figure 5.

**Prepare Interrupts for IDLE**
1. Clear IFR0, IFR1 by writing 0xFFFF to them
2. Enable wake-up interrupt in IER1

**Begin Oscillator Disable**

**Is USB present and enabled?**

**Prepare USB for IDLE**
1. DP pull-up enable
2. Deactivate USB when IDLE by writing 0x0005 to the USBIDLCTL register (USB reset = 1, USB IDLE = 1)

**Enable and Set the USB DPLL**
1. Set USB DPLL to generate 48-MHz clock
e.g., for a 12-MHz input clock, set to x4 Lock mode by writing 0x200 to USBDPLL register
2. Enable the USB DPLL by writing 0x0210 to USBDPLL register
3. Enable the USB peripheral by writing 0x0004 to USBIDLCTL register

**IDLE All Domains**
1. Idle EMIF, PERI, DMA, CLKGEN, CPU domains by writing 0x003F to ICR register
2. Wait 6 cycles
3. Execute IDLE command

**After 6 cycles, device is in full Idle and the internal oscillator is shut off. Core power consumption should now be in the microamperes. This is the maximum power saving state.**

**IDLE All Domains Except CPU and CLKGEN**
1. Idle EMIF, PERI, and DMA by writing 0x002E to ICR register
2. Wait 165 cycles
3. Execute IDLE command

**IDLE All Domains Except CPU and CLKGEN**
1. Idle EMIF, PERI, and DMA by writing 0x0004 to USBIDLCTL register

**Prepare to Disable Internal Oscillator**
1. Set CLKOUT and OSC disable bits by writing 0xC000 to EBSR register

**Prepare to Disable Internal Oscillator**
1. Set CLKOUT and OSC disable bits by writing 0xC000 to EBSR register

**Figure 4. Disabling the Internal Oscillator on the TMS320VC5509**
Prepare Interrupts for IDLE
1. Clear IFR0, IFR1 by writing 0xFFFF to them
2. Enable wake-up interrupt in IER1

Begin Oscillator Disable

Is USB present and enabled?

Yes, if using USB APLL

Switch to the USB DPLL
1. Switch from the USB APLL to the USB DPLL
See Using the USB APLL on the TMS320VC5509A application report (SPRA997) for this procedure

Yes, if using USB DPLL

Prepare USB for IDLE
1. DP pull-up enable
OR 0x0080 with the USBCTL register
2. Deactivate USB when IDLE by writing 0x0005 to the USBIDLCTL register (USB reset = 1, USB IDLE = 1)

Prepare to Disable Internal Oscillator
1. Set CLKOUT and OSC disable bits by writing 0xC000 to EBSR register

IDLE All Domains
1. Idle EMIF, PERI, DMA, CLKGEN, CPU domains by writing 0x003F to ICR register
2. Wait 6 cycles
3. Execute IDLE command

After 6 cycles, device is in full Idle and the internal oscillator is shut off. Core power consumption should now be in the microamperes. This is the maximum power saving state.

IDLE All Domains Except CPU and CLKGEN
1. Idle EMIF, PERI, and DMA by writing 0x002E to ICR register
2. Wait 165 cycles
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Enable and Set the USB DPLL
1. Set USB DPLL to generate 48-MHz clock
e.g., for a 12-MHz input clock, set to x4 Lock mode by writing 0x200 to USBDPLL register
2. Enable the USB DPLL by writing 0x0210 to USBDPLL register
3. Enable the USB peripheral by writing 0x0004 to USBIDLCTL register

No

Yes,

Evaluate and Set the USB DPLL
1. Set USB DPLL to generate 48-MHz clock
e.g., for a 12-MHz input clock, set to x4 Lock mode by writing 0x200 to USBDPLL register
2. Enable the USB DPLL by writing 0x0210 to USBDPLL register
3. Enable the USB peripheral by writing 0x0004 to USBIDLCTL register

Prepare to Disable Internal Oscillator
1. Set CLKOUT and OSC disable bits by writing 0xC000 to EBSR register

IDLE All Domains Except CPU and CLKGEN
1. Idle EMIF, PERI, and DMA by writing 0x002E to ICR register
2. Wait 165 cycles
3. Execute IDLE command

After 6 cycles, device is in full Idle and the internal oscillator is shut off. Core power consumption should now be in the microamperes. This is the maximum power saving state.

Figure 5. Disabling the Internal Oscillator on the TMS320VC5507/C5509A
3 Enabling the Internal Oscillator

The internal oscillator can be awakened from IDLE mode with any of the four events shown below:

- Hardware RESET
- USB resume/reset events
- Real-time clock (RTC) interrupt
- External interrupt

Please note that all external interrupts are automatically masked when powering up from an IDLE state. This is needed because it gives the oscillator time to stabilize when being powered up. The TMS320VC5503, TMS320VC5506, TMS320VC5507, TMS320VC5509, and TMS320VC5509A use the USB DPLL as the time keeper, to allow time for this to happen. Therefore, if USB DPLL is not set up correctly, external interrupts will not be re-activated after wake up.

After wake up, the INTM bit in the status register ST1, and the respective IER register bits for the various interrupts, should be set to enable the CPU to execute interrupt service routines.

Also, note that after wakeup only the CLKGEN and CPU domains are awakened. It is your responsibility to enable the other domains by clearing the IDLEEN bit and setting the ICR appropriately. Afterwards, you must use the IDLE command to execute these changes. The IDLE command is not pipeline protected, so extra cycles are required between the ICR assignment and the IDLE command (6 cycles are recommended). For more details on pipeline protection and operation, see the TMS320C55x DSP Programmer's Guide (SPRU376).

Any wake-up event must consider the oscillator stabilize time. Since typically, most oscillators take at least 100-200 ms to stabilize, any wake-up event must typically be asserted for 10 CPU clock cycles + oscillator stabilize time. Oscillator stabilize time can be obtained for the specific manufacturer's oscillator being used.

For each system, you must evaluate the oscillator stabilization time. This is an analog parameter that is affected by the board parasitics, crystal characteristics, temperature, and I/O supply voltage. Also, the ESR and the load capacitance (including parasitic capacitance) of the oscillator circuit influence the oscillator stability time. Lower DV_{DD} voltages require longer oscillator stabilization times, and lower CV_{DD} require longer PLL lock times.

You must wait for 1ms after the PLL lock bit is set before the PLL wrapper has locked onto the PLL clock and switches from the bypass clock to the new PLL clock. After the PLL lock bit is set, the PLL core has locked onto the oscillator clock, and will be outputting the PLL clock to the PLL wrapper. If you do not wait for the PLL wrapper to output the PLL clock to the rest of the chip, the CPU could potentially latch up if it is still running in bypass mode and trying to interface with faster devices.
Lock signal from the USB PLL is achieved
1. USB receives 48-MHz clock

48-MHz USB clock interrupts DSP
1. Clears DSP ICR register
2. Clears DSP CLKGEN
3. DSP PLL starts locking sequence
4. After PLL lock bit is set, wait for 1.0 ms
5. ISR starts
6. ISR makes response to USB host

System awakened

Figure 6. Waking Up the Internal Oscillator With a Hardware or USB Reset/Resume for the TMS320VC5509
An external or RTC interrupt is generated
The duration of which must be greater than the clock stabilize time + 1 CPU clock cycle

Interrupt reaches the DSP
1. Clears DSP ICR register
2. Wait 6 cycles
3. Clears DSP CLKGEN
4. DSP PLL starts locking sequence
5. After PLL lock bit is set, wait for 1.0 ms
6. ISR starts

Wake-up signals initiated
1. Reset/resume signal wakes up the internal oscillator
2. The USB PLL is enabled
3. The interrupt cannot access the DSP at this time; it is masked by the USB

USB PLL starts locking sequence
1. The USB PLL drives 1/2 the frequency of the CLKOUT before the lock
2. The lock signal from the USB PLL is asserted after the LOCK and the USB PLL starts to drive at x4 frequency from the USB cycle generator

System awakened

Figure 7. Waking Up the Internal Oscillator With an RTC or External Interrupt for the TMS320VC5506/C5507/C5509
Figure 8 and Figure 9 show each of the wake up procedures for TMS320VC5506/C5507/C5509/C5509A in detail.

**USB host asserts RESUME or hardware reset is asserted**

- The duration of which must be greater than the clock stabilize time + 1 CPU clock cycle

**Wake-up signals initiated**

1. Reset/resume signal wakes up the internal oscillator
2. The USB PLL is enabled

**USB PLL starts locking sequence**

1. The USB PLL drives 1/2 the frequency of the CLKOUT before the lock
2. The lock signal from the USB PLL is asserted after the LOCK and the USB PLL starts to drive at x4 frequency from the USB cycle generator

**Lock signal from the USB PLL is achieved**

1. USB receives 48-MHz clock

**48-MHz USB clock interrupts DSP**

1. Clears DSP ICR register
2. Clears DSP CLKGEN
3. DSP PLL starts locking sequence
4. After PLL lock bit is set, wait for 1.0 ms
5. ISR starts
6. ISR makes response to USB host

**System awakened**

**Switch back to the USB APLL if using the USB peripheral**

See *Using the USB APLL on the TMS320VC5506/C5507/C5509/C5509A* (SPRA997)

Figure 8. Waking Up the Internal Oscillator With a Hardware or USB Reset/Resume for the TMS320VC5506/C5507/C5509/C5509A
Interrupt reaches the DSP
1. Clears DSP ICR register
2. Clears DSP CLKGEN
3. DSP PLL starts locking sequence
4. After PLL lock bit is set, wait for 1.0 ms
5. ISR starts

An external or RTC interrupt is generated
The duration of which must be greater than the clock stabilize time + 1 CPU clock cycle

Wake-up signals initiated
1. Reset/resume signal wakes up the internal oscillator
2. The USB PLL is enabled
3. The interrupt cannot access the DSP at this time; it is masked by the USB

USB PLL starts locking sequence
1. The USB PLL drives 1/2 the frequency of the CLKOUT before the lock
2. The lock signal from the USB PLL is asserted after the LOCK and the USB PLL starts to drive at x4 frequency from the USB cycle generator

System awakened

Shut off the USB DPLL if it is not being used

See Using the USB APLL on the TMS320VC5506/C5507/C5509A (SPRA997)

Figure 9. Waking Up the Internal Oscillator With an RTC or External Interrupt for the TMS320VC5506/C5507/C5509A/C5509A

4 References
- Using the USB APLL on the TMS320VC5506/C5507/C5509A (SPRA997)
- TMS320C55x DSP Programmer's Guide (SPRU376)
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