EDRAM™ Memory Controller for the TMS320C31 DSP

Application Report

1998 Digital Signal Processor Solutions
EDRAM™ Memory Controller for the TMS320C31 DSP

Enhanced Memory Systems
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EDRAM™ Memory Controller for the TMS320C31 DSP

ABSTRACT
This report provides an overview of a controller chip set to improve processor memory management and transactions while using the Texas Instruments (TI™) TMS320C31 digital signal processor (DSP). This application uses a minimum number of wait states which increases processor throughput.
1 EDRAM Controller Design

This Enhanced DRAM controller design supports TMS320C31 DSP memory transactions with a minimum of wait states. This EDRAM controller is designed to support one EDRAM bank of 2M bytes; however, memory size can expanded by adding additional control outputs to the logic. Figure 1 shows a functional block diagram of the TMS320C31 DSP System. The TMS320C31 DSP primary-bus interface can be programmed to control wait states and hold operations. The memory-control register for the local bus is programmed with the following parameters:

- SWW is programmed to respond only to the external RDY input for wait states (SWW=00). The internal RDY wtcnt is ignored.
- WTCNT does not need to be programmed since software programmable wait states are not used.
- BNKCMP is set as shown below:

<table>
<thead>
<tr>
<th>EDRAM</th>
<th>MSBs Defining a Bank</th>
<th>Bank Size</th>
<th>BNKCMP</th>
</tr>
</thead>
<tbody>
<tr>
<td>512K x 8</td>
<td>23–8</td>
<td>256</td>
<td>10000</td>
</tr>
</tbody>
</table>

The TMS320C31 supports the following memory transactions:
- 32-bit page-read hit
- 32-bit page-read miss
- 32-bit write (hit or miss)

To support these bus transactions, the EDRAM controller must interface with the following processor control and address signals:
- A18–A0 – address bus
- STRB – external-access strobe
- R/W – read-write-mode outputs
- RDY – ready input
- RESET – reset input
- H1CLK – processor-clock output
- TCLK0 – timer zero output clock/pulse
EDRAM Controller Design

Figure 1. TMS320C31 System Block Diagram
The controller generates the following signals to control the EDRAM:

- **ROWSEL** – multiplexed row-address enable
- **COLSEL** – multiplexed column-address enable
- **RE** – row enable
- **CAL** – column-address strobe
- **WE** – write enable
- **WRG** – combined W/R and G
- **F** – refresh
- **S** – chip select

The EDRAM W/R and G control lines are tied together to form WRG. The ROWSEL, COLSEL, CAL, WE, WRG, and F logic signals are supplied from the 26V12 PLD.

S is an enable pin for the EDRAM and should be active for the desired page(s) of DSP memory. Because of the limited number of outputs of the PAL26V12, S is not included within the PAL. A simple decode might be to connect STRB to S where all external memory accesses enable the EDRAM, or in combination with an upper address line. Note that disabling the EDRAM will also lower the EDRAM power consumption. Optionally, the S input signal can be tied to ground if EDRAM power consumption is not an issue.
2 EDRAM Controller Functional Description

This section describes the EDRAM controller block diagram shown in Figure 2. The refresh counter is formed by using an internal timer in the TMS320C31 DSP to generate a refresh signal every 64 μs for the state machine. This refresh signal triggers an refresh on the next available bus cycle. Up to three wait states can be inserted for the processor while a bus transaction is occurring.

Figure 3, the address multiplexer, selects a row and a column address for the EDRAM multiplex address lines under control of the state machine. The multiplexer is implemented using the two 74FCT541CT 8-bit buffer chips. These chips were selected for their short throughput delay time (4.1 ns) and short select-delay time (5.8 ns), respectively. A column address is connected to pins A7–A0 for 512K x 8 EDRAM. The row address comprises the 11 local address bits above the column address. Address lines A10–A8 of the EDRAM are connected directly to A18–A16 of the TMS320C31 DSP. During column select times, the upper address lines are ignored so there is no need to feed these address lines through a buffer.

Figure 2. EDRAM Controller Block Diagram
Figure 3. Address Multiplexer Using Two 74FCT541CT Buffers

The state machine operates synchronously with the rising edge of H1CLK.

Figure 4. EDRAM Controller State Machine
The following memory-control sequences are selected, based on control-input-line status. Read and write sequences are described. All logic states are determined at the rising edge of H1CLK.

- **Reset Sequence** – When \text{RESET} is at logic 0, the processor is in the reset state. The EDRAM controller continuously executes \text{F} refresh cycles until \text{RESET} returns to logic 1 level. This meets the EDRAM initialization requirements of eight \text{F} refresh cycles during start up. It is assumed that a startup control program is run immediately following a reset. This program must configure the TMS320C31 to perform two read-miss cycles to different row addresses for each internal EDRAM bank. Row address bits A8 and A9 define the four internal EDRAM banks. This startup procedure must be performed for proper EDRAM operation.

- **Page-read-miss sequence** – Starting from the idle state, when \text{STRB} is at logic 0 and \text{R/W} is at logic 1, a page-read-miss sequence is executed. The row address is selected, and \text{WRG} signal is set to logic 0. The \text{RE} signal is then clocked to load a new page of memory into the internal DRAM cache column, which takes 30-ns. \text{RDY} is brought to logic 1 at the start of cycle R1 to insert a wait state for the processor. Data is available to the processor at the end of cycle two. Because of the TMS320C31 addressing system, one wait state is inserted when a read cycle follows a write cycle.

- **Page-read-hit sequence** – Starting from the R1 state, when \text{STRB} is at logic 0 and \text{R/W} is logic 1, a page-read-hit sequence is executed. The column address is selected, and \text{WRG} is brought to logic 0 to gate data onto the data bus. The EDRAM can support back-to-back page reads from cache in zero wait states. The TMS320C31 processor holds \text{STRB} at logic 0 during back-to-back page hit reads since the programmable bank switching feature is being used. On a page-read miss, \text{STRB} goes to logic 1, which also causes an idle state to be inserted.

- **Write sequence** – If \text{STRB} is at logic 0 and \text{R/W} is also at logic 0, a write sequence is executed. The row address is selected and write-data operation is stable and the \text{WE} signal is clocked to post the write data operation into an internal latch. When \text{CAL} falls, write data is written to the EDRAM array. Following the write-data operation, \text{RE} is brought to logic 1 to terminate the write-data cycle. The write operation is completed in two cycles or zero wait states. The EDRAM supports back-to-back writes in two cycles or zero wait states.
- Refresh sequence – If TCKL0 input is at logic 1, an F refresh sequence is performed after any current memory cycles are completed. The TCKL0 output is at logic 1 for 40 ns and it then goes to logic 0 and remains at logic 0 until the next refresh period. The F pin is brought to logic 0 and RE is clocked to perform an internal refresh using the internal-refresh counter. A refresh sequence is executed every 62-μs. During a refresh sequence, RDY is held at logic 1 to cause the processor to wait. The processor may need to wait for up to three wait states to complete the current memory transaction.

- Idle – If STRB is at logic 1 (except at the start of the W2 state), this indicates the cycle is an idle cycle. The WRG is brought to logic 1 to disable the EDRAM outputs from the data bus until the next active cycle.

- Chip select (S) – The S is generated using a NAND, NOR or equivalent gate to decode the Q2–Q0 state machine outputs. S is brought to logic 1 during the idle and refresh states to reduce power consumption. This circuit is optional and S can be tied to ground if reduced power consumption is not desired.

- Programming the TMS320C31 DSP Timer – The timer global-control register must be programmed immediately after power up so that the refresh counter can be initialized properly. The TCLK0 output is used to generate a 40-ns minimum high pulse every 62-μs. The bit values to be programmed are as follows:

  - CLKSRC = 1  \( f(\text{Timer clock}) \) 12.5MHz
  - FUNC = 1  \( \text{period register} \) = 780
  - C/P = 0  \( f(\text{INT}) \) 16KHz
  - I/O = 1
  - HLD = 1
  - INV = 0

  Period Register Value = 780d

The remaining bit fields can remain at their default values after power up. The interrupt-enable register does not need to be programmed to generate an interrupt when timer zero generates a high pulse every 62-μs. The timer must be started immediately after power up by setting the GO/HLD bits in the timer-global-control register to 11. When the counter value equals the value set in the period register, a 40-ns logic 1 pulse is output on TCLK0 pin. This logic 1 pulse causes the REF_PENDING register output-logic level to remain at logic 1 starting with the next rising edge of H1CLK. This level is cleared only after a refresh sequence is performed. The TMS320C31 DSP timer does not need to be restarted and no interrupt is generated. A refresh sequence is not started until after the second cycle of a read-miss or write sequence, if one is in progress.
Timing of the EDRAM controller is shown in Figure 5, Figure 6, and Figure 7. The EDRAM controller operates with a 50-MHz TMS320C31 DSP system using the 12-ns version of the EDRAM as shown. The EDRAM–controller parameters are for a 26V12-7 programmable logic device (PLD) and Pericom 74FCT541CT 8-bit buffers. The TMS320C31 DSP timing parameters are from the TMS320C31 DSP Data Manual (literature number SPRU031D).
3 Summary

An EDRAM controller for the 50 MHz and 60 MHz versions of the TI TMS320C31 DSP can be implemented using a simple PLD and two Pericom 74FCT541CT data buffers. The controller supports one EDRAM bank of 2M bytes (using DM2203 components) and can be expanded easily to include more memory. The EDRAM system as shown in this application report achieves zero wait states on read-hit cycles and on all write cycles.

System cost is reduced significantly by using an internal timer in the TMS320C31 to generate the refresh signals. The EDRAM achieves near 12 ns static RAM (SRAM) performance, while providing much lower memory cost at 4M-bit density. The EDRAM/TMS320C31 DSP provides an excellent ratio of cost/performance for DSP applications.

Example 1. PLD Equations

* TMS320C31 PLD Equations – 25 MHz Bus
* 26V12–7 PLD
* Revision 2.0
* Vantis MACH–XL 5.0 Compiler

INPUT H1CLK;
INPUT TCLK0;
LOW_TRUE INPUT RESET;
LOW_TRUE INPUT RW;
LOW_TRUE INPUT STRB;

LOW_TRUE OUTPUT RDY;
LOW_TRUE OUTPUT RE;
LOW_TRUE OUTPUT CAL;
LOW_TRUE OUTPUT WE;
LOW_TRUE OUTPUT WRG;
LOW_TRUE OUTPUT F;
LOW_TRUE OUTPUT ROWSEL;
LOW_TRUE OUTPUT COLSEL;

NODE q2..q0 CLOCKED_BY H1CLK;
D_FLOP NODE REF_PENDING CLOCKED_BY H1CLK;

MACRO ON 1;
MACRO OFF 0;

* Equations

* We need to store the current cycle state to generate EDRAM
* timings
STATE_MACHINE TMS320C31
  STATE_BITS [q2..q0]
  CLOCKED_BY H1CLK;
STATE IDLE:
REF_PENDING = OFF;
RDY = STRB * RW;
RE = OFF;
CAL = OFF;
WE = OFF;
WRG = OFF;
F = OFF;
ROWSEL = ON;
COLSEL = OFF;
IF (RESET) THEN
    GOTO REFRESH1;
ELSE
    IF (TCLK0) THEN
        GOTO REFRESH1;
    ELSE
        IF (STRB) THEN
            IF (RW) THEN
                GOTO WRITE1;
            ELSE
                GOTO READ1;
            END IF;
        END IF;
    END IF;
END IF;
STATE REFRESH1 :
REF_PENDING = OFF;
RDY = OFF;
RE = H1CLK;
CAL = OFF;
WE = OFF;
WRG = OFF;
F = ON;
ROWSEL = OFF;
COLSEL = OFF;
GOTO REFRESH2;
STATE REFRESH2 :
REF_PENDING = OFF;
RDY = OFF;
RE = H1CLK;
CAL = OFF;
WE = OFF;
WRG = OFF;
F = OFF;
ROWSEL = OFF;
COLSEL = OFF;
GOTO IDLE;
STATE READ1 :
  RDY = /H1CLK;
  RE = /H1CLK;
  CAL = OFF;
  WE = OFF;
  WRG = ON;
  F = OFF;
  ROWSEL = H1CLK;
  COLSEL = /H1CLK;
  REF_PENDING = TCLK0;
  GOTO READ2;

STATE READ2 :
  RDY = /H1CLK;
  RE = /H1CLK;
  CAL = OFF;
  WE = OFF;
  WRG = ON;
  F = OFF;
  ROWSEL = OFF;
  COLSEL = ON;
  REF_PENDING = TCLK0

IF (RESET) THEN
  GOTO IDLE
ELSE IF (TCLK0 + REF_PENDING) THEN
  GOTO REFRESH1;
ELSE IF (STRB * /RW) THEN
  GOTO READ2;
ELSE
  GOTO IDLE;
END IF;

STATE WRITE1 :
  RDY = OFF;
  RE = /H1CLK;
  CAL = OFF;
  WE = /H1CLK;
  WRG = OFF;
  F = OFF;
  ROWSEL = H1CLK;
  COLSEL = /H1CLK;
  REF_PENDING = TCLK0;
  GOTO WRITE2;

STATE WRITE2 :
  RDY = STRB * RW;
  RE = H1CLK;
  CAL = H1CLK;
  WE = H1CLK;
  WRG = OFF;
  F = OFF;
  ROWSEL = OFF;
  COLSEL = ON;
REF_PENDING = TCLK0;

IF (RESET) THEN
    GOTO IDLE;
ELSE IF (TCLK0 + REF_PENDING)
    THEN GOTO REFRESH1;
ELSE IF (/STRB * RW)
    THEN GOTO WRITE1;
ELSE IF (STRB * /RW)
    THEN GOTO READ1;
ELSE IF (/STRB * /RW)
    THEN GOTO IDLE;
ELSE GOTO IDLE;
END IF;
END TMS320C31;
Figure 5. TMS320C31 Read-Miss and Read-Hit Cycles @ 50 MHz
Table 1. TMS320C31 Read-Miss and Read-Hit Cycles @ 50 MHz

<table>
<thead>
<tr>
<th>NO.</th>
<th>NAME</th>
<th>FORMULA</th>
<th>MIN</th>
<th>MAX</th>
<th>MARGIN</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V tASR</td>
<td>5</td>
<td>5</td>
<td></td>
<td></td>
<td>Setup time, row address</td>
</tr>
<tr>
<td>2</td>
<td>V tRAH</td>
<td>1,5</td>
<td>1,5</td>
<td></td>
<td></td>
<td>Hold time, row address</td>
</tr>
<tr>
<td>3</td>
<td>C tRSU</td>
<td>6</td>
<td>5</td>
<td></td>
<td>&lt;8.&gt;</td>
<td>Setup time, RDY before H1 high</td>
</tr>
<tr>
<td>4</td>
<td>C tRH</td>
<td>0</td>
<td>6</td>
<td></td>
<td>&lt;4.&gt;</td>
<td>Hold time, RDY after H1 high</td>
</tr>
<tr>
<td>5</td>
<td>C tASR</td>
<td>5</td>
<td>5</td>
<td></td>
<td>&lt;7.&gt;</td>
<td>Setup time, row address</td>
</tr>
<tr>
<td>6</td>
<td>D tSTRB</td>
<td>4</td>
<td>4</td>
<td></td>
<td></td>
<td>Valid time, H1CLK to STRB</td>
</tr>
<tr>
<td>7</td>
<td>D tADDR</td>
<td>9</td>
<td>9</td>
<td></td>
<td>&lt;4.&gt;</td>
<td>Valid time, H1CLK to address</td>
</tr>
<tr>
<td>8</td>
<td>D tRWV</td>
<td>4</td>
<td>4</td>
<td></td>
<td>&lt;8.&gt;</td>
<td>Valid time, H1CLK to R/W</td>
</tr>
<tr>
<td>9</td>
<td>C tRE</td>
<td>30</td>
<td>30</td>
<td></td>
<td>&lt;8.&gt;</td>
<td>Active time, row enable</td>
</tr>
<tr>
<td>10</td>
<td>C tRAH</td>
<td>1</td>
<td>1</td>
<td></td>
<td>&lt;3.&gt;</td>
<td>Hold time, row enable</td>
</tr>
<tr>
<td>11</td>
<td>C tC</td>
<td>55</td>
<td>55</td>
<td></td>
<td>&lt;7.&gt;</td>
<td>Cycle time, row enable</td>
</tr>
<tr>
<td>12</td>
<td>D tAC</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td></td>
<td>Access time, column address</td>
</tr>
<tr>
<td>13</td>
<td>D tGQV</td>
<td>5</td>
<td></td>
<td>5</td>
<td></td>
<td>Access time, output enable</td>
</tr>
<tr>
<td>14</td>
<td>C tRP</td>
<td>20</td>
<td>20</td>
<td></td>
<td>&lt;2.&gt;</td>
<td>Precharge time, row</td>
</tr>
<tr>
<td>15</td>
<td>C tMSU</td>
<td>5</td>
<td>5</td>
<td></td>
<td>&lt;13.&gt;</td>
<td>Setup time, F and W/R mode select</td>
</tr>
<tr>
<td>16</td>
<td>D tCOBUF</td>
<td>6</td>
<td>6</td>
<td></td>
<td>&lt;6.&gt;&lt;5.</td>
<td>Delay time, clock to output</td>
</tr>
<tr>
<td>17</td>
<td>C tDSU</td>
<td>10</td>
<td>10</td>
<td></td>
<td>&lt;6.&gt;&lt;5.</td>
<td>Setup time, 'C31 data</td>
</tr>
<tr>
<td>18</td>
<td>C tDH</td>
<td>0</td>
<td>0</td>
<td></td>
<td>&lt;3.&gt;</td>
<td>Hold time, 'C31 data</td>
</tr>
<tr>
<td>19</td>
<td>D tPDBUF</td>
<td>4</td>
<td>4</td>
<td></td>
<td>&lt;3.&gt;&lt;3.</td>
<td>Delay time, propagation</td>
</tr>
<tr>
<td>20</td>
<td>D tCO</td>
<td>4,6</td>
<td>4</td>
<td>6</td>
<td></td>
<td>Delay time, clock to output</td>
</tr>
</tbody>
</table>
Figure 6. TMS320C31 Refresh After Idle Cycle @ 50 MHz
### Table 2. TMS320C31 Refresh After Idle Cycle @ 50 MHz

<table>
<thead>
<tr>
<th>NO.</th>
<th>NAME</th>
<th>FORMULA</th>
<th>MIN</th>
<th>MAX</th>
<th>MARGIN</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V tASR</td>
<td>5</td>
<td>5</td>
<td></td>
<td></td>
<td>Setup time, row address</td>
</tr>
<tr>
<td>2</td>
<td>V tRAH</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td>Hold time, row address</td>
</tr>
<tr>
<td>3</td>
<td>C tRSU</td>
<td>6</td>
<td>6</td>
<td></td>
<td>&lt;3.&gt;</td>
<td>Setup time, RDY before H1 high</td>
</tr>
<tr>
<td>4</td>
<td>C tRH</td>
<td>0</td>
<td>0</td>
<td></td>
<td>&lt;14.&gt;</td>
<td>Hold time, RDY after H1 high</td>
</tr>
<tr>
<td>5</td>
<td>C tRE</td>
<td>30</td>
<td>30</td>
<td></td>
<td>&lt;8.&gt;</td>
<td>Active time, row enable</td>
</tr>
<tr>
<td>6</td>
<td>C tCE</td>
<td>55</td>
<td>55</td>
<td></td>
<td>&lt;3.&gt;</td>
<td>Cycle time, row enable</td>
</tr>
<tr>
<td>7</td>
<td>C tMSU</td>
<td>5</td>
<td>5</td>
<td></td>
<td>&lt;13.&gt;</td>
<td>Setup time, F and W/R mode select</td>
</tr>
<tr>
<td>8</td>
<td>C tMH</td>
<td>5</td>
<td>5</td>
<td></td>
<td>&lt;13.&gt;</td>
<td>Hold time, F and W/R mode select</td>
</tr>
<tr>
<td>9</td>
<td>C tRP</td>
<td>20</td>
<td>20</td>
<td></td>
<td>&lt;-2.&gt;</td>
<td>Precharge time, row</td>
</tr>
<tr>
<td>10</td>
<td>D tCO</td>
<td>4,6</td>
<td>4</td>
<td>6</td>
<td></td>
<td>Delay time, clock to output</td>
</tr>
</tbody>
</table>
Figure 7. TMS320C31 Write Cycle – 50 MHz
### Table 3. TMS320C31 Write Cycle – 50 MHz

<table>
<thead>
<tr>
<th>NAME</th>
<th>FORMULA</th>
<th>MIN</th>
<th>MAX</th>
<th>MARGIN</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>C₁₅ₛᵤ</td>
<td>6</td>
<td>6</td>
<td>&lt;0.,1.&gt;</td>
<td>Setup time, RDY before H1 high</td>
</tr>
<tr>
<td>2</td>
<td>C₁₅ₐₚ</td>
<td>0</td>
<td>0</td>
<td>&lt;4.,8.&gt;</td>
<td>Hold time, RDY after H1 high</td>
</tr>
<tr>
<td>3</td>
<td>C₁₅ₛᵦᵢ</td>
<td>5</td>
<td>5</td>
<td>&lt;7.,7.&gt;</td>
<td>Setup time, row address</td>
</tr>
<tr>
<td>4</td>
<td>D₁ᵥₛₚₚ</td>
<td>2.4</td>
<td>2</td>
<td>4</td>
<td>Valid time, H1CLK to STRB</td>
</tr>
<tr>
<td>5</td>
<td>C₁₅ₑ</td>
<td>30</td>
<td>30</td>
<td>&lt;8.&gt;</td>
<td>Hold time, row address</td>
</tr>
<tr>
<td>6</td>
<td>C₁₅ₐₕ</td>
<td>1</td>
<td>1</td>
<td>&lt;1.,3.&gt;</td>
<td>Cycle time, row enable</td>
</tr>
<tr>
<td>7</td>
<td>C₁₅ₙ</td>
<td>55</td>
<td>55</td>
<td>&lt;23.&gt;</td>
<td>Cycle time, row enable</td>
</tr>
<tr>
<td>8</td>
<td>C₁₅ₛᵦᵢ</td>
<td>5</td>
<td>5</td>
<td>&lt;7.&gt;</td>
<td>Setup time, column address</td>
</tr>
<tr>
<td>9</td>
<td>C₁₅ₖ₃₁</td>
<td>0</td>
<td>0</td>
<td>&lt;12.,2.&gt;</td>
<td>Hold time, ‘C31 data</td>
</tr>
<tr>
<td>10</td>
<td>C₁₅ₛᵦᵢ</td>
<td>5</td>
<td>5</td>
<td>&lt;22.&gt;</td>
<td>Setup time, column address latch to row enable</td>
</tr>
<tr>
<td>11</td>
<td>D₁₅ₛᵦᵢ</td>
<td>2.7</td>
<td>2</td>
<td>7</td>
<td>Valid time, H1CLK to R/W</td>
</tr>
<tr>
<td>12</td>
<td>D₁₅ₛᵦᵢ</td>
<td>2.9</td>
<td>2</td>
<td>9</td>
<td>Valid time, H1CLK to address</td>
</tr>
<tr>
<td>13</td>
<td>D₁₅ₛᵦᵢ</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>Buffer output invalid</td>
</tr>
<tr>
<td>14</td>
<td>D₁₅ₛᵦᵢ</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>Delay time, clock to output</td>
</tr>
<tr>
<td>15</td>
<td>D₁₅ₛᵦᵢ</td>
<td>12</td>
<td>14</td>
<td>14</td>
<td>Valid time, ‘C31 data</td>
</tr>
<tr>
<td>16</td>
<td>C₁₅ₛᵦᵢ</td>
<td>20</td>
<td>20</td>
<td>&lt;18.&gt;</td>
<td>Precharge time, row</td>
</tr>
<tr>
<td>17</td>
<td>C₁₅ₛᵦᵢ</td>
<td>2</td>
<td>2</td>
<td>&lt;0.,0.&gt;</td>
<td>Setup time, CAL high to RE high</td>
</tr>
<tr>
<td>18</td>
<td>D₁₅ₛᵦᵢ</td>
<td>4.6</td>
<td>4</td>
<td>4</td>
<td>Delay time, clock to output</td>
</tr>
<tr>
<td>19</td>
<td>D₁₅ₛᵦᵢ</td>
<td>3.7</td>
<td>3</td>
<td>7</td>
<td>Delay time, propagation</td>
</tr>
<tr>
<td>20</td>
<td>C₁₅ₛᵦᵢ</td>
<td>5</td>
<td>5</td>
<td>&lt;25.,25.&gt;</td>
<td>Setup time, ‘C31 data</td>
</tr>
<tr>
<td>21</td>
<td>C₁₅ₛᵦᵢ</td>
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<td>0</td>
<td>&lt;16.,26.&gt;</td>
<td>Hold time, ‘C31 data</td>
</tr>
<tr>
<td>22</td>
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<td>0</td>
<td>&lt;44.&gt;</td>
<td>Hold time, column address</td>
</tr>
<tr>
<td>23</td>
<td>C₁₅ₛᵦᵢ</td>
<td>5</td>
<td>5</td>
<td>&lt;13.&gt;</td>
<td>Active time, column address latch</td>
</tr>
<tr>
<td>24</td>
<td>C₁₅ₛᵦᵢ</td>
<td>12</td>
<td>12</td>
<td>&lt;66.&gt;</td>
<td>Cycle time, column address latch</td>
</tr>
<tr>
<td>25</td>
<td>C₁₅ₛᵦᵢ</td>
<td>5</td>
<td>5</td>
<td>&lt;33.&gt;</td>
<td>Active time, write enable</td>
</tr>
<tr>
<td>26</td>
<td>C₁₅ₛᵦᵢ</td>
<td>12</td>
<td>12</td>
<td>&lt;66.&gt;</td>
<td>Cycle time, write enable</td>
</tr>
<tr>
<td>27</td>
<td>C₁₅ₛᵦᵢ</td>
<td>5</td>
<td>5</td>
<td>&lt;53.&gt;</td>
<td>Column address latch high time (latch transparent)</td>
</tr>
<tr>
<td>28</td>
<td>C₁₅ₛᵦᵢ</td>
<td>5</td>
<td>5</td>
<td>&lt;33.&gt;</td>
<td>Inactive time, write enable</td>
</tr>
<tr>
<td>29</td>
<td>C₁₅ₛᵦᵢ</td>
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<td>0</td>
<td>&lt;–2.&gt;</td>
<td>Column address latch high to write enable low</td>
</tr>
</tbody>
</table>