EVM Application #7

Measuring the Frequency of an Input Square Wave Using the TMS320F240 EVM

APPLICATION REPORT: SPRA416

David Figoli

Digital Signal Processing Solutions
January 1999

Texas Instruments
IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty, or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated
TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.
CONTACT INFORMATION

US TMS320 HOTLINE (281) 274-2320
US TMS320 FAX (281) 274-2324
US TMS320 BBS (281) 274-2323
US TMS320 email dsph@ti.com
Contents

Abstract ........................................................................................................................................ 7

Product Support.......................................................................................................................... 8
  World Wide Web .................................................................................................................. 8
  Email .................................................................................................................................... 8

Overview .................................................................................................................................. 9
  Modules Used ..................................................................................................................... 9
  Input .................................................................................................................................... 9
  Output .................................................................................................................................. 9

Background and Methodology ................................................................................................. 10
  PLL Module ......................................................................................................................... 10
  Digital I/O Ports ................................................................................................................... 10
  Event Manager .................................................................................................................... 11
Figures

Figure 1. Timing Diagram Demonstrating How Latency Affects Measured Frequency...... 14
EVM Application #7

Measuring the Frequency of an Input Square Wave Using the TMS320F240 EVM

Abstract

This EVM application measures the frequency of an input square wave using the capture input module in the Event Manager. The frequency is output to a variable that can be viewed in the debugger environment. This application is written in C2xx Assembly code. The algorithm described in this application report was implemented using the Texas Instruments (TI™) TMS320F240 Evaluation Module (EVM).

The specific topics discussed include:

- PLL module
- Digital I/O ports
- Event Manager
Product Support

World Wide Web

Our World Wide Web site at www.ti.com contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

Email

For technical issues or clarification on switching products, please send a detailed email to dsph@ti.com. Questions receive prompt attention and are usually answered within one business day.
Overview

This application measures the frequency of an input square wave using the capture input module in the Event Manager. The frequency is output to a variable that can be viewed in the debugger environment. This application is written in C2xx Assembly code. The algorithm described in this application report was implemented using the TI TMS320F240 EVM.

To view the results, the following commands need to be entered into the debugger environment when the program is loaded.

```
ba STOP
wa "FREQ, u
```

The measured frequency will appear in a watch window for the variable FREQ.

Modules Used

- Event Manager
- General Purpose Timer 2
- Capture Input 1

Input

CAP1/QEP1

Output

None
Background and Methodology

The initial setup of the program is similar to the previous capture application (CAP0.ASM). The PLL module, digital I/O ports, and the Event Manager need to be configured prior to capturing the input waveform.

This application makes use of the timer and the capture portion of the Event Manager module. The timer portion is used to determine the 1 second interval that the number of rising edges are to be captured in. The capture portion will determine when a rising edge on the input has occurred. Because the timer and the capture portion will be used to determine the frequency of the input square wave, this application will make use of two interrupt service routines. The interrupt priority for the timer is higher than the capture, which is what is desired; thus both interrupts can be unmasked at the same time.

We want the timer priority to be higher because when 1 second has elapsed, if the capture port had a higher priority, it would continue to count the number of rising edges. However, with the timers being higher in priority, the counting will have to stop because the core will service the higher priority interrupt.

PLL Module

The PLL module is set up as in Application #1 (PWM0.ASM). The frequency that the CPUCLK is setup to be is important in order to determine the period of the input square wave. The PLL divide by 2 is enabled and the multiplication ratio is set to 1; as a result, with a CLKIN (crystal oscillator) value of 10MHz, the CPUCLK is then 5MHz.

NOTE:
When changing the PLL settings, you must disable the PLL and then re-enable it so the new settings can take effect. If not, the PLL will retain the first settings it was set to when the system was powered on.

Digital I/O Ports

Similar to the PWM applications in which Output Control Register A (OCRA) has to be set so that the PWM signal can be output on the proper pins, Output Control Register B (OCRB) has to be set so that the pins that the capture inputs share with the I/O pins are configured as capture inputs.
Event Manager

Once the digital I/O port and the PLL module have been set, then the Event Manager module registers can be configured to capture the rising edges of an input square wave. Since only one input capture port will be used, only one GP timer in the Event Manager will be needed. In this application, the input will be placed into capture input 1. Since the number of rising edges is what is important in this application and not the actual timer value, it is not necessary to use GP timer 2 or 3. Instead, GP timer 1 can be used to dictate the 1 second interval.

This application uses two interrupt service routines. The capture port of the Event Manager is set to capture the rising edge of an input wave. Once a rising edge is captured, an interrupt is generated; the service routine of the capture register increments a counter. Each time a rising edge is captured, the counter is incremented until the timer portion of the Event Manager causes a period interrupt. A period interrupt is generated after 1 second has elapsed; once the period register of the timer module matches the timer, an interrupt is generated which causes the current value of the counter to be stored into a variable. Once the value is stored the counter is reset, control is returned back to the main line to await another interrupt. Several frequency counts are obtained and then averaged. The average of the measurements is stored into the variable FREQ. By creating a watch window and setting a break point at the end of the program, the frequency can be viewed once the program has ended.

The limitation of this application is the frequency of the input square wave. If the period of the input square wave exceeds one second, then the counter may not count any rising edges during the execution of the program. If the period of the signal is too short compared with the latency that the interrupt service routines are executed, then the frequency obtained will be lowered than the actual input frequency. For slow frequencies, if the frequency is lower than 1 Hertz, the results will be unreliable because each 1 second period may not contain a rising edge. For faster frequencies, the upper limit depends on the counter size and the ISR latency. If the ISR latency is considered (assuming an infinite counter), then the maximum measurable frequency will be 714kHz.
If the counter size is considered (assuming a negligible latency), then the maximum measurable frequency is 65.5kHz.

Ignoring counter size:

\[
\text{Maximum Frequency} = \frac{1}{28 \text{ cycles} \times 50\text{ns}} \approx 714,000\text{Hz}
\]

Ignoring ISR latency:

\[
\text{Maximum Frequency} = \text{16bit Counter} \approx 65,500\text{Hz}
\]

The smaller maximum frequency is the upper limit of this application. Because latency is an issue, the range of frequencies that this application can measure accurately is frequencies between 5Hz and 50kHz.

**Period Interrupt Service Routine**

- Event Manager interrupt: 1 cycle
- Flush Pipeline, Check Vector Table: 4 cycles
- Branch to ISR: 4 cycles

<table>
<thead>
<tr>
<th>Period_ISR</th>
<th>LDP  #0</th>
<th>2 cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LACC  COUNTS</td>
<td>1 cycle</td>
</tr>
<tr>
<td></td>
<td>SACL  *+,0,AR2</td>
<td>1 cycle</td>
</tr>
<tr>
<td></td>
<td>LACC  #0</td>
<td>1 cycle</td>
</tr>
<tr>
<td></td>
<td>SACL  COUNTS</td>
<td>1 cycle</td>
</tr>
<tr>
<td></td>
<td>LACC  *</td>
<td>1 cycle</td>
</tr>
<tr>
<td></td>
<td>SUB   #1</td>
<td>1 cycle</td>
</tr>
<tr>
<td></td>
<td>SACL  *+,0,AR1</td>
<td>1 cycle</td>
</tr>
<tr>
<td></td>
<td>BCND  LEAVE,EQ</td>
<td>2 cycles</td>
</tr>
<tr>
<td></td>
<td>LDP   #232</td>
<td>2 cycles</td>
</tr>
<tr>
<td></td>
<td>LACC  EVIVRA</td>
<td>1 cycle</td>
</tr>
<tr>
<td></td>
<td>CLRC  INTM</td>
<td>1 cycle</td>
</tr>
<tr>
<td></td>
<td>RET</td>
<td>4 cycles</td>
</tr>
</tbody>
</table>

28 cycles
Capture Port Interrupt Service Routine

Event manager interrupt 1 cycle
Flush Pipeline, Check Vector Table 4 cycles
Branch to ISR 4 cycles

```
CAP_ISR
LDP #0 2 cycles
LACC COUNTS 1 cycle
ADD #1 1 cycle
SACL COUNTS 1 cycle
LDP #232 2 cycles
LACC EVIVRC 1 cycle
CLRC INTM 1 cycle
RET 4 cycles
```

22 cycles

The period interrupt service routine is a constant delay that is always included, but the capture interrupt service routine is variable because it depends on the input signal. Thus, the faster the frequency of the input signal, the more the latency associated with the capture interrupt service routine is going to affect the measured frequency. The higher frequency will be measured at a lower frequency, which is somewhat analogous to under-sampling.
Figure 1. Timing Diagram Demonstrating How Latency Affects Measured Frequency
; *******************************************************************
; File Name: cap1.asm
; Originator: Digital control systems Apps group - Houston
; Target System: 'C24x Evaluation Board
;
; Description: Capture Input of the Event Manager Module is set up
to count the number of rising edges that
an input square wave has in a 1 second period
;
; To view the results in the debugger environment
enter the following commands before running the
program
    ba STOP
    wa *FREQ,,u
;
; The value in FREQ is the number of rising edges
that occur within a 1 second period.
;
; Last Updated: 12 June 1997
;
;*******************************************************************

.include f240regs.h

;----------------------------------------------------------------------
; Vector address declarations
;----------------------------------------------------------------------
.sect "vectors"

RSVECT    B    START ; Reset Vector
INT1      B    PHANTOM ; Interrupt Level 1
INT2      B    PERIOD_ISR ; Interrupt Level 2
INT3      B    PHANTOM ; Interrupt Level 3
INT4      B    CAP_ISR ; Interrupt Level 4
INT5      B    PHANTOM ; Interrupt Level 5
INT6      B    PHANTOM ; Interrupt Level 6
RESERVED  B    PHANTOM ; Reserved
SW_INT8   B    PHANTOM ; User S/W Interrupt
SW_INT9   B    PHANTOM ; User S/W Interrupt
SW_INT10  B    PHANTOM ; User S/W Interrupt
SW_INT11  B    PHANTOM ; User S/W Interrupt
SW_INT12  B    PHANTOM ; User S/W Interrupt
SW_INT13  B    PHANTOM ; User S/W Interrupt
SW_INT14  B    PHANTOM ; User S/W Interrupt
SW_INT15  B    PHANTOM ; User S/W Interrupt
SW_INT16  B    PHANTOM ; User S/W Interrupt
TRAP      B    PHANTOM ; Trap vector
NMINT     B    PHANTOM ; Non-maskable Interrupt
EMU_TRAP  B    PHANTOM ; Emulator Trap
SW_INT20  B    PHANTOM ; User S/W Interrupt
SW_INT21  B    PHANTOM ; User S/W Interrupt
SW_INT22  B    PHANTOM ; User S/W Interrupt
SW_INT23  B    PHANTOM ; User S/W Interrupt
;===================================================================
; MAIN CODE - starts here
;===================================================================
.text
NOP
START:
SETC INTM    ;Disable interrupts
SPLK #000Ah,IMR ;Mask all core interrupts
               ;except INT4 and INT2
LACC IFR     ;Read Interrupt flags
SACL IFR     ;Clear all interrupt flags
CLRC SXM     ;Clear Sign Extension Mode
CLRC OVM     ;Reset Overflow Mode
CLRC CNF     ;Config Block B0 to Data mem

; Set up PLL Module
LDP   #00E0h

;The following line is necessary if a previous program set the PLL
;to a different setting from the settings which the application
;uses. By disabling the PLL, the CKCR1 register can be modified so
;that the PLL can run at the new settings when it is re-enabled.

SPLK #0000000001000001b,CKCR0
 ; CLKMD=PLL; Disable, SYSCLK=CPUCLK/2

;  5432109876543210
SPLK #0000000101110000b,CKCR1
 ; CKIN(OSC)=10MHz, CPUCLK=5MHz

;CKCR1 - Clock Control Register 1
;
;  Bits 7-4   (1011)CKINF(3)-CKINF(0) - Crystal or Clock-In
;          Frequency
;          Frequency = 10MHz
;  Bit 3     (1)  PLLDIV(2) - PLL divide by 2 bit
;          Divide PLL input by 2
;  Bits 2-0   (000) PLLFB(2)-PLLFB(0) - PLL multiplication ratio
;          PLL Multiplication Ratio = 1
;
;  5432109876543210
SPLK #0000000110000001b,CKCR0
 ; CLKMD=PLL Enable, SYSCLK=CPUCLK/2

;CKCR0 - Clock Control Register 0
;
;  Bits 7-6   (11)  CLKMD(1),CLKMD(0) - Operational mode of Clock
;          Module
;  PLL Enabled; Run on CKIN on exiting low power mode
;  Bits 5-4   (00)  PLLOCK(1),PLLOCK(0) - PLL Status. READ ONLY

Measuring the Frequency of an Input Square Wave Using the TMS320F240 EVM
Bits 3-2 (00) PLLPM(1),PLLPM(0) - Low Power Mode
; LPM0
; Bit 1 (0) ACLKENA - 1MHz ACLK Enable
; ACLK Disabled
; Bit 0 (1) PLLPS - System Clock Prescale Value
; \( f(\text{sysclk}) = \frac{f(\text{cpuclk})}{2} \)

SPLK #0100000011000000b, SYSCR ; CLKOUT=CPUCLK

; SYSCR - System Control Register
; Bit 15-14 (01) RESET1,RESET0 - Software Reset Bits
; No Action
; Bits 13-8 (000000) Reserved
; Bit 7-6 (11) CLKSRC1,CLKSRC0 - CLKOUT-Pin Source Select
; CPUCLK: CPU clock output mode
; Bit 5-0 (000000) Reserved

SPLK #006Fh, WDCR ; Disable WD if VCCP=5V (JP6 in pos. 2-3)
KICK_DOG ; Reset Watchdog

-----------------------------------
Set up Digital I/O Port
-----------------------------------
LDP #225 ; DP=225, Data Page to Configure OCRx
SPLK #0011100000000000b, OCRA

; OCRA - Output Control Register A
; Bit 15 (0) CRA.15 - IOPB7
; Bit 14 (0) CRA.14 - IOPB6
; Bit 13 (1) CRA.13 - T3PWM/T3CMP
; Bit 12 (1) CRA.12 - T2PWM/T2CMP
; Bit 11 (1) CRA.11 - T1PWM/T1CMP
; Bit 10 (0) CRA.10 - IOPB2
; Bit 9 (0) CRA.9 - IOPB1
; Bit 8 (0) CRA.8 - IOPB0
; Bits 7-4 (0000) Reserved
; Bit 3 (0) CRA.3 - IOPA3
; Bit 2 (0) CRA.2 - IOPA2
; Bit 1 (0) CRA.1 - IOPA1
; Bit 0 (0) CRA.0 - IOPA0

76543210
SPLK #11110000b, OCRB

; OCRB - Output Control Register B
; Bit 7 (1) CRB.7 - CAP4
; Bit 6 (1) CRB.6 - CAP3
; Bit 5 (1) CRB.5 - CAP2/QEP2
; Bit 4 (1) CRB.4 - CAP1/QEP1
; Bit 3 (0) CRB.3 - BIO
LDP #232 ;DP=232 Data Page for the Event Manager
SPLK #0000h, GPTCON ;Clear General Purpose Timer Control
SPLK #0000h, T1CON ;Clear GP Timer 1 Control
SPLK #0000h, T2CON ;Clear GP Timer 2 Control
SPLK #0000h, T3CON ;Clear GP Timer 3 Control
SPLK #0000h, COMCON ;Clear Compare Control
SPLK #0000h, ACTR ;Clear Full Compare Action Control
; SPLK #0000h, ACTR ;Clear Full Compare Action Control
; SPLK #0000h, SACTR ;Clear Simple Compare Action Control
; SPLK #0000h, DBTCON ;Clear Dead-Band Timer Control
; SPLK #0000h, DBTCON ;Clear Dead-Band Timer Control
SPLK #0000h, CAPCON ;Clear Capture Control
SPLK #0FFFFh, EVIFRA ;Clear Interrupt Flag Register A
SPLK #0FFFFh, EVIFRB ;Clear Interrupt Flag Register B
SPLK #0FFFFh, EVIFRC ;Clear Interrupt Flag Register C
SPLK #0000h, EVIMRA ;Clear Event Manager Mask Register A
SPLK #0000h, EVIMRB ;Clear Event Manager Mask Register B
SPLK #0000h, EVIMRC ;Clear Event Manager Mask Register C

---

T1COMPARE .set 4C4Bh ; T1Compare Initialized to 0
T1PERIOD .set 9897h ; T1Period Initialized to 1Hz value

.text
LDP #232 ;DP=232, Data Page for Event Manager Addresses
```assembly
SPLK #T1COMPARE,T1CMPR;T1CMPR = T1PERIOD/2

; 2109876543210
SPLK #0000001010101b,GPTCON

;GPTCON - GP Timer Control Register
;   Bit 15  (0) T3STAT - GP Timer 3 Status.  READ ONLY
;   Bit 14  (0) T2STAT - GP Timer 2 Status.  READ ONLY
;   Bit 13  (0) T1STAT - GP Timer 1 Status.  READ ONLY
;   Bits 12-11  (00) T3TOADC - ADC start by event of GP Timer 3
;                    No event starts ADC
;   Bits 10-9  (00) T2TOADC - ADC start by event of GP Timer 2
;                    No event starts ADC
;   Bits 8-7  (00) T1TOADC - ADC start by event of GP Timer 1
;                    No event starts ADC
;   Bit 6   (1) TCOMPOE - Compare output enable
;            Enable all three GP timer compare outputs
;   Bits 5-4 (01) T3PIN - Polarity of GP Timer 3 compare output
;                  Active Low
;   Bits 3-2 (01) T2PIN - Polarity of GP Timer 2 compare output
;                  Active Low
;   Bits 1-0 (01) T1PIN - Polarity of GP Timer 1 compare output
;                  Active Low

SPLK #T1PERIOD,T1PR ; T1PR = 9897h
SPLK #0000001010101b,GPTCON

;T1CON - GP Timer 1 Control Register
;   Bits 15-14  (00) FREE,SOFT - Emulation Control Bits
;                   Stop immediately on emulation suspend
;   Bits 13-11  (010) TMODE2-TMODE0 - Count Mode Selection
;                   Continuous-Up Count Mode
;   Bits 10-8  (111) TPS2-TPS0 - Input Clock Prescaler
;                   Divide by 128
;   Bit 7   (0) Reserved
;   Bit 6   (0) TENABLE - Timer Enable
;            Disable timer operations
;   Bits 5-4 (00) TCLKS1,TCLKS0 - Clock Source Select
;                   Internal Clock Source
;   Bits 3-2 (01) TCLD1,TCLD0 - Timer Compare Register Reload
;                   Condition
;                   When counter is 0 or equals period
;                   register value
;   Bit 1   (1) TECMPR - Timer compare enable
;            Enable timer compare operation
```

Measuring the Frequency of an Input Square Wave Using the TMS320F240 EVM
; Bit 0 (0) Reserved
;
5432109876543210
SPLK #0000000000000000b,T2CON ;GP Timer 2-Not Used

;T2CON - GP Timer 2 Control Register
; Bits 15-14 (00) FREE,SOFT - Emulation Control Bits
; Stop immediately on emulation suspend
; Bits 13-11 (000) TMODE2-TMODE0 - Count Mode Selection
; Stop/Hold
; Bits 10-8 (000) TPS2-TPS0 - Input Clock Prescaler
; Divide by 1
; Bit 7 (0) TSWT1 - GP Timer 1 timer enable bit
; Use own TENABLE bit
; Bit 6 (0) TENABLE - Timer Enable
; Disable timer operations
; Bits 5-4 (00) TCLKS1,TCLKS0 - Clock Source Select
; Internal Clock Source
; Bits 3-2 (00) TCLD1,TCLD0 - Timer Compare Register
; Reload Condition
; When counter is 0
; Bit 1 (0) TECMPR - Timer compare enable
; Disable timer compare operation
; Bit 0 (0) SELT1PR - Period Register select
; Use own period register
;
5432109876543210
SPLK #0000000000000000b,T3CON ;GP Timer 3-Not Used

;T3CON - GP Timer 3 Control Register
; Bits 15-14 (00) FREE,SOFT - Emulation Control Bits
; Stop immediately on emulation suspend
; Bits 13-11 (000) TMODE2-TMODE0 - Count Mode Selection
; Stop/Hold
; Bits 10-8 (000) TPS2-TPS0 - Input Clock Prescaler
; Divide by 1
; Bit 7 (0) TSWT1 - GP Timer 1 timer enable bit
; Use own TENABLE bit
; Bit 6 (0) TENABLE - Timer Enable
; Disable timer operations
; Bits 5-4 (00) TCLKS1,TCLKS0 - Clock Source Select
; Internal
; Bits 3-2 (00) TCLD1,TCLD0 - Timer Compare Register
; Reload Condition
; When counter is 0
; Bit 1 (0) TECMPR - Timer compare enable
; Disable timer compare operation
; Bit 0 (0) SELT1PR - Period Register select
; Use own period register
;
5432109876543210
SPLK #1011110001010101b,CAPCON
;CAPCON - Capture Control Register
; Bit 15  (0)  CAPRES - Capture Reset
;         Clear all registers of capture units and
;         QEP circuits to 0
; Bits 14-13 (01) CAPQEPN - Capture Units 1 & 2 and QEP Circuit
;        Enable Capture Units 1 & 2. Disable QEP Circuit
; Bit 12  (1)  CAP3EN - Capture Unit 3 Control
;         Enable Capture Unit 3
; Bit 11  (1)  CAP4EN - Capture Unit 4 Control
;         Enable Capture Unit 4
; Bit 10  (1)  CAP34TSEL - GP Timer Selection for Capture
; Units 3 & 4
;        Select GP Timer 3
; Bit 9   (0)  CAP12TSEL - GP Timer Selection for Capture
; Units 1 & 2
;        Select GP Timer 2
; Bit 8   (0)  CAP4TOADC - Capture Unit 4 starts ADC
;         No Action
; Bits 7-6 (01) CAP1EDGE - Edge Detection for Capture Unit 1
;        Detect Rising Edge
; Bits 5-4 (01) CAP2EDGE - Edge Detection for Capture Unit 2
;        Detect Rising Edge
; Bits 3-2 (01) CAP3EDGE - Edge Detection for Capture Unit 3
;        Detect Rising Edge
; Bits 0-1 (01) CAP4EDGE - Edge Detection for Capture Unit 4
;        Detect Rising Edge
;
; 876543210
SPLK #011111111b,CAPFIFO

;CAPFIFO - Capture FIFO Status Register
; Bits 15-14  CAP4FIFO Status - READ ONLY
; Bits 13-12  CAP3FIFO Status - READ ONLY
; Bits 11-10  CAP2FIFO Status - READ ONLY
; Bits 9-8    CAP1FIFO Status - READ ONLY
; Bit 7 (1)   CAPFIFO15 - CAP4FIFO bit 15 Clear
;            Clear Bit 15 of CAPFIFO
; Bit 6 (1)   CAPFIFO14 - CAP4FIFO bit 14 Clear
;            Clear Bit 14 of CAPFIFO
; Bit 5 (1)   CAPFIFO13 - CAP3FIFO bit 13 Clear
;            Clear Bit 13 of CAPFIFO
; Bit 4 (1)   CAPFIFO12 - CAP3FIFO bit 12 Clear
;            Clear Bit 12 of CAPFIFO
; Bit 3 (1)   CAPFIFO11 - CAP2FIFO bit 11 Clear
;            Clear Bit 11 of CAPFIFO
; Bit 2 (1)   CAPFIFO10 - CAP2FIFO bit 10 Clear
;            Clear Bit 10 of CAPFIFO
; Bit 1 (1)   CAPFIFO9 - CAP1FIFO bit 9 Clear
;            Clear Bit 9 of CAPFIFO
; Bit 0 (1)   CAPFIFO8 - CAP1FIFO bit 8 Clear
Clear Bit 8 of CAPFIFO

SPLK #00010000000b, EVIMRA

EVIMRA - EV Interrupt Mask Register A

Bits 15-11 Reserved

Bit 10 (0) T1OFINT ENABLE - Timer 1 Overflow Interrupt

   Enable

   Disabled

Bit 9 (0) T1UFINT ENABLE - Timer 1 Underflow Interrupt

   Enable

   Disabled

Bit 8 (0) T1CINT ENABLE - Timer 1 Compare Interrupt Enable

   Disabled

Bit 7 (1) T1PINT ENABLE - Timer 1 Period Interrupt Enable

   Enabled

Bit 6 (0) SCMP3INT ENABLE - Simple Compare Unit 3 Comp Int

   Enable

   Disabled

Bit 5 (0) SCMP2INT ENABLE - Simple Compare Unit 2 Comp Int

   Enable

   Disabled

Bit 4 (0) SCMP1INT ENABLE - Simple Compare Unit 1 Comp Int

   Enable

   Disabled

Bit 3 (0) CMP3INT ENABLE - Full Compare Unit 3 Comp Int

   Enable

   Disabled

Bit 2 (0) CMP2INT ENABLE - Full Compare Unit 2 Comp Int

   Enable

   Disabled

Bit 1 (0) CMP1INT ENABLE - Full Compare Unit 1 Comp Int

   Enable

   Disabled

Bit 0 (1) PDPINT ENABLE - Power Drive Protection Interrupt

   Enable

   Disabled

SPLK #0001b, EVIMRC

EVIMRC - EV Interrupt Mask Register C

Bits 15-4 Reserved

Bit 3 (0) CAP4INT Enable

   Disable

Bit 2 (0) CAP3INT Enable

   Disable

Bit 1 (0) CAP2INT Enable

   Disable

Bit 0 (1) CAP1INT Enable
Measuring the Frequency of an Input Square Wave Using the TMS320F240 EVM

; Enable

; VARIABLES FOR CAP_ISR

.bss VALUE1,1 ; 1st timer value for 1st period interrupt
.bss VALUE2,1 ; 2nd timer value for 2nd period interrupt
.bss VALUE3,1 ; 3rd timer value for 3rd period interrupt
.bss VALUE4,1 ; 4th timer value for 4th period interrupt
.bss VALUE5,1 ; 5th timer value for 5th period interrupt
.bss COUNTER,1 ; Counter to acquire 5 values
.bss FREQ,1 ; Frequency to count the number of rising edges
.bss COUNTS,1 ; Counts the number of rising edges in 1 second

.text

LAR AR1,#VALUE1 ; AR1 = address of VALUE1
LAR AR2,#COUNTER ; AR2 = address of COUNTER
LDP #0
SPLK #0000h,VALUE1 ; Initialize VALUE1
SPLK #0000h,VALUE2 ; Initialize VALUE2
SPLK #0000h,VALUE3 ; Initialize VALUE3
SPLK #0000h,VALUE4 ; Initialize VALUE4
SPLK #0000h,VALUE5 ; Initialize VALUE5
SPLK #0005h,COUNTER; Counter set to acquire 5 values
SPLK #0000h,FREQ ; Initialize FREQ
SPLK #0000h,COUNTS ; Initialize COUNTS
LDP #232
LACC EVIFRC ; ACC = Interrupt Flags of EVIFRC
SACL EVIFRC ; EVIFRC = ACC => clears all flags
LDP #0
LACC IFR ; ACC = Interrupt Flags of IFR
SACL IFR ; IFR = ACC => clears all flags
LDP #232
SBIT1 T1CON,B6_MSK ; Sets Bit 6 of T1CON
; TxCON - GP Timer x Control Register
;   Bit 6 (1) TENABLE - Timer Enable
;       Enable Timer Operations

MAR *,AR1 ; ARP = AR1
CLRC INTM ; Enable Interrupts

WAIT B WAIT ; Wait for an interrupt

;-------------------------------------------------------------------
; PERIOD INTERRUPT SERVICE ROUTINE
;-------------------------------------------------------------------

PERIOD_ISR
LDP #0 ; DP = 0 for addresses 0000h - 007Fh
LACC COUNTS ; ACC = Counts
SACL *,0,AR2 ; VALUEx = value of GP Timer from CAP1FIFO, ARP = AR2

LACC #0 ; ACC = 0
SACL COUNTS ; Clear the Counts

LACC * ; ACC = COUNTER
SUB #1 ; Decrement Counter
SACL *,0,AR1 ; Store new value of Counter, APR = AR1
BCND LEAVE,EQ ; If captured all values stop else restart

LDP #232 ; DP = 232 for address 7400h - 747Fh
LACC EVIVRA ; Reading Vector Register Clears Interrupt Flags
CLRC INTM ; Enable Interrupts
RET ; Return to program

LEAVE
LDP #0 ; DP = 0, Data Page for the acquired values
LACC VALUE2 ; ACC = VALUE2
ADD VALUE3 ; ACC = VALUE2 + VALUE3
ADD VALUE4 ; ACC = VALUE2 + VALUE3 + VALUE4
ADD VALUE5 ; ACC = VALUE2 + VALUE3 + VALUE4 + VALUE5

SFR ; Shift ACC right = Divide by 2
SFR ; Shift ACC right = Divide by 2
SACL FREQ ; Store value into AVERAGE

STOP B STOP ; End the Program

;-------------------------------------------------------------------
; CAPTURE INTERRUPT SERVICE ROUTINE

Measuring the Frequency of an Input Square Wave Using the TMS320F240 EVM
Measuring the Frequency of an Input Square Wave Using the TMS320F240 EVM

;-------------------------------------------------------------------
; CAP_ISR
LDP #0 ;DP = 0 for addresses 0000h - 007Fh
LACC COUNTS ;ACC = COUNTS
ADD #1 ;ACC = COUNTS + 1; Increment Counts
SACL COUNTS ;COUNTS = ACC; Store new value

LDP #232 ;DP = 232 for addresses 7400h - 747Fh
LACC EVIVRC ;Reading Vector Register clears
; Interrupt Flags
CLRC INTM ;Enable Interrupts
RET ;Return from interrupt

;-------------------------------------------------------------------
; ISR - PHANTOM
;
; Description: Dummy ISR, used to trap spurious interrupts.
;
; Modifies: Nothing
;
; Last Update: 16 June 95
;-------------------------------------------------------------------
PHANTOM KICK_DOG ;Resets WD counter
B PHANTOM