Using Boundary Scan on the TMS320VC5441

Yi Luo
Clay Turner

VOP Platform

ABSTRACT

The TMS320VC5441 DSP (hereafter referred to as VC5441) is a quad-core processor implementing standard IEEE 1149.1 boundary scan capability. This application report contains a description of the VC5441 boundary scan implementation and information about how to use it with other boundary scan tools and devices.

The material covered in this application report assumes the reader is familiar with the boundary scan concepts defined by IEEE Standard 1149.1. An overview of these concepts is presented in the IEEE Std 1149.1 (JTAG) Testability Primer (literature number SSYA002). For detailed information on the operation and requirements for boundary scan, refer to the IEEE standard itself. Copies of the standard are available from IEEE at 1-800-678-IEEE.

Contents

1 VC5441 Boundary Scan Implementation .................................................. 1
  1.1 VC5441 Silicon Revision Requirements ............................................. 1
  1.2 Full Observe and Control Capability ................................................. 2
  1.3 VC5441 Hardware Requirements for Boundary Scan Test ....................... 2
  1.4 VC5441 Boundary Scan Pin Coverage .............................................. 2
  1.5 VC5441 Boundary Scan Description Language (BSDL) Implementation .......... 3
  1.6 VC5441 Boundary Scan Instruction Implementation ............................. 5

List of Figures

Figure 1. Initialization for Boundary Scan Test Mode Using TRST, EMU0 and EMU1/OFF .... 2
Figure 2. Boundary Scan Structure of the VC5441 ........................................ 3
Figure 3. The VC5441 Subsystems Modeled as a “Module” in the Scan Chain ............. 5

List of Tables

Table 1. Device Pins Not Testable Through Boundary Scan ............................ 2
Table 2. Pins Captured by Each VC5441 Subsystem During Boundary Scan Test ........ 4

1 VC5441 Boundary Scan Implementation

1.1 VC5441 Silicon Revision Requirements

The VC5441 boundary scan implementation described in this document applies to all silicon revisions.
1.2 Full Observe and Control Capability

VC5441 implements standard observe and control capability with respect to the IEEE Standard 1149.1. This means all pins with input functions (input or I/O pins) have observe capability and all pins with output functions (outputs and I/O pins) have control capability.

1.3 VC5441 Hardware Requirements for Boundary Scan Test

Boundary scan test requires control of the five test access port signals (TMS, TCK, TDI, TDO and TRST) as described in IEEE standard 1149.1. Two additional signals, EMU0 and EMU1/OFF, are used by TI DSPs to provide emulation debug capability through the JTAG test access port. Also, TI uses these signals for scan-based factory tests.

During boundary scan tests, EMU0 and EMU1/OFF must be held high while TRST is transitioned from low to high. This operation sets the correct internal test mode for boundary scan test to be performed. EMU0 and EMU1/OFF should be pulled high through a 4.7k ohm pull-up resistor on each pin. The pull-up resistors are connected to the DVDD power supply for the VC5441.

Boundary scan ATPG tools should be configured to cycle TRST prior to beginning boundary scan tests to ensure that the device is in the proper test mode.

```
<table>
<thead>
<tr>
<th>Pin</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVDD, CVDD, VSS, AVDD, VSSA</td>
<td>Power supply pins</td>
</tr>
<tr>
<td>TEST</td>
<td>Factory test pins</td>
</tr>
<tr>
<td>TMS, TCK, TDI, TDO, TRST</td>
<td>JTAG test access pins</td>
</tr>
<tr>
<td>EMU0, EMU1/OFF</td>
<td>Emulation test pins</td>
</tr>
</tbody>
</table>
```

Figure 1. Initialization for Boundary Scan Test Mode Using TRST, EMU0 and EMU1/OFF

1.4 VC5441 Boundary Scan Pin Coverage

All digital pins (112 pins) on the VC5441 have boundary scan cells for test with the following exceptions. The device pins not testable through boundary scan are shown below in Table 1.
1.5 VC5441 Boundary Scan Description Language (BSDL) Implementation

A representation of the internal structure of the VC5441 with respect to boundary scan is shown in Figure 2. The VC5441 is composed of four internal processors called subsystems. Each subsystem has its own independent TAP controller to provide boundary scan test and emulation capability. The device signals TMS, TCK and TRST are connected to each subsystem in parallel.

Figure 2. Boundary Scan Structure of the VC5441

The device TDI is connected to subsystem A.

The internal equivalent of TDO for subsystem A is connected to the internal TDI for subsystem B. The output of the chain from subsystem B is connected to the internal TDI for subsystem C.

The output of the chain from subsystem C is connected to the internal TDI for subsystem D.

The output of the chain from subsystem D is connected to the device TDO.

To a boundary scan test system, this structure is equivalent to treating the subsystems as independent devices.

The four subsystems have the ability to capture unique groups of pins on the device. Subsystem A captures 67 pins which include the pins associated uniquely with subsystem A and some of the device pins that are common to four subsystems. Subsystem B captures only the 13 device pins associated with subsystem B. Subsystem C captures 19 pins that include the pins associated uniquely with subsystem C and some of the device pins that are common to four subsystems. Subsystem D captures only the 13 device pins associated with subsystem D. The pins captured by each subsystem are listed in Table 2.
### Table 2. Pins Captured by Each VC5441 Subsystem During Boundary Scan Test

<table>
<thead>
<tr>
<th>Subsystem</th>
<th>Pins</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>HA[0:18]</td>
<td>HPI Address Bus</td>
</tr>
<tr>
<td></td>
<td>HD[0:15]</td>
<td>HPI Data Bus</td>
</tr>
<tr>
<td></td>
<td>HCS, HAS, HMODE, HDS1, HDS2, HR/W, HRDY, HPI_SEL1, HPI_SEL2</td>
<td>HPI-16 Signals</td>
</tr>
<tr>
<td></td>
<td>RESET</td>
<td>Device Reset Signal</td>
</tr>
<tr>
<td></td>
<td>CLKMD, CLKIN, CLKOUT</td>
<td>Clock Signals</td>
</tr>
<tr>
<td></td>
<td>BDR2, BCLKR2, BCLKX2, BFSR2, BFSX2, BDX2</td>
<td>McBSP2 Signals</td>
</tr>
<tr>
<td></td>
<td>A_BDR0, A_BCLKR0, A_BCLKX0, A_BFSR0, A_BFSX0, A_BDX0</td>
<td>A_McBSP0 Signals</td>
</tr>
<tr>
<td></td>
<td>A_GPIO[0:3]</td>
<td>A General Purpose I/O Signals</td>
</tr>
<tr>
<td></td>
<td>A_RS, A_NMI, A_INT</td>
<td>A Reset Interrupt Signals</td>
</tr>
<tr>
<td>B</td>
<td>B_BDR0, B_BCLKR0, B_BCLKX0, B_BFSR0, B_BFSX0, B_BDX0</td>
<td>B_McBSP0 Signals</td>
</tr>
<tr>
<td></td>
<td>B_GPIO[0:3]</td>
<td>B General Purpose I/O Signals</td>
</tr>
<tr>
<td></td>
<td>B_RS, B_NMI, B_INT</td>
<td>B Reset Interrupt Signals</td>
</tr>
<tr>
<td>C</td>
<td>C_BDR0, C_BCLKR0, C_BCLKX0, C_BFSR0, C_BFSX0, C_BDX0</td>
<td>McBSP1 Signals</td>
</tr>
<tr>
<td></td>
<td>C_GPIO[0:3]</td>
<td>C General Purpose I/O Signals</td>
</tr>
<tr>
<td></td>
<td>C_RS, C_NMI, C_INT</td>
<td>C Reset Interrupt Signals</td>
</tr>
<tr>
<td>D</td>
<td>D_BDR0, D_BCLKR0, D_BCLKX0, D_BFSR0, D_BFSX0, D_BDX0</td>
<td>D_McBSP0 Signals</td>
</tr>
<tr>
<td></td>
<td>D_GPIO[0:3]</td>
<td>D General Purpose I/O Signals</td>
</tr>
<tr>
<td></td>
<td>D_RS, D_NMI, D_INT</td>
<td>D Reset Interrupt Signals</td>
</tr>
</tbody>
</table>

Although ATPG tools vary in how they describe system level structure, all tools provide a method to describe the order of the devices in the scan chain. The BSDL description of the VC5441 is implemented as 4 BSDL files, one for each subsystem. These four boundary scan objects must always be grouped and described to the ATPG tools in the proper order. Subsystem D must be described as the subsystem closer to TDO, then subsystem C, subsystem B follows, and the last is subsystem A. If the order is reversed, tests generated by the ATPG tools will be incorrect.
Since the connection between the scan chains of the four subsystems is internal to the device, some ATPG tools may issue a warning or error indicating that the TDO–TDI connection between the two subsystem objects is not present. In this case, the device can be modeled as a multi-chip module using the hierarchical capabilities of the ATPG tool. Many boundary scan systems have hierarchical scan chain descriptions where, for example, a plug-in module may be described as a sub-chain to the main boundary scan chain. The model for the sub-chain is generated separately, and then referenced in the description of the main boundary scan chain. The same approach can be used to model the VC5441 as a single object if necessary. The device can be modeled as a sub-chain composed of subsystem A, subsystem B, subsystem C, and subsystem D, shown in Figure 3. Then, the VC5441 can be referenced in the main description of the scan chain as a single device “module”. Since the methods to describe hierarchical and modular systems are tool dependent, a single method cannot be described here. It will be necessary to contact the ATPG tool vendor regarding how this procedure is done on their tool. Given the BSDL files for each subsystem and the information in this document, a model can be generated.

Separate BSDL files are provided for subsystem A, B, C, and D. Current VC5441 BSDL files and information are available on the web at:

http://www.ti.com/sc/docs/tools/dsp/ftp/c54x.htm

1.6 VC5441 Boundary Scan Instruction Implementation

The VC5441 implements the following instructions for boundary scan:

- SAMPLE/PRELOAD
- EXTEST
- BYPASS
- HIGHZ
IEEE standard 1149.1 specifies that the SAMPLE/PRELOAD instruction samples inputs and preloads but does not drive outputs. During the SAMPLE/PRELOAD instruction, the device pins maintain their normal functional behavior. The behavior of the VC5441 during execution of this instruction is consistent with the specification in the standard.

IEEE standard 1149.1 specifies that the EXTEST instruction samples inputs, and loads and drives outputs. During the EXTEST instruction, all device pins function as boundary scan inputs or outputs depending on their function. The behavior of the VC5441 during execution of this instruction is consistent with the specification in the standard.

IEEE standard 1149.1 specifies that the BYPASS instruction maps a one-bit bypass register between TDI and TDO (to minimize the chain length when a device is not being tested) and the device pins operate in their normal functional (non-test) mode. The behavior of the VC5441 during execution of this instruction is consistent with the specification in the standard. Note that the VC5441 has one bypass bit for each subsystem (since there is a TAP controller for each subsystem) for a total of four bits between the device TDI and TDO. This behavior is accounted for (and maintains compliance with IEEE standard 1149.1) through the use of separate BSDL files for each subsystem.

IEEE standard 1149.1 specifies that the HIGHZ instruction places the bypass register in the scan chain and causes all output pins (either dedicated outputs or I/O pins) to enter a high-impedance state. The behavior of the VC5441 during execution of this instruction is consistent with the specification in the standard.

None of the other boundary scan instructions specified as optional in IEEE standard 1149.1 are implemented on the VC5441.
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI’s standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2002, Texas Instruments Incorporated