Application Report
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TMS320C672x Power Consumption Summary

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ABSTRACT

This document discusses the power consumption of the Texas Instruments TMS320C672x digital signal processor (DSP). Power consumption on TMS320C67x™ devices is highly application-dependent. A spreadsheet is provided to model power consumption for the user's application. To get good results from the spreadsheet, realistic usage parameters must be entered. The low-core voltage and other power design optimizations allow these DSPs to operate with industry-leading performance, while maintaining a low power-to-performance ratio.

The data presented in this document and in the accompanying spreadsheet was measured from units at the maximum end of power consumption for production units; no production units will have average power consumption that exceeds the spreadsheet values. Thus, the spreadsheet values may be used for board thermal analysis and power supply design as a maximum long-term average. All power measurements were taken from silicon revision 1.0 units of the TMS320C672x.

This application report contains a spreadsheet that can be downloaded from this link: http://www.ti.com/lit/zip/spraaa4.

Table 1. Typical Activity

			Power Per Frequency (mW/MHz) (1)	Power at Frequency (W) (2)		
Device	**Core Voltage**	**CPU Frequency**	**CPU**	**Internal Logic**	**IO**	**Total**
C6727-GDH	1.2 V	300 MHz	1.0	0.789	0.251	1.041
C6726-RFP C6722-RFP	1.2 V	250 MHz	1.0	0.666	0.190	0.857
C6720-RFP	1.2 V	200 MHz	1.0	0.559	0.190	0.750

(1) Assumes 60% CPU utilization.

(2) Assumes the following conditions: 60% CPU utilization; EMIF at 50% utilization (100 MHz), 50% writes, (32-bits for GDH, 16-bits for RFP), 50% bit switching, two 10-MHz SPI at 100% utilization, 50% bit switching.

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1 Typical Activity 1

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1 Activity-Based Models

TMS320C672x power consumption can vary widely depending on the use of on-chip resources. Thus, power consumption cannot be estimated accurately without an understanding of the components of the DSP in use and the usage patterns for those components. By providing the usage parameters that describe how and what on the DSP is being used, accurate consumption numbers can be obtained for power-supply and thermal analysis.

This model breaks down power consumption into two major components: baseline power and activity power. Using this model, different applications that use the DSP differently can get accurate predictions, all across the spectrum of possible power consumption on C672x.

1.1 Baseline Power

Baseline consumption is power that is consumed that is not dependent on chip activity. This includes things like static power, PLL power, clock tree power, etc. While independent of activity, baseline power is dependent on the device operating frequency, voltage, and temperature. Thus, the user can affect baseline power only by changing the device operating frequency (through the CPU frequency), the applied voltage, or the operating temperature.

1.2 Activity Power

Activity consumption is power that is consumed by active parts of the DSP (the CPU, dMAX, peripherals, etc.). Activity power is independent of temperature, but dependent on voltage and activity levels. Activity power is separated by the major modules of the device, so that their contribution can be measured independently of each other. This helps with tailoring power consumption to specific applications. The parameters used to determine the activity level of a module are frequency, utilization, read/write balance, bus size, and switching probability. Module activity power includes necessary dMAX service for peripherals that require it. Note that not all parameters apply to all modules.

- *Frequency* is the operating frequency of a module or the frequency of external interface to that module.
- *% Utilization* is the relative amount of time the module is active or in use versus off or idled.
- *% Write* is the relative amount of time (considering active time only) the module is sending data out of the DSP versus reading data into the DSP. The exception to this rule is the UHPI, where % Write is the relative amount of time (considering active time only) the external host is writing data into the DSP.
- *Bits* is the number of data bits being used in a selectable-width interface.
- *% Switch* is the probability that any one data bit will change state from one cycle to the next.

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1.3 Modules

The C672x power estimation spreadsheet contains the following modules with adjustable parameters:

- CPU
- EMIF
- UHPI
- SPI0
- SPI1
- McASP0
- McASP1
- McASP2
- I2C0
- I2C1

dMAX is not listed as a separate module because the module activity models include necessary dMAX service. For available peripherals and peripheral configuration, please refer to the device-specific data manual.

2 Using the Power Estimation Spreadsheet

Using the power estimation spreadsheet involves simply entering appropriate usage parameters. Cells that are designed for user input are white in color. To use the spreadsheet, simply:

- Enter the case temperature for which you want to estimate power
- Choose the desired C672x device: C6727, C6727B, C6726, C6726B, C6722, C6722B, or C6720
- Fill in the appropriate module use parameters

  The spreadsheet will take the provided information and display the details of power consumption for that configuration.

  As the spreadsheet is being configured, the settings will be checked for conflicts, e.g. peripheral clock frequency out of allowed range, etc. For best results, the information should be entered from left to right starting at the top and moving downward.

2.1 Choosing Appropriate Values

The frequency and bits user values are determined by design and it will be clear what the correct values to enter are. Peripherals that are completely unused should use 0 for frequency. The utilization, read/write balance, and bit switching require estimation and a good understanding of the user application to choose appropriate values.

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2.1.1 Utilization

For modules except CPU, utilization is simply the percentage of time the module spends doing something useful, versus being unused or idle. For these peripherals, there are not various degrees of use, so the value is just an average over time. For example, if the EMIF performs reads and writes one-quarter of the time and has no data to move for the other three-quarters of the time (though it continues to perform background tasks like refresh), this would be 25% utilization.

For peripherals with IO, utilization can be estimated by comparing used bandwidth with theoretical maximum bandwidth. If, for example, an application must transfer 160 Kb/s via the I2C port using the Fast Mode, with a theoretical 400 Kb/s maximum, the I2C port utilization would be about 40%.

The CPU utilization is not as straightforward, because there are varying degrees of use for the CPU. Here, 0% utilization means the CPU is idle and does no useful work, where 100% utilization means all 8 functional units are active every cycle and the maximum amount of data is brought in from internal RAM every cycle. Few DSP algorithms will achieve 100% utilization, because this requires everything to be used every cycle, with no stalls. Even DSP-intense applications do not spend all of the time in such highly parallel loops. Time is typically also spent executing control code or less demanding DSP algorithms. These types of code may execute only a few instructions in parallel and significantly reduce the IO of the CPU, and thus reduce overall utilization. Thus the balance of CPU use for the application must be considered, and entering 100% utilization is not practical for real applications.

For example, an application that executes control code (estimated at 25% of CPU capability) half of the time, and very dense DSP code (estimated at 90% of CPU capability) the other half, would have an average utilization of about 60% (25% x 50% + 90% x 50%). If the balance were changed to 25% control code and 75% DSP code, the weighted average would be about 75% utilization (25% x 25% + 90% x 75%). If the 25%/75% ratio is kept, but the DSP code does not fully use all the CPU resources (estimate now at 75% of CPU capability) then the overall utilization returns to about 60% (25% x 25% + 75% x 75%). Using estimates of intensity and duration of blocks of code in the application, an estimate of the overall CPU utilization can be obtained.

System level issues may also reduce utilization. Though the spreadsheet will accept 100% utilization for all peripherals, this is not possible in reality. As memory and dMAX bandwidth is consumed, peripheral activity is throttled back due to these bottlenecks and therefore 100% utilization is not achieved. In applications with a lot of memory and/or dMAX usage, individual module utilization numbers should be entered keeping this overall limitation in mind.

2.1.2 % Writes

Peripherals that move data out of the DSP as much as they move data into the DSP have 50% writes (the spreadsheet will assume the remaining 50% of the time is spent on reads). In some applications, peripherals move data in only one direction, or have a known balance of data movement. In these cases, % writes should be changed to 0%, 100%, or the known ratio as appropriate for the cases when the DSP is reading all the time, writing all the time, or a combination of the two, respectively. Otherwise, 50% is a typical number that should be used.

2.1.3 % Switching

Random data has a 50% chance any bit will change from one cycle to the next. Some applications may be able to predict this chance using some a priori information about the data set. If there is a property of the algorithm that allows prediction of the bit changes, the application-specific probability can be used. All other applications should use the default number of 50%.

2.2 Graphs

The graphs page in the spreadsheet contains graphs that provide a visual breakdown of power consumption. Shown is a comparison of active power (based on the parameters supplied) and pie charts showing the relative contributions of each module to the core and IO power consumption.

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3 Using the Results

The results presented by the spreadsheet are based on measured data for revision 1.0 silicon of the C672x. The measured units were selected to be at the maximum end of power consumption for production units; no production units will have average power consumption that exceeds the spreadsheet values. The spreadsheet data may therefore be considered maximum average power consumption. That is, transient currents may cause power to spike above the spreadsheet value for a small amount of time, but over a long period of time, the observed average consumption will be below the spreadsheet value. Thus, the spreadsheet value may be used for board thermal analysis and power supply design as a maximum long-term average.

3.1 Adjusting IO Power Results

IO power is dependent not only on the DSP and activity, but also the load being driven. For loads with CMOS inputs, the power required to drive the trace dominates, and is a better measure of load than the number of inputs or lumped load capacitance. For the data presented in the spreadsheet, the EMIF (with serial termination), SPI, and I2C interfaces were loaded with approximately 1.5 inches of 50 ohm trace. The UHPI and McASPs were loaded with approximately 3.5 inches of 50 ohm trace, with no termination. If the target system has very different IO loading, the spreadsheet results may be scaled either up or down to compensate. For this reason, the spreadsheet allows the user to specify the approximate load on the IO pins for each module. This parameter is used to adjust the reported IO power numbers.

4 Example

Here is an example demonstrating how to choose appropriate values for a particular application. The values used in this example may be imported into the spreadsheet by clicking the appropriate macro button.

4.1 Sample Application

In this example, the DSP is transmitting 192 KHz stereo audio data through one McASP in I2S mode using four serializers (32-bit slots). A particular algorithm is run approximately 40% of the time to process the data. The rest of the time the processor is performing non-optimized background tasks. The device is communicating with a microcontroller through the I2C at a rate of 350 Kb/s. Furthermore, the application requires external buffer reads at 5.25 MB/s and writes at 10 MB/s via the EMIF. The DSP is running at 1.2 V, 300 MHz CPU, at 60°C. The EMIF is running at 100 MHz, with a 16-bit bus.

In the spreadsheet, there is a button named Sample Application that will configure these values outlined here.`

- Case Temperature: 60C
- CPU: 200 MHz, 35% utilization
  - CPU utilization is based on the following factors:
    - Optimized DSP algorithm: 75% of CPU capability for 40% of the time.
    - Background: 10% of CPU capability for 40% of the time
- EMIF: 100 MHz, 10% utilization, 55% writes, 16 bits, 50% switching
  - EMIF utilization is based on the following factors:
    - External Buffer Writes: 10 Mbytes/sec
    - External Buffer Reads: 8.5 Mbytes/sec
    - Total: 18.5 Mbytes/sec , 10 Mbytes/sec of which are writes
- SPI0: 2 MHz, 100% utilization, 50% switching
- SPI1: 2 MHz, 100% utilization, 50% switching
- McASP0: 12.3 MHz bit clock rate (192 kHz frame sync rate in I2S mode yields 6.14 MHz bit frequency), 100% utilization, 50% switching, 4 serializers
- I2C0: 350Kb/s, 100% utilization, 50% switching
- All other modules are not being used (0% utilization).

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Entering these values into the spreadsheet gives a maximum power consumption of about 535 mW for core and 143 mW for IO, for a total of 678 mW.

5 References

1. *TMS320C6727, TMS320C6726, TMS320C6722 Floating-Point Digital Signal Processors* (SPRS268)
2. *TMS320C6727B, TMS320C6726B, TMS320C6722B, TMS320C6720 Floating-Point Digital Signal Processors* (SPRS370)
3. *TMS320C6727, TMS320C6727B, TMS320C6726, TMS320C6726B, TMS320C6722, TMS320C6722B, TMS320C6720 Digital Signal Processors Silicon Errata* (SPRZ232)

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