Application Report
SPRAAC6B–May 2006

Implementing DDR2 PCB Layout on the TMS320DM4xx DMSoc

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ABSTRACT

This document contains implementation instructions for the DDR2 interface contained on the TMS320DM4xx Digital Media System-on-Chip (DMSoC) device. The approach to specifying interface timing for the DDR2 interface is quite different than on previous devices.

The previous approach specified device timing in terms of data sheet specifications and simulation models. The customer was required to obtain compatible memory devices, as well as their data sheets and simulation models. The customer would then take this information and design their printed circuit board (PCB) using high speed simulation to close system timing.

For the DM4xx DDR2 interface, the approach is to specify compatible DDR2 devices and provide the PCB routing rule solution directly to the customer. TI has performed the simulation and system design work to ensure DDR2 interface timings are met. This document describes the required routing rules.

The DM4xx EVM provides an example of a PCB layout following these routing rules that passes FCC EMI requirements. The customer may copy the DDR2 portion of this layout directly, but the intent is to allow enough flexibility in the routing rules to meet other PCB requirements.

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1 Prerequisites

1.1 High Speed Design

While the goal of this document is to make system implementation easier for the customer by providing the system solution, it is still expected that the PCB design work be supervised by a knowledgeable high speed PCB designer as an assumption is made that the PCB designer is using established high speed design rules. Ground plane cuts should be avoided if at all possible as they are tricky to do correctly. Crosstalk and EMI impacts due to PCB design should be evaluated as the PCB design progresses as it can be difficult to go back and fix issues later. Thorough planning will aid in the design cycle.

1.2 Familiarity with the JEDEC DDR2 Specification

The DDR2 interface on the DM4xx device is designed to be compatible with the JEDEC JESD-79A DDR2 specification. It is assumed that the reader is familiar with this specification and the basic electrical operation of the interface. In addition, several memory manufacturers provide detailed application notes on DDR2 operation.

2 DM4xx DDR2 Supported Devices

The DM4xx DDR2 interface supports JEDEC DDR2 x16 devices. Supported densities are 256Mb, 512Mb, and 1Gb in the x16 device width. Any JEDEC DDR2-400 speed grade device at these densities in the x16 width will work with DM4xx's DDR2 controller at DDR2 clock supported in the DM4xx data sheet. The DM4xx does not utilize the differential DQS feature of the DDR2 memories, all DQS signals are single ended.

TI is working with specific DDR2 manufacturers/devices. The following JEDEC DDR2 compatible devices are recommended:

MT47H64M16BT-5E – Micron 1Gb DDR2-400 92 ball package

MT47H32M16BT-5E – Micron 512Mb DDR2-400 92 ball package

MT47H32M16CC-5E – Micron 512Mb DDR2-400 84 ball package

MT47H16M16BG-5E – Micron 256Mb DDR2-400 84 ball package

EDE5116ABSE-4A-E – Elpida 512Mb DDR2-400 84 ball package

EDE5116AFSE-4A-E – Elpida 512Mb DDR2-400 84 ball package

EDE2516ABSE-4A-E – Elpida 256Mb DDR2-400 84 ball package

2.1 JEDEC DDR2 84 Versus 92 Ball Packages

The 84 and 92 ball DDR2 BGA packages are electrically compatible. The additional 8 balls on the 92 ball package are support balls only. The provided DDR2 layout provides room for these support balls.

2.2 DDR2 Package Size Warning

Use caution when determining the DDR2 component keep out as the JEDEC specification generally calls out only maximums for package sizing. Some manufacturers' JEDEC compliant DDR2 parts are narrower than these maximums and this can cause assembly interference issues if the part is later changed to another manufacturer with a wider package width. It is best to follow MO-207J and the manufacturer's documentation to determine overall package sizing. Pay close attention to the limits allowed by MO-207J, as these will likely be more restrictive than a specific manufacturer's part specification. This will allow physical placement compatibility with all JEDEC DDR2 parts supported by this device

3 Other Documentation

The Flip Chip Ball Grid Array Package Reference Guide (SPRU811) provides guidance with respect to PCB design and Texas Instruments BGA packages. It contains PCB design rules, PCB assembly parameters, rework process, thermal management, troubleshooting tips plus other critical information.

JEDEC specification JEDSD-79A contains the JEDEC DDR2 specification. JEDEC specification MO-207J contains package drawings for JEDEC DDR2 devices.

For additional general information on high-speed board design, the interested reader is referred to the *High Speed DSP Systems Design Guide* (SPRU889).

4 Schematics and Electrical Connections

Figure 1 shows a high level schematic of the DDR2 interface. Specific pin numbers can be obtained from the DM4xx and JEDEC DDR2 data sheets. The 32 bit DDR2 interface of DM4xx is connected to two 16 bit DDR2 devices, thus the clock, address, and control connections are three point nets and the data lines are point to point nets.

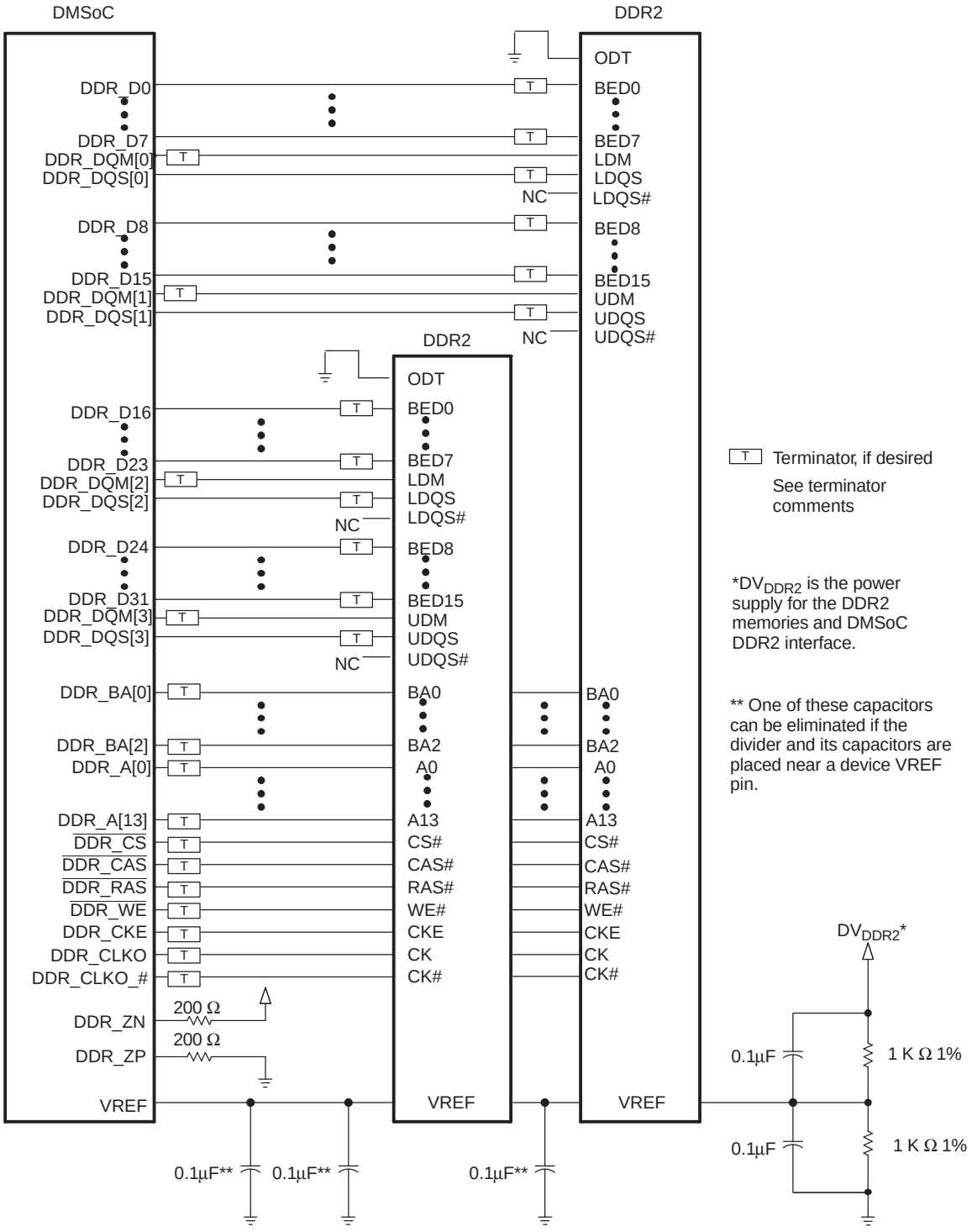


Figure 1. DM4xx DDR2 High Level Schematic

4.1 Differences Between the DM4xx DDR2 Interface and the Typical PC Application

There are some subtle differences between the embedded DDR2 application used on DM4xx and the typical PC motherboard/DDR2 DIMM application. The DM4xx DDR2 interface does not use stub series termination (the SST in SSTL). Stub series terminators are parallel terminators and they are not used in this case due to their high power consumption. Consequently, the termination voltage, V*tt*, is also not used nor is it required for the DM4xx DDR2 interface. The terminators shown in Figure 1 are series resistor terminators.

4.2 DDR2 Power Supplies

The nominal power supply for the DDR2 interface is 1.8V. This power supply is used for the DM4xx DDR2 power pins (DV_{DDR2}) as well as the JEDEC DDR2 devices. VREF is derived from the DDR2 power supply via a resistive divider. Bypassing for the 1.8V and VREF supplies are covered in this document.

4.3 Signal Terminations

The DM4xx DDR2 interface does not require terminations to meet overshoot requirements provided the DDR2 memories are operated at 60% strength. This means all the DDR2 signals will meet their input overshoot and ring back requirements without serial termination. Parallel termination is not supported by the DDR2 interface on the DM4xx. The example EVM PCB layout meets EMI requirements with its termination scheme. The no termination approach for new designs is not without risk, however.

Terminations on the PCB will allow the DDR2 signals to be tuned to meet EMI certification requirements. A PCB which fails EMI certification without terminations will likely have to be re-spun in order to address the EMI shortcomings. It can take multiple PCB spins to correct EMI issues. Note that re-spinning a dense non-terminated PCB layout to include terminators can be a very difficult effort because physical room must be made for the terminations. This means an entire PCB design may have to be redone. It is much easier to remove terminations rather than adding them after the PCB has been found to fail EMI.

Customers who are sensitive to the cost/schedule issues with respect to EMI may wish to include terminations on their boards even though they plan not to have terminations on the final product. This way, the terminations can easily be replaced with zero ohm resistors and checked for EMI compliance. If the PCB fails EMI, it is then straightforward to install the necessary terminations without re-spinning the PCB. Once the termination scheme has been verified to pass EMI, the remaining zero ohm terminations can be carefully removed from the PCB layout in a single PCB design spin.

5 Stackup

The minimum stackup required for routing DM4xx is a 6 layer stack as shown in Table 1. Additional layers may be added to the PCB stack up to accommodate other circuitry or to reduce the size of the DM4xx/DDR2 PCB footprint.

Table 1. Minimum PCB Stackup

Layer	Type	Description
1	Signal	Top Routing Mostly Horizontal
2	Plane	Ground
3	Plane	Power
4	Signal	Internal Routing
5	Plane	Ground
6	Signal	Bottom Routing Mostly Vertical

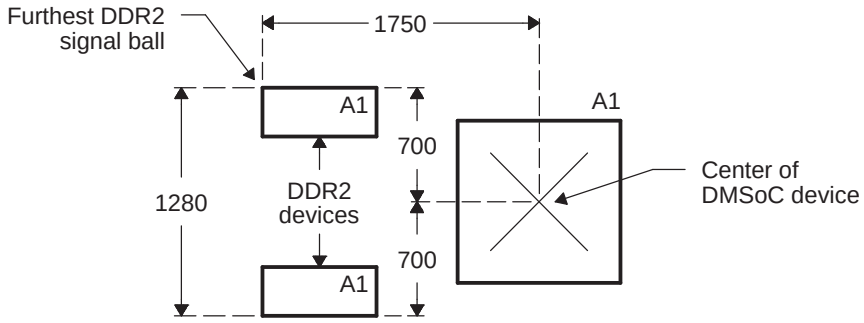
Single ended controlled impedance with a nominal value between 50 and 75 ohms is acceptable for the DDR2 interface. DDR2 impedance should be controlled to within 10 ohms. The CK net class should have a differential impedance twice the single ended impedance of the DDR2 interface. For example if the PCB is nominally 50 ohms, the differential impedance of CK should be 100 ohms.

5.1 Ground Reference Planes

It is critical that all signal routing layers have a *ground reference plane*, meaning that there is a full, contiguous ground plane next to every DDR2 routing layer. Two routing layers can share a ground plane (one signal layer above, and one signal layer below the ground plane). Ground plane cuts are not allowed in the DDR2 region (Ground plane cuts are generally a bad idea, and should only be done very carefully, only if absolutely necessary on other areas of the PCB). The purpose of the ground plane is to provide a path for return currents to minimize crosstalk and EMI. Power planes cannot be used as signal returns for the DDR2 interface. *Improper ground plane stackup will likely cause the DDR2 interface to fail or operate unreliably.*

6 Placement

Figure 2 shows the required placement of the DM4xx device as well as the DDR2 devices. The distances shown are maximums and there are no restrictions on how close the devices can be to each other. Generally, closer is better both from a cost and signal integrity point of view, but the tightness of the layout will be limited by the room required by the signal traces. Note that minimum placement is usually limited by the number of vias required to route the design, not the traces themselves. The PCB designer needs to take the routing requirements into consideration while determining placement.



Maximum placement distances from center of DMSoC package to furthest DDR2 signal ball.
Does not include distances to possible DDR2 NC outrigger balls. All dimensions in mils.

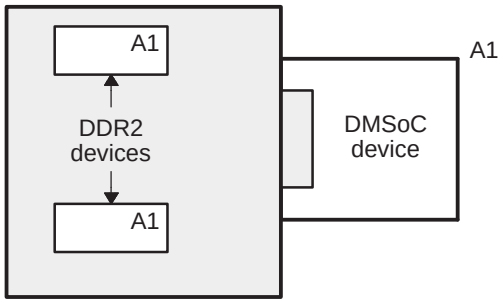
Figure 2. DM4xx and DDR2 Device Placement Specification

6.1 Minimizing PCB Area

The maximum placement and minimum PCB stackup uses the lowest cost PCB technology and generally results in the lowest unit cost PCB at the penalty of the largest footprint for the DDR2 interface. Customers need to evaluate the cost/benefit tradeoffs of smaller feature sizes and additional signal layers for their systems. Note that the minimum feature size and stackup may be limited by other circuitry on the PCB.

6.2 DDR2 Keep-Out Region

Figure 3 shows an example DDR2 keep-out region. This keep-out region will vary with the individual design. Its purpose is to ensure other signals do not interfere with the DDR2 interface. The only signals allowed in region on the DDR2 signal layers are those for this interface. The 1.8V power partial plane should encompass at least the entire DDR2 keep-out region.



Example DDR2 keep−out region. Region should encompass all DDR2 circuitry and will vary depending on placement. Non−DDR2 signals shall not be routed on the DDR2 signal layers within the DDR2 keep−out region. Non−DDR2 signals may be routed in this region provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks shall be allowed in the reference ground layers in this region. In addition the 1.8V power plane should cover the entire keep−out region.

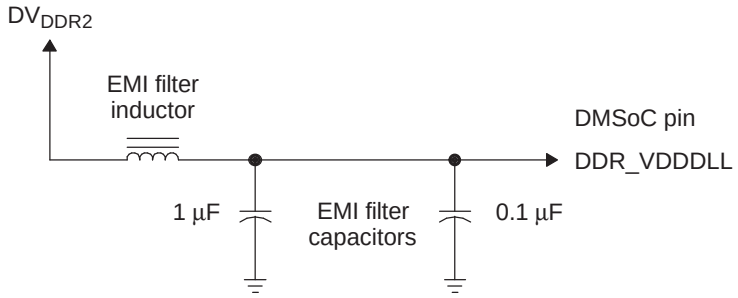
Figure 3. Example DDR2 Keep out Region

6.3 Discrete Device Placement

The DM4xx DDR2 interface uses a number of discrete devices consisting of resistors, resistor packs, capacitors, and inductors. Figure 5 shows an example placement of discrete devices around DM4xx and the DDR2 devices. It is useful to refer to it while reading the next sections.

6.3.1 PLL and DLL Filters

The DLL power supply pins on the DM4xx device draw small currents, but they are noise sensitive. The DLL power supply is derived from the DV_{DDR2} supply. Figure 4 shows the placement and routing rules for the DLL power supply.



EMI filter capacitors should be placed no further than 350 mils from associated DMSoC ball.

Traces for the nets in this figure should be 15 mils wide minimum. Necking down for BGA fanout is acceptable.

Figure 4. Example DLL Filter

6.3.2 Resistors and Resistor Packs

The DM4xx DDR2 interface uses resistors for VREF generation and may use resistors or resistor packs for signal terminations. Specific placement requirements for these components are specified by the routing rules for VREF and the other net classes of the interface. These routing rules are presented later in this document.

Generally speaking, termination resistors can be either discrete resistors or resistor packs and they are placed in between the DDR2 memories and the DM4xx. The VREF divider resistors will be placed somewhere in between the DDR2 devices and the DM4xx.

6.3.3 Bypass Capacitors

Bypass capacitors are critical to the reliable operation of a high speed PCB. Great care should be taken to ensure the following guidelines are followed. Failure to follow these guidelines will likely result in an unstable system.

Table 2 shows the minimum quantity of bypass capacitors required near the DM4xx and DDR2 devices. Additional bypass capacitors will be required for the rest of the system board. It is the responsibility of the system designer to design the bypass solution for the rest of the system. The small bypass capacitors (0.1uF) should be 0402 size or smaller. The 22uF mid-bulk bypass capacitors can be sized for availability and convenience. The capacitor values in Table 2 are intended to be a starting point. Adjustment of the values may have to be performed if the PCB has EMI compliance issues.

Exact placement of capacitors is not critical. Figure 5 is an example placement. Bypass capacitors should be placed near the device being bypassed. Distance from the capacitor to the power pins being bypassed should not exceed 125 mils.

Table 2. Bypass Capacitor Minimum Quantities

Power Supply	Quantity 22uF	Quantity 0.1 uF
CV_{DD}	2	4
CV_{DDDSP}	2	3
DV_{DD18}	2	8
VDDQ DDR2 #1	1	8
VDDQ DDR2 #2	1	8
DV_{DDR2}	3	11
DV_{DD33}	1	4

6.3.3.1 Bypass Capacitor Vias, Connections to Power Planes, and Placement

Each bypass capacitor requires two vias, one for each pin. Via sharing for bypass capacitors is not permitted. This is due to the inductance of the vias. Via sharing seriously compromises the performance of the bypass capacitor due to this inductance. For the same reason, sharing of vias by power and ground pins of the DM4xx or DDR2 devices is also not permitted. Vias used for bypass capacitor and device power connections are referred to as power vias.

To minimize inductance, power vias should be as large as possible. Use care to ensure power vias are not so large as to inadvertently cut planes. Power vias should be connected to the device pads with the shortest possible traces that are as wide as possible. Ideally, the trace length from the power via to the device pad should not exceed 30 mils. Maximum trace length from power via to bypass capacitor is 60 mils. Maximum trace length from power via to power ball pad is 35 mils.

Figure 5 shows an example placement for the bypass capacitors. Placement of the mid-bulk bypass capacitors (22uF) is not that critical and they can be placed to accommodate other circuitry with more constrained placement and routing requirements. The PCB designer should keep the trace length specifications in this section in mind when placing the bypass capacitors.

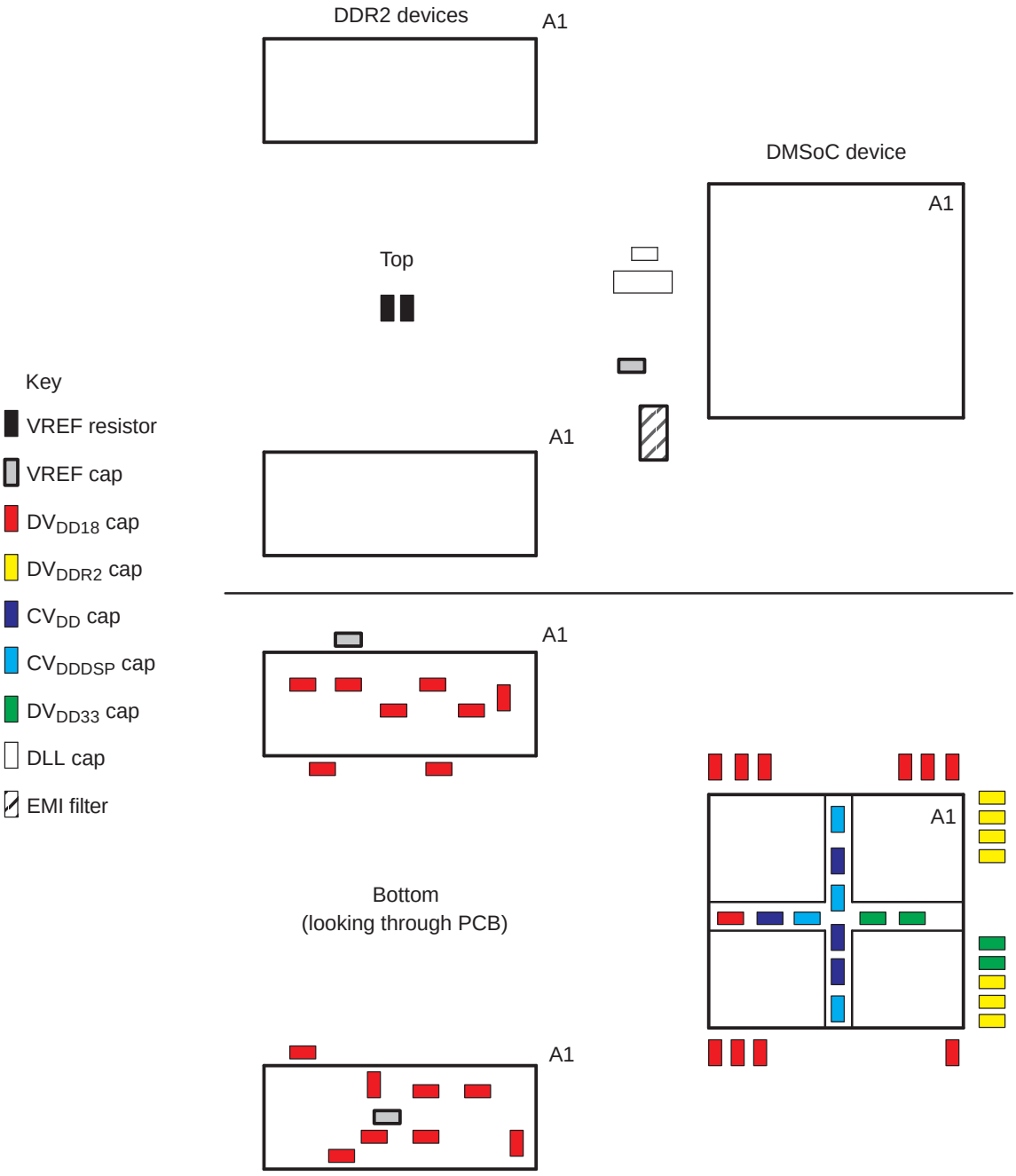


Figure 5. Discrete Part Placement

6.3.4 DDR2 Signal Terminations

Termination is not required to meet reflection and overshoot specifications provided the DDR2 device is operated at 60% strength. All DDR2 signals may be terminated if desired. Recommended terminations are shown in Table 3. There is room in the placement shown in Figure 2 for the terminations in Table 3. Termination values may have to be adjusted once hardware is available to pass EMI regulations.

Table 3. DDR2 Signal Terminations

Net Class	Termination
CK	10 ohm series resistor/resistor packs located near DMSoC
ADDR_CTRL	22 ohm series resistor/resistor packs located near DMSoC
DQB0 (DDR_D0-DDR-D7)	22 ohm series resistor/resistor packs located near DDR2
DQB0 (DDR_DQM[0])	22 ohm series resistor/resistor packs located near DMSoC
DQSB0	22 ohm series resistor/resistor packs located near DDR2
DQB1 (DDR_D8-DDR_D15)	22 ohm series resistor/resistor packs located near DDR2
DQB1 (DDR_DQM[1])	22 ohm series resistor/resistor packs located near DMSoC
DQSB1	22 ohm series resistor/resistor packs located near DDR2
DQB2 (DDR_D16-DDR_23)	22 ohm series resistor/resistor packs located near DDR2
DQB2 (DDR_DQM[2])	22 ohm series resistor/resistor packs located near DMSoC
DQSB2	22 ohm series resistor/resistor packs located near DDR2
DQB3 (DDR_D24-DDR_D31)	22 ohm series resistor/resistor packs located near DDR2
DQB3 (DDR_DQM[3])	22 ohm series resistor/resistor packs located near DMSoC
DQSB3	22 ohm series resistor/resistor packs located near DDR2

7 Routing

7.1 Required PCB Feature Sizes

The minimum PCB feature sizes referenced in this document are the largest that can be accommodated in order to physically route the PCB due to the size of the BGA packages. Maximum PCB trace width/space for BGA escape is 4 mils. Dog bone BGA escape will require via sizes on the order of 8 mil holes with 18 mil pads if conventional vias are used. Smaller feature sizes can also be used as well to improve PCB density as long as all routing rules are followed.

It is also a good idea to maximize the size of the vias used for bypass capacitors and power pins. This is done to minimize via inductance. It is the via and bypass capacitor stray inductance that limits the performance of the bypass capacitors. Use care to ensure that vias are not sized so large as to cut off a portion of a plane.

7.1.1 BGA Feature Sizes

PCB BGA feature size selection is critical for PCB yield and reliability. Generally, it is best if the pad on the PCB has the same area as the pad on the BGA package. Before layout begins, the device manufacturer, PCB fabricator and PCB assembler should be consulted with respect to BGA pad stacks and other critical BGA PCB mechanical details. As a general warning, the recommended BGA pad size is generally *not* equal to the BGA ball size.

The PCB BGA pad requirements for the DM4xx device are documented by the *Flip Chip Ball Grid Array Package Reference Guide* (SPRU811), available at www.ti.com. The DM4xx is a 0.8 mm ball pitch part and should follow the 0.8 mm guidelines. The PCB BGA pad requirements for the DDR2 device should follow its manufacturer's guidelines.

7.2 VREF

VREF is used by the input buffers of the DDR2 memories as well as the DM4xx DDR2 interface to determine logic levels. VREF is specified to be ½ the power supply voltage and is created using a voltage divider constructed from two 1K ohm, 1% tolerance resistors (see Figure 1). VREF is not a high current supply, but it is important to keep it as quiet as possible with minimal inductance. The minimum nominal trace width for VREF is 20 mils. Necking down VREF to accommodate BGA escape and localized via

congestion is acceptable, but care should be taken to keep VREF 20 mils wide as much as possible. VREF is a DC net and as such, trace delay is not critical, however, overall trace length should be kept to a minimum. The four or five bypass capacitors on the VREF net are intended to reduce AC noise. Two are used at the divider, and one each is used near the VREF input of the three loads (2 DDR2's and DM4xx). See Figure 6.

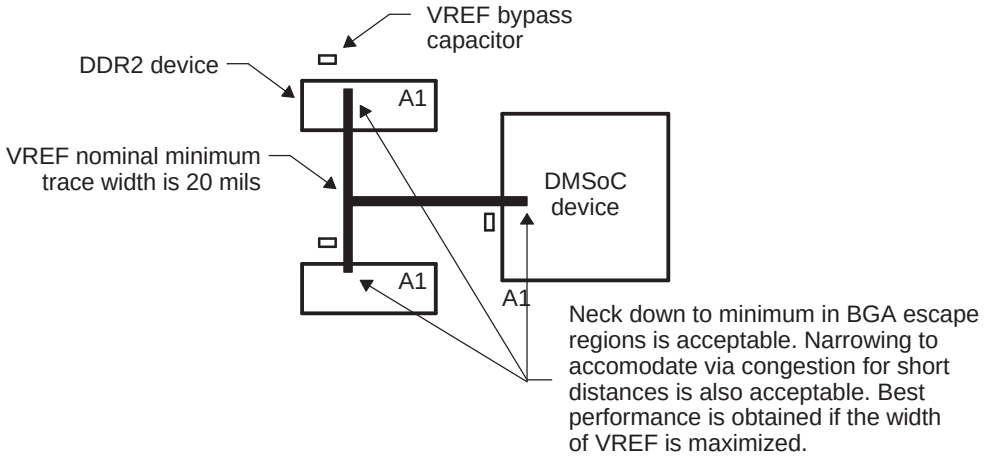


Figure 6. VREF Specification

7.3 General DDR2 Routing

Figure 7 through Figure 11 illustrate the general routing of the DDR2 interface. The address, bank address, control signals, as well as the DDR2 clock route from the center of the DM4xx device to the DDR2 devices in a "balanced T" route. Each data byte is routed point to point, with the lower two bytes routing to the lower DDR2 memory and the upper two bytes routing to the upper DDR2 memory. The figures show the maximum PCB area placement. Tighter placements are achieved by reducing feature size and/or adding PCB layers and pulling the DDR2 memories toward each other and/or closer to the DM4xx device. The routing of the DDR2 interface should look similar to these figures when a proper placement is used. Note that the most extreme minimum placement of DDR2 devices, overlapping each other with one on the top and the other on the bottom of the PCB should work; however, all routing rules must still be followed. This type of placement will require advanced PCB technology.

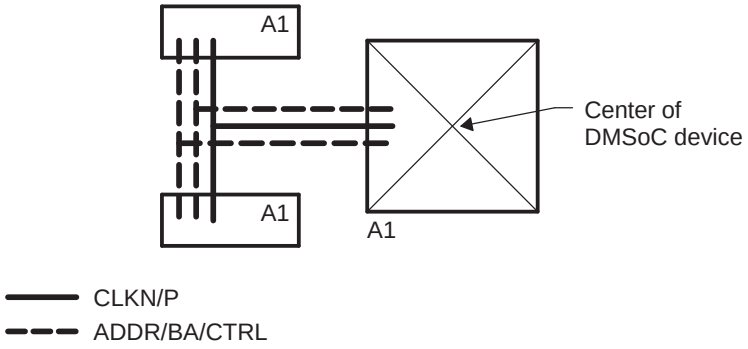


Figure 7. General Address, Bank Address, Control, and Clock Routing

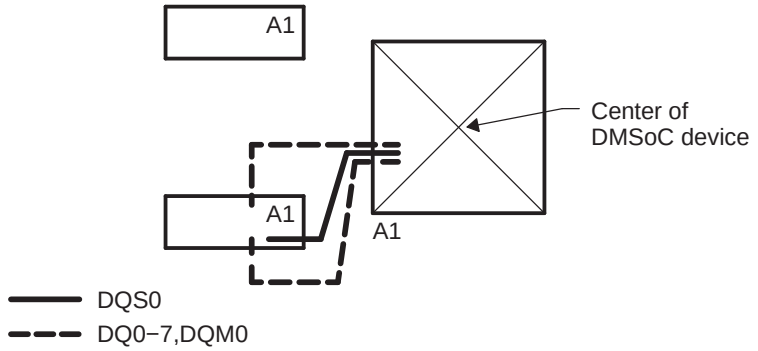


Figure 8. General Data Byte 0 Routing

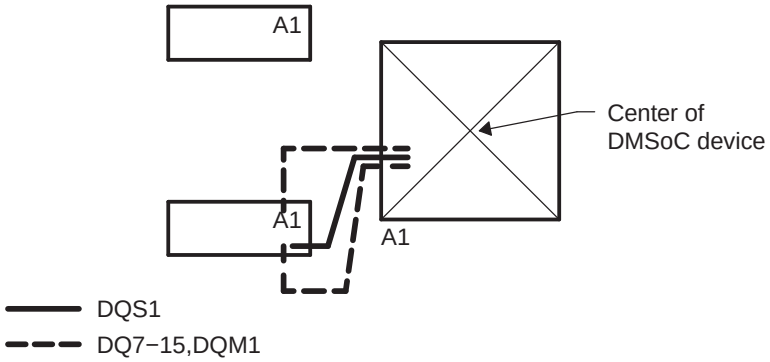


Figure 9. General Data Byte 1 Routing

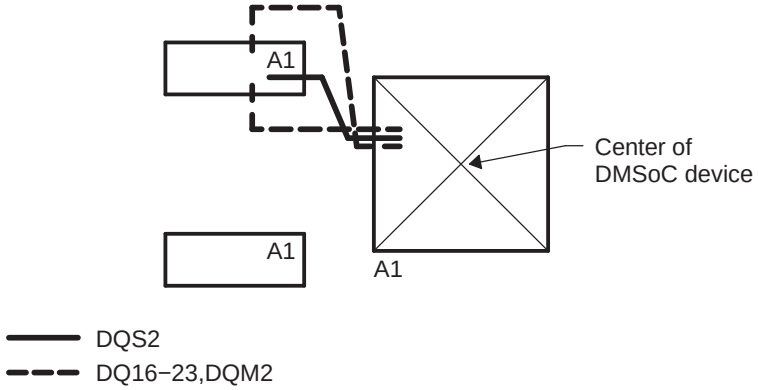


Figure 10. General Data Byte 2 Routing

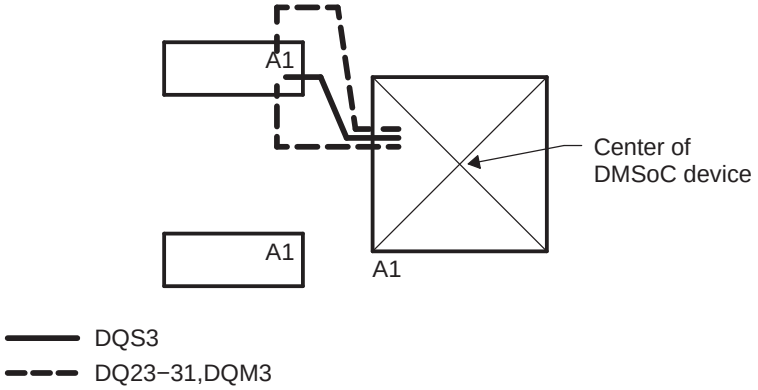


Figure 11. General Data Byte 3 Routing

7.4 Signal Routing Rules

The routing rules for the DM4xx DDR2 system design are divided among net classes. Each net class contains all the signals within a clock domain. There are five clock domains: CK, DQS0, DQS1, DQS2, and DQS3. The general requirement is to skew match within a domain and to minimize crosstalk. Crosstalk across domains is especially troublesome and steps should be taken to minimize coupling between signals in different domains.

The PCB routing rules in this document assume a minimum PCB route width and spacing of 4 mils. The PCB route trace width is defined as w for the purposes of defining minimum trace separation for the various net classes discussed later in the routing rules. Thus, if the PCB is designed with the widest possible traces, then the trace width is w = 4 mils. If the PCB is designed with 3 mil traces/spaces, w would be 3 mils.

7.4.1 Net Classes

7.4.1.1 Clock Domain Net Classes

Net classes are used to associate the assorted groups of nets in the DDR2 interface to each other and their clock domain. These net classes are used in the DDR2 routing rules. The DDR2 interface has five clock domains, four of which are bi-directional. The clock net classes are shown in Table 4.

The CK clock net class is differential; the other four clock net classes (DQSB0-3) are single ended. The CK clock net class needs to be routed as a differential signal with matched lengths for the non-inverting and inverting signals. Differential impedance should also be controlled.

7.4.1.2 Signal Net Classes

Table 5 shows the five additional net classes that use the clock net classes as their reference. Generally speaking, the nets within a net class and their associated clock net class should be skew matched to each other. The goal is to minimize the skew within each clock domain and crosstalk betweens signals – especially between signals of differing clock domains.

Table 4. Clock Net Classes

Clock Net Class	Description	DMSoC Pin Names
CK	DDR2 Interface Clock	DDR_CLKO DDR_CLKO_#
DQSB0	DQS for byte 0	DDR_DQS[0]
DQSB1	DQS for byte 1	DDR_DQS[1]
DQSB2	DQS for byte 2	DDR_DQS[2]
DQSB3	DQS for byte 3	DDR_DQS[3]

Table 5. Signal Net Classes

Net Class	Associated Clock Net Class	Description	DMSoC Pin Names
ADDR_CTRL	CK	Bank Address, Address, Control	DDR_BA[0-2] DDR_A[0-13] $\overline{\text{DDR\_CS}}$ $\overline{\text{DDR\_CAS}}$ $\overline{\text{DDR\_RAS}}$ $\overline{\text{DDR\_WE}}$ DDR_CKE
DQB0	DQSB0	DQs for byte 0	DDR_D[0-7] DDR_DQM[0]
DQB1	DQSB1	DQs for byte 1	DDR_D[8-15] DDR_DQM[1]
DQB2	DQSB2	DQs for byte 2	DDR_D[16-23] DDR_DQM[2]
DQB3	DQSB3	DQs for byte 3	DDR_D[24-31] DDR_DQM[3]

7.4.1.3 A Word About Trace Separation and BGA Escapes

The net class routing rules in the next section give minimum trace separation requirements for the respective net class. It is understood that in the region near the BGA devices that the traces will have to be routed quite close together, many times at minimum trace separation. Minimum separation routing should be kept to a minimum and the total minimum separation routed length should not exceed 500 mils for each net.

7.5 Net Class Routing Rules

7.5.1 CK and ADDR_CTRL

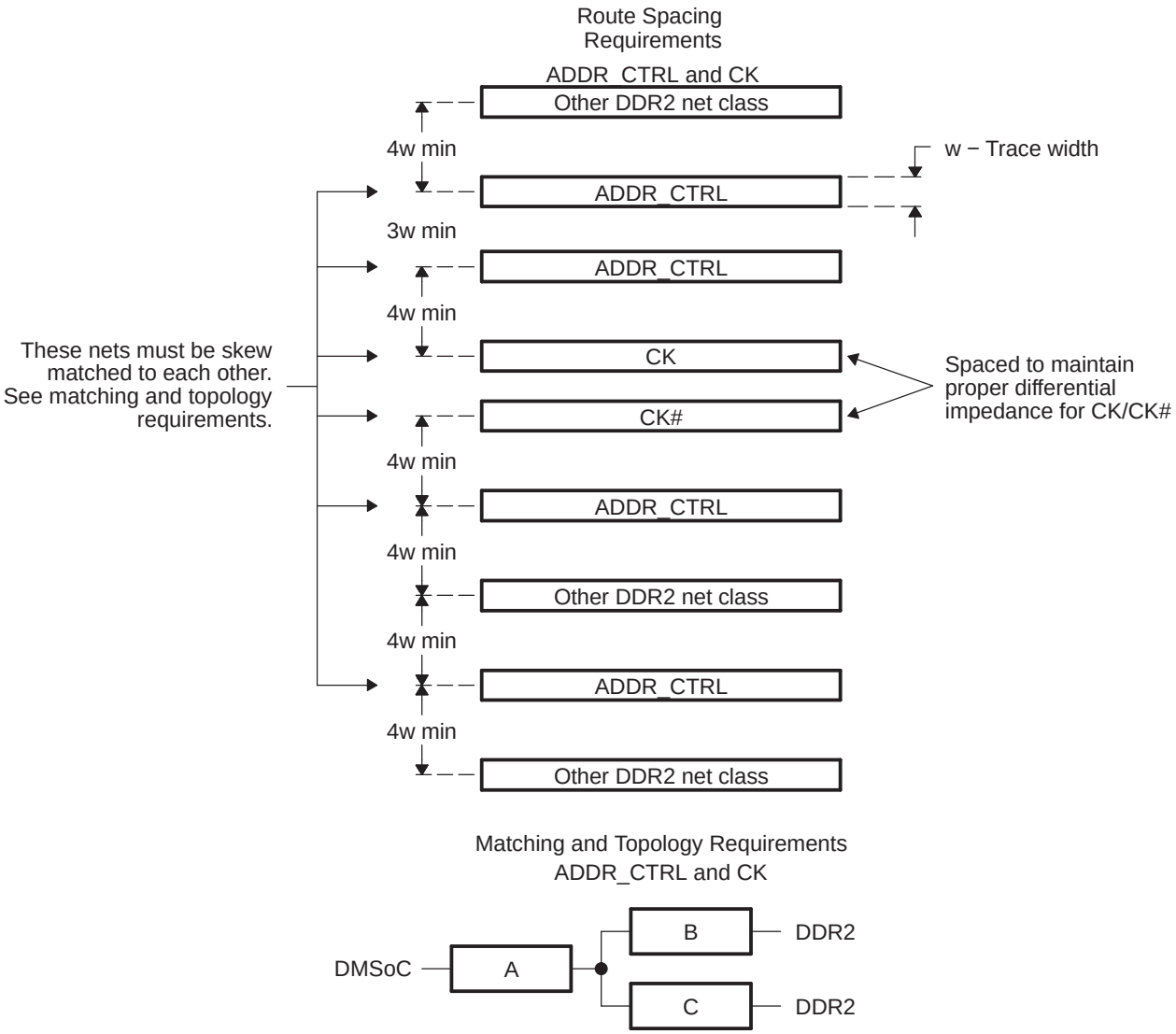
This net class is completely sourced by the DM4xx to the DDR2 devices. Each net is a balanced "T" route, see Figure 12. Ideally, the PCB delay of the CK net class is identical to the delay for the ADDR_CTRL net class. All nets in the CK and ADDR_CTRL net classes should be matched in length to each other within 100 mils. The nets in the CK net class must be laid out as a differential pair. The trace separation between the differential pair of net class CK should be such to maintain the desired differential impedance. Other traces should be kept away from the CK net class traces by at least 4*w* center-to-center spacing (recall that *w* = minimum trace width/space). Traces within the ADDR_CTRL net class should be spaced at least 3w center-to-center from each other. Traces of other net classes should be kept 4*w* away from the ADDR_CTRL net class. The length of segment A should be maximized and the overall length from A to B or A to C should be minimized.

7.5.2 DQSBn and DQBn

The 8 net classes that make up the 4 DQS's and 4 DQ bytes have the same routing rules. Note the individual byte net classes do not have to be skew matched to each other. Skew matching is only required between the DQBn net class and its associated DQSBn net class. Figure 13 shows the topologies for the DQSBn and DQSB nets.

These net classes are sourced by the DM4xx device during writes and are sourced by the DDR2 devices during reads. The DQS acts as the data strobe at it is always sourced with the DQs. For write cycles, the DQS transitions in the middle of the bits cells on DQ. For read cycles, the DQS transitions at the same time as the DQS. The interface is more sensitive to DQS <-> DQ crosstalk during reads. The data mask bits (DDR_DQM[n]) are static during reads, thus they can be used as shields between the DQ and DQS to improve read crosstalk performance.

Ideally, the PCB delay of the DQSBn net class is identical to the delay for the DQBn net class. All nets in the DQSBn and DQBn net class should be matched in length to each other within 100 mils. The longest trace permissible is equal to the longest manhattan distance of the DQSBn and DQBn net classes. Other traces should be kept away from the DQSBn net class traces by at least 4*w* center-to-center spacing (recall that *w* = minimum trace width/space). Traces within the DQBn net classes should be spaced at least 3*w* center-to-center from each other. Traces of other net classes should be kept 4*w* away from the DQBn net class.



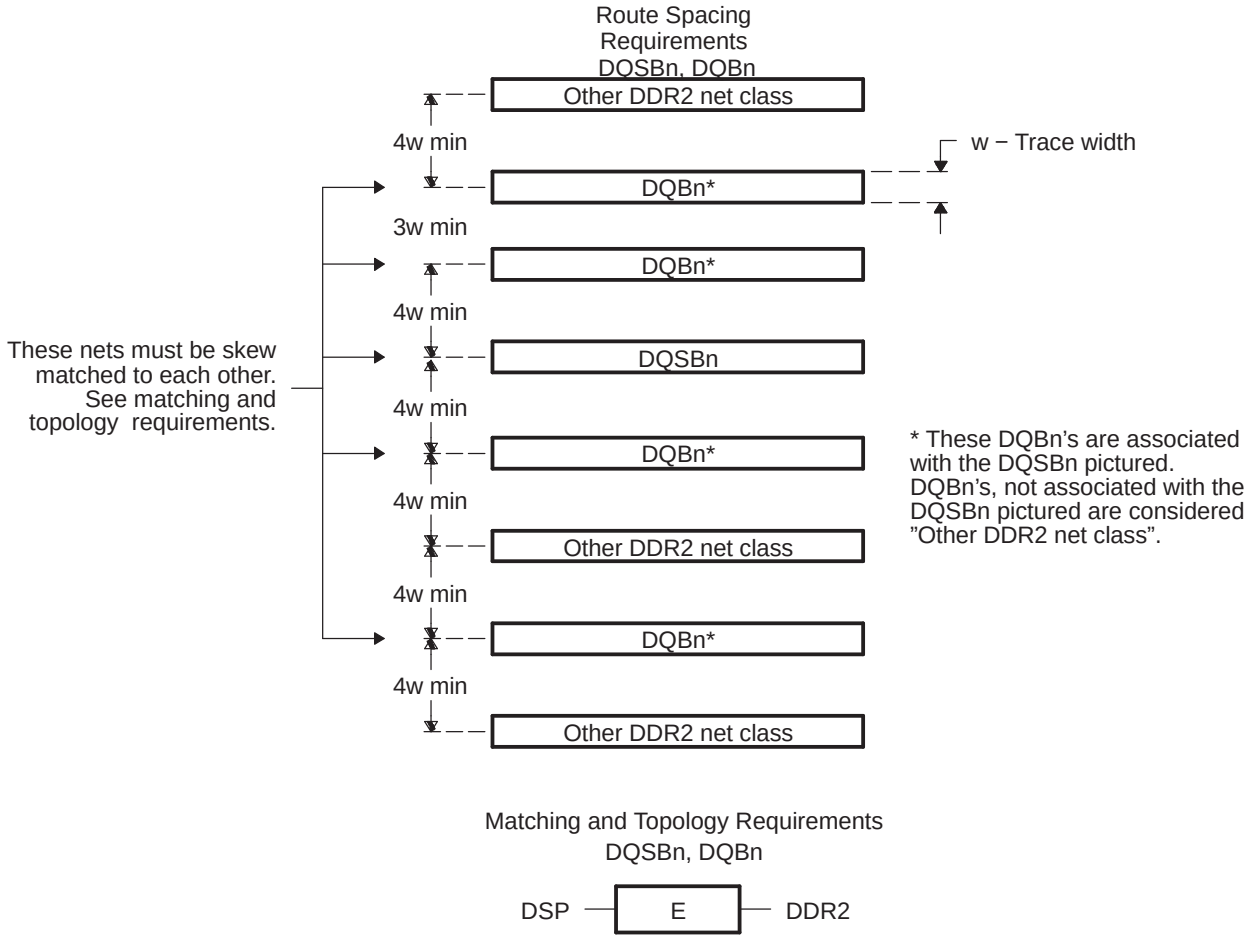
For ADDR_CTRL and CK:

1) Length B should match length C within 100 mils.
2) Length A to C and A to B should match within 100 mils within ADDR_CTRL net class.
3) Series terminating resistor, if desired, should be located closest to DMSoC as possible.
4) Length A should be maximized while meeting the above specifications.

In addition, for CK:

5) The length of CK should match length of net CK# within 25 mils.

Figure 12. Route Spacing, Matching, and Topology Requirements for ADDR_CTRL and CK Net Classes



For DQBn and DQSBn:

1) Length E should match within 100 mils within the DQSB0 and DQB0 net classes.
2) Length E should match within 100 mils within the DQSB1 and DQB1 net classes.
3) Length E should match within 100 mils within the DQSB2 and DQB2 net classes.
4) Length E should match within 100 mils within the DQSB3 and DQB3 net classes.
5) Series terminating resistor, if desired, should be located closest to DDR2 as possible for data bits (DDR_D[n]) and closest to DSP as possible for data masks (DDR_DQM[n]).

Figure 13. Routing Spacing, Matching, and Topology Requirements for the DQBn and DQBSn Net Classes

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