ABSTRACT
This application report describes the TMS320DM6467 embedded Host electrical compliance of a high-speed (HS) universal serial bus (USB) operation conforming to the USB 2.0 specification. The non-OTG controller supports the USB 2.0 Host mode operation at HS, full-speed (FS), and low-speed (LS). Furthermore, it supports the USB 2.0 device mode operation at HS and FS. LS operation, when assuming the role of a device, is not supported.

Contents
1 Introduction ........................................................................................................................................... 2
2 Test Items ............................................................................................................................................... 3
3 Required Instruments ............................................................................................................................. 4
4 Test Condition ......................................................................................................................................... 5
5 References .............................................................................................................................................. 31

List of Figures
1 USB Functional Block Diagram .................................................................................................................. 2
2 Equipment Setup for High-Speed Downstream Host Signal Quality Testing ............................................. 6
3 Downstream Eye Diagram ........................................................................................................................ 7
4 Downstream Waveform Plot ..................................................................................................................... 8
5 Rise and Fall Time Patterns ..................................................................................................................... 8
6 Duty Cycle Distortion (DCD) .................................................................................................................. 9
7 Random Jitter/Deterministic Jitter/Total Jitter .......................................................................................... 9
8 Equipment Setup for Downstream Host Packet Parameters Tests ......................................................... 10
9 Status Stage of a GET DEVICE DESCRIPTOR Transaction SYNC Field of the Token Packet ................. 11
10 Inter-Packet-Gap Between the Data Packet of Device and Acknowledge Packet of the Embedded Host on the Data Stage of the GET DESCRIPTOR Command ................................................. 12
11 Inter-Packet-Gap Between the Token Packet and the Data Packet of the Status Stage of the GET DESCRIPTOR Transaction ............................................................................................................. 13
12 EOP Field of Non-SOP Packet of the Data Packet of the Status Stage of the GET DESCRIPTOR Command .............................................................................................................................................. 14
13 EOP Field of an SOP Packet .................................................................................................................. 15
14 Equipment Setup for Downstream Host Chirp and Suspend and Resume Timings .................................. 16
15 Downstream Chirp Response Time ........................................................................................................ 17
16 Chirp-K and Chirp-J Duration ................................................................................................................ 18
17 Time Between First SOF and Last Chirp-(J or K) .................................................................................... 19
18 DUT Host Enters Suspend State ............................................................................................................. 20
19 DUT Host Resumes .................................................................................................................................. 21
20 Equipment Setup for Downstream Test J/K, SEO_NAK ......................................................................... 22
21 Equipment Setup for Full-Speed Downstream Host Signal Quality Testing .......................................... 24
22 Full-Speed Downstream Signal Quality Test .......................................................................................... 25
23 Waveform Plot ...................................................................................................................................... 26
24 Full-Speed Eye Diagram ........................................................................................................................ 27
1 Introduction

The DM6467 Host high-speed electrical test of the USB is performed on a verification and debug board (VDB), which is used to validate the device feature and is not optimized for USB characterization. Better results are expected when using test boards that are optimized for characterization purposes. These optimized boards follow the board design guidelines as recommended by the USB-IF. In addition, the DM6467 device is soldered directly to the board instead of residing in a socket as used on the VDB.

The USB functional block diagram is shown in Figure 1.

---

**List of Tables**

1. Host Electrical Tests Result Summary ............................................. 3
2. Test Categories ............................................................................. 3
3. Required Instruments ................................................................... 4
4. Power Supply Voltage and Temperature Condition ........................... 5
5. Test Packet Data ........................................................................... 5
6. Overall Results of Signal Quality Test .............................................. 6
7. Result Summary for Full-Speed Downstream Host Signal Quality .......... 27
8. Result Summary for Low-Speed Downstream Host Signal Quality Test .... 31

---

**Figure 1. USB Functional Block Diagram**

---

Code Composer Studio is a trademark of Texas Instruments.
Windows is a registered trademark of Microsoft Corporation in the United States and/or other countries.
Tektronix is a registered trademark of Tektronix, Inc.
All other trademarks are the property of their respective owners.
2 Test Items

Table 1 shows a summary of the test listings results of the compliance tests performed to evaluate the USB controller operation while operating in Host mode.

<table>
<thead>
<tr>
<th>Test#</th>
<th>Test Items</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB_EL.2</td>
<td>HS Host transmitter data rate 480 Mb/s ± 0.05%</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.3</td>
<td>HS Host signal quality test measured at the near end</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.6</td>
<td>10% to 90% differential rise and fall time &gt; 500 ps</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.7</td>
<td>Monotonic data transitions over the vertical openings in the appropriate EYE pattern template</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.21</td>
<td>SYNC field (packet originating from Host)</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.22</td>
<td>Inter-packet gap field (device and Host)</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.23</td>
<td>Inter-packet gap field (back-to-back Host)</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.25</td>
<td>EOP field (non-SOF packets)</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.55</td>
<td>EOP field (SOF packets)</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.33</td>
<td>Chirp response time</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.29</td>
<td>Chirp-K and chirp-J duration</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.31</td>
<td>Time between SOF and last chirp-(JorK)</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.39</td>
<td>Host suspend capability/timing</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.41</td>
<td>Host resume capability/timing</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.8</td>
<td>Test J/K (controller transmits continuous J)</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.8</td>
<td>Test K (controller transmits continuous K)</td>
<td>PASS</td>
</tr>
<tr>
<td>USB_EL.9</td>
<td>Test_SE0 (controller does not drive data lines)</td>
<td>PASS</td>
</tr>
<tr>
<td>--------</td>
<td>Legacy compliance (full-speed signal quality)</td>
<td>PASS</td>
</tr>
<tr>
<td>--------</td>
<td>Legacy compliance (low-speed signal quality)</td>
<td>PASS</td>
</tr>
</tbody>
</table>

The tests are classified into six categories (see Table 2). These categories correspond to the electrical test in the USB2.0 compliance test.

<table>
<thead>
<tr>
<th>Test Items</th>
<th>Categories</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS Host transmitter data rate 480 Mb/s ± 0.05%</td>
<td>HS downstream signal quality test</td>
</tr>
<tr>
<td>HS Host signal quality test measured at the near end</td>
<td></td>
</tr>
<tr>
<td>10% to 90% differential rise and fall time &gt; 500ps</td>
<td></td>
</tr>
<tr>
<td>Monotonic data transitions over the vertical openings in the appropriate EYE pattern template</td>
<td></td>
</tr>
<tr>
<td>SYNC field (packet originating from Host)</td>
<td>Host packet parameters</td>
</tr>
<tr>
<td>Inter-packet gap field (device and Host)</td>
<td></td>
</tr>
<tr>
<td>Inter-packet gap field (back-to-back Host)</td>
<td></td>
</tr>
<tr>
<td>EOP field (non-SOF packets)</td>
<td></td>
</tr>
<tr>
<td>EOP field (SOF packets)</td>
<td></td>
</tr>
<tr>
<td>Chirp response time</td>
<td>Host chirp timing</td>
</tr>
<tr>
<td>Chirp-K and chirp-J duration</td>
<td></td>
</tr>
<tr>
<td>Time between SOF and last chirp-(JorK)</td>
<td></td>
</tr>
<tr>
<td>Host suspend capability/timing</td>
<td>Host suspend/resume timing</td>
</tr>
<tr>
<td>Host resume capability/timing</td>
<td></td>
</tr>
<tr>
<td>Test J (controller transmits continuous J)</td>
<td>Host test_J/K/SE0</td>
</tr>
<tr>
<td>Test K (controller transmits continuous K)</td>
<td></td>
</tr>
<tr>
<td>Test_SE0 (Host stops driving data lines)</td>
<td></td>
</tr>
</tbody>
</table>
### Table 2. Test Categories (continued)

<table>
<thead>
<tr>
<th>Test Items</th>
<th>Categories</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full-speed signal quality</td>
<td>Legacy USB compliance testing</td>
</tr>
<tr>
<td>Low-speed signal quality</td>
<td></td>
</tr>
</tbody>
</table>

### 3 Required Instruments

This section discusses the required instruments used for performing compliance tests. USB characterization tests are performed using test fixtures produced by Tektronix®.

**Note:** It is recommended that you use a scope with a 2 GHz bandwidth for performing the tests. This will not allow noise magnification to disturb the test. The DSA71604 is a very fast scope with a maximum operating bandwidth of 16 GHz. Even though the bandwidth needed is user selectable, during the time this test was performed, the TDSUSB2 software re-configures the user set bandwidth to the default 16 GHz speed configuration, disrupting the user settings. This is more important when performing low-speed signal quality testing since the test result captures differ heavily with a low bandwidth configuration yielding a much better result.

The high-speed electrical test (HSET) is not applicable for use with this solution since it requires an EHCI USB controller with Windows® XP/2000 running on the device. The DM6467 USB controller is not an EHCI controller, nor is it not running the required operating system (O/S). For this reason, you are required to create a similar application to the HSET utility furnished by the USB-IF. This utility should put the USB controller into the required test modes or configure the USB controller to perform transfers to create the right test conditions applicable for the test. The method used to invoke these tests is a Host test program running under Code Composer Studio™ software with test options controlled by variables where you select the desired test by modifying the variables within the watch window.

### Table 3. Required Instruments

<table>
<thead>
<tr>
<th>Type</th>
<th>Manufacturer</th>
<th>Product</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscilloscope</td>
<td>Tektronix</td>
<td>DSA71604</td>
<td>To measure USB signals</td>
</tr>
<tr>
<td>Differential probe (1)</td>
<td>Tektronix</td>
<td>P7313</td>
<td>Signal quality/receiver sensitivity tests</td>
</tr>
<tr>
<td>Single ended FET probe (2)</td>
<td>Tektronix</td>
<td>P6245</td>
<td>Packet parameters/Chirp timings</td>
</tr>
<tr>
<td>Measurement application (USB test software that is part of the scope application)</td>
<td>Tektronix</td>
<td>TDSUSB V3.1.1 Build 2</td>
<td>USB compliance test software specifically used for USB</td>
</tr>
<tr>
<td>Test fixture</td>
<td>Tektronix</td>
<td>TDSUSBF 071-1832-01</td>
<td>For USB test</td>
</tr>
<tr>
<td>Power Supply</td>
<td>-</td>
<td>-</td>
<td>5 V power supply for TDSUSBF</td>
</tr>
<tr>
<td>Digital multimeter</td>
<td>-</td>
<td>-</td>
<td>Actual voltage monitor</td>
</tr>
<tr>
<td>Test board (VDB) (1)</td>
<td>TI</td>
<td>EVM like board</td>
<td>Non-optimized test board used for DM6467 device validation</td>
</tr>
<tr>
<td>4 self powered USB certified high-speed hubs</td>
<td>-</td>
<td>-</td>
<td>For full-speed signal quality testing</td>
</tr>
<tr>
<td>1 self powered USB certified full-speed hub</td>
<td>-</td>
<td>-</td>
<td>For full-speed signal quality testing</td>
</tr>
<tr>
<td>1 known good USB 2.0 certified compliant device</td>
<td>-</td>
<td>-</td>
<td>For high-speed testing</td>
</tr>
<tr>
<td>1 known good USB 1.1 certified compliant device</td>
<td>-</td>
<td>-</td>
<td>For full-speed signal quality testing</td>
</tr>
<tr>
<td>1 USB mouse</td>
<td>-</td>
<td>-</td>
<td>For low-speed signal quality test</td>
</tr>
<tr>
<td>6 five meter USB cable</td>
<td>-</td>
<td>-</td>
<td>For full-speed signal quality testing</td>
</tr>
</tbody>
</table>

(1) Results could change for the better if using an optimized test board.
4 Test Condition

4.1 Power Supply Voltage/Temperature

Table 4 shows the power supply voltage and temperature conditions:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB_VDDA1P2LDO</td>
<td>1.14</td>
<td>1.2</td>
<td>1.26</td>
<td>V</td>
</tr>
<tr>
<td>USB_VDDA3P3</td>
<td>3.1</td>
<td>3.3</td>
<td>3.5</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-10</td>
<td>25</td>
<td>95</td>
<td>°C</td>
</tr>
</tbody>
</table>

4.2 HS Downstream Signal Quality Test

The HS downstream signal quality test uses the TEST_PACKET to place the DM6467 USB controller in a test mode where the controller continuously transmits a fixed defined format test packet, which is defined in the USB 2.0 specification, Section 7.1.20. Even though there are many ways to achieve this task, the method used here is for the DM6467 to enumerate a known good device (a HS USB Flash drive); at the end of enumeration, you will force the device to go into TEST_PACKET test mode via the Code Composer Studio watch window. When this test mode is entered, the device continually transmits the data packet shown in Table 5.

The oscilloscope, along the embedded TDSUSB2 software, automatically analyzes the test packet signal quality as observed on the USB bus. For detailed procedures on how to configure the scope as well as the TDSUSB2 software, see the Host High-Speed Electrical Test Procedure documentation issued by the USB Implementers Forum (http://www.usb.org/home).

<table>
<thead>
<tr>
<th>Table 5. Test Packet Data</th>
</tr>
</thead>
</table>
| Data Used for Generating Test Packet | 00 00 00 00 00 00 00 00 00 00 00 00 AA AA AA AA AA AA AA AA EE EE EE EE EE EE EE EE EE EE FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
4.2.1 EL_2: Signal Rate

A USB 2.0 high-speed transmitter data rate must be 480 Mb/s ± 0.05%.

4.2.2 EL_3: Signal Quality/Eye Diagram Test

An eye diagram provides an intuitive view of jitter. It is a composite view of all the bit periods of a captured waveform superimposed upon each other. The USB 2.0 downstream port on a device, without a captive cable, must meet template 1 transform waveform requirements measured at a test point close to the port.

4.2.3 EL_6: Rise and Fall Time

A USB 2.0 high-speed driver must have 10% to 90% differential rise and fall times of greater than 500 ps.

4.2.4 EL_7: Monotonic Data Transitions

A USB 2.0 driver must have monotonic data transitions over the vertical openings specified in the appropriate EYE pattern template. These results were based on USB-IF/waiver limits.

Table 6. Overall Results of Signal Quality Test (1)

<table>
<thead>
<tr>
<th>Measurement Name</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Mean</th>
<th>pk-pk</th>
<th>Standard Deviation</th>
<th>RMS</th>
<th>Pop.</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye diagram test</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Signal rate</td>
<td>474.1477 Mbps</td>
<td>488.1790 Mbps</td>
<td>479.9187 Mbps</td>
<td>0.0000 bps</td>
<td>2.254397 Mbps</td>
<td>479.9072 Mbps</td>
<td>512</td>
<td>Pass</td>
</tr>
<tr>
<td>EOP width</td>
<td>-</td>
<td>-</td>
<td>16.63800 ns</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>Pass</td>
</tr>
<tr>
<td>EOP width (bits)</td>
<td>-</td>
<td>-</td>
<td>7.984887 ns</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>Pass</td>
</tr>
<tr>
<td>Rise time</td>
<td>-719.3333 ps</td>
<td>2.947333 ns</td>
<td>624.3670 ps</td>
<td>3.666667 ns</td>
<td>346.5622 ps</td>
<td>713.3141 ps</td>
<td>107</td>
<td>Pass</td>
</tr>
<tr>
<td>Fall time</td>
<td>458.4421 ps</td>
<td>1.309169 ns</td>
<td>897.5293 ps</td>
<td>850.7271 ps</td>
<td>145.8569 ps</td>
<td>909.1953 ps</td>
<td>108</td>
<td>Pass</td>
</tr>
</tbody>
</table>

(1) Additional Information:
- Consecutive jitter range: 53.98 ps to 33.51 ps RMS jitter 16.98 ps
- KJ paired jitter range: -36.29 ps to 42.12 ps RMS jitter 13.10 ps
- JK paired jitter range: -37.51 ps to 27.63 ps RMS jitter 12.75 ps
• Eye diagram/signal eye (Figure 3)
• Waveform plot (Figure 4)
• Rise/fall time (Figure 5)
• Duty cycle distortion (DCD) (Figure 6)
• Jitter (Figure 7)
  – Random jitter (RJ)
  – Deterministic jitter (DJ)
  – Total jitter (TJ)

Figure 3. Downstream Eye Diagram
Figure 4. Downstream Waveform Plot

Figure 5. Rise and Fall Time Patterns
4.3 Host Packet Parameters

The Host packet parameter tests are comprised of a set of tests that pertains to the fields/elements of USB packets. Unlike the signal quality test, the Host controller does not need to enter into a test mode. A single step GET DEVICE DESCRIPTOR control transfer is invoked from the DM6467 DUT Host by pausing in between transactions to an attached known good high-speed device (Flash drive was used on this setup). The downstream host high-speed packet parameter test requires the use of the three stages of the GET DEVICE DESCRIPTOR command: setup, data, and status. The DM6467 DUT Host invokes the setup stage of the transaction and pauses until it is told to continue. For a GET DEVICE DESCRIPTOR command, it would be good to measure the Host packet parameters tests from either the setup stage or the status stage of the transaction since both of these stages comprises of the token and data packets originating from the Host. The packet delimiter fields, SYNC, EOP fields, and inter-packet delay are measured from either the setup stage or the status stage of the transaction.
Figure 8 displays the equipment setup for the high-speed downstream Host packet parameter tests.

Figure 8. Equipment Setup for Downstream Host Packet Parameters Tests
4.3.1 EL_21: Synchronization (SYNC) Field

The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field. Figure 9 displays the status stage of the GET DESCRIPTOR command with the SYNC field of the token packet zoomed.

Handshake packet SYNC field: PASS

---

**Note:** Measured value: 66.0 ns => 66.0 ns / (1/480*10^6) = 31.68 bits.

---

**Figure 9. Status Stage of a GET DEVICE DESCRIPTOR Transaction SYNC Field of the Token Packet**
4.3.2 EL_22: Inter-Packet-Gap Field of Device and Host Packets

When transmitting after receiving a packet, hosts and devices must provide an inter-packet-gap of at least 8-bit times and not more than 192-bit times.

To test this parameter, it is important to use a transaction that forces the DM6467 Host to source a packet in response to a reception of a packet from the known good device. The data stage of the GET DESCRIPTOR command is ideal transaction to measure the inter-packet-gap existing between the device responding with its descriptor data and the DUT Host acknowledging the reception by testing the gap time honored by the DUT Host DM6467 device.

Figure 10 displays the inter-packet-gap observed between the device and embedded Host packets.

Packet gap between device data packet and Host acknowledge packet: PASS

Note: Measured value: 221.6 ns => 221.6 ns / (1/480*10^6) = 106.368 bits.

Figure 10. Inter-Packet-Gap Between the Data Packet of Device and Acknowledge Packet of the Embedded Host on the Data Stage of the GET DESCRIPTOR Command
4.3.3 EL_23: Inter-Packet-Gap Field of Back-to-Back Packets

The Host transmitting two packets in a row must have an inter-packet-gap of at least 88-bit times and not more than 192-bit times.

Figure 11 displays the inter-packet-gap between the token packet and the zero byte data packet of the status stage of a GET DESCRIPTOR command sourced from the DUT Host with the inter-packet-gap zoomed.

Packet gap between the Host token packet and the Host data packet: PASS

**Note:** Measured value: 273.2 ns => 273.2 ns / (1/480*10^6) = 131.136 bits.

Figure 11. Inter-Packet-Gap Between the Token Packet and the Data Packet of the Status Stage of the GET DESCRIPTOR Transaction
4.3.4 **EL_25: End-of-Packet (EOP) Field of Non-SOF Packets**

The EOP for all transmitted packets (except SOF) must be an 8-bit NRZI byte of 01111111 without bit stuffing. Note, that a longer EOP is waiverable.

The EOP of the token packet or the data packet of the status stage can be used to verify this timing since both of these packets are sourced by the DUT DM6467 Host during the status stage of a GET DESCRIPTOR command. **Figure 12** displays the EOP field of the data packet of the status stage of the GET DESCRIPTOR command.

Non-SOP EOP field: PASS.

---

**Note:** Measured value: 17.2 ns => 17.2 ns / (1/480*10^6) = 8.256 bits.

---

**Figure 12.** EOP Field of Non-SOP Packet of the Data Packet of the Status Stage of the GET DESCRIPTOR Command
4.3.5 **EL_55: End-of-Packet (EOP) Field of SOF Packets**

The Host transmitting SOF packets must provide a 40-bit EOP without bit stuffing where the first symbol of the EOP is a transition from the last data symbol. *Figure 13* displays the EOP field capture of a SOF packet.

SOF packet EOP Field: PASS.

---

**Note:** Measured value: $83.6\text{ ns} \Rightarrow 83.6\text{ ns} / (1/480\times10^6) = 40.128\text{ bits}$

---

*Figure 13. EOP Field of an SOP Packet*
4.4 Device Chirp Timing

The Host chirp timing is used to validate high-speed detection handshake and happens during reset time. Some time after the Host resets a high-speed device, the device should indicate its high-speed capability by generating chirp-K signaling. A high-speed Host follows up by generating a minimum of three sets of chirp-KJ signaling at full-speed signaling environment. The device should disconnect its 1.5KΩ pull-up resistor and enable the 45 Ω termination resistors right after the last chirp J from the Host.

To invoke this test, a similar setup used for the device parameter testing, with two single ended FET probes replacing the differential probe, is used and shown on Figure 14.

There are several ways to perform this test. The method used here is to perform the test during an initial attachment. However, the embedded Host test software can be programmed to perform a RESET.

Figure 14. Equipment Setup for Downstream Host Chirp and Suspend and Resume Timings
4.4.1 EL_33: Chirp Response Timing

Downstream ports start sending and alternating a sequence of chirp K’s and chirp J’s within 100 µs after the device chirp K stops. Should be <= 100 µs.

The device chirp K stop time is usually detected when the signal level of the chirp K drops around its high value.

Chirp response timing is the time between the device’s de-assertion of chirp-K and the start of the alternate chirp-K and chirp-J sent by the Host.

Figure 15 displays the chirp response time measured for a downstream DM6467 Host device.

Chirp response time: PASS

---

**Note:** Measured value: 2.0 µs

---

![Figure 15. Downstream Chirp Response Time](https://www.ti.com/lit/ds/symlink/spraav9.pdf)
4.4.2 EL_34: Chirp-K and Chirp-J Duration

Downstream ports start sending and alternating a sequence of chirp K’s and chirp J’s within 100 µs after the device chirp K stops.

Chirp-K and chirp-J duration must be between 40 µs and 60 µs.

Figure 16 displays chirp-K and chirp-J duration measured for the DM6467 Host DUT device.

Chirp-K and chirp-J duration: PASS.

Note: Measured value: 1.09651 ms.

Figure 16. Chirp-K and Chirp-J Duration
4.4.3 **EL_35: Time Between SOF and Last Chirp-(J or K)**

The downstream DM6467 DUT Host should begin sending SOFs within 500 µs and not sooner than 100 µs from the transmission of the last chirp-(J or K).

*Figure 17* displays the captured time for this event.

Time between SOF and the last chirp-(J or K): **PASS**

---

**Note:** Measured value: 346 µs.

---

![Figure 17. Time Between First SOF and Last Chirp-(J or K)](image)

---

4.5 **Host Suspend/Resume Timing**

The embedded Host is attached to a known good high-speed device (Flash drive) and finishes up the enumeration process. The DUT Host does no transaction, but periodically generates a SOF packet to the attached high-speed device every 125 µs.

The Host DUT is forced to transition to suspend state via the firmware when needed. The results are that the DM6467 Host DUT stops generating SOF packets.

To exit suspend mode and start the resume process, the DUT Host firmware does the following:

1. Clears the suspend bit
2. Sets the resume bit
3. Leaves the resume bit set for around 20 ms
4. Clears the resume bit

This will end the resume state.

*Figure 14* displays the equipment setup for the suspend and resume tests.
4.5.1 EL_39: Host Suspend Timing

This is the time interval from the end of the last SOF packet issued by the DUT host to when the device attached its full-speed pull-up resistor on D+ (transition to full-speed J-state). This time should be between 3.0 ms and 3.125 ms. No measurement is required as this sequence verifies that the Host supports the suspend state.

The embedded Host is attached to a known good high-speed device (Flash drive) and finishes the enumeration process. The DUT Host does no transaction, but periodically generates a SOF packet to the attached high-speed device every 125 µs. The Host DUT is then forced to transition to suspend state via the Firmware. The results are that the DM6467 Host DUT stops generating SOF packets.

Figure 18 captures the signal capture of SOF from DUT Host vanishing when it enters into suspend mode along with the automatic result published by the TDSUSB2 software.

DUT Host support suspend capability: PASS

---

**Note:** Measured Value (by the TDSUSB2 S/W): 3.04 ms.

---

Figure 18. DUT Host Enters Suspend State

<table>
<thead>
<tr>
<th>Measurement Name</th>
<th>Suspend Time</th>
<th>USB Limits</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Suspend Test</td>
<td>3.07894 ms</td>
<td>3.000000 ms to 3.125000 ms</td>
<td>Pass</td>
</tr>
</tbody>
</table>
4.5.2 EL_41: Host Resume Timing

After resuming a port, the Host must begin sending SOFs within 3 ms of the start of the idle state.

Figure 19 captures the resume signal capture alongside the automatic result generated by the TDSUSB2 software.

DUT Host support resume capability: PASS

---

**Note:** Measured Value: 120.93 µs.

---

![Figure 19. DUT Host Resumes](image)

<table>
<thead>
<tr>
<th>Measurement Name</th>
<th>Resume TIME</th>
<th>USB Limits</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resume Test</td>
<td>120.9346 µs</td>
<td>3.000000 ms</td>
<td>Pass</td>
</tr>
</tbody>
</table>
4.6 **DUT Host Test_J/K, SE0**

A USB 2.0 Specification compliant controller is required for the controller to support mandatory tests (where Test_SE0_NAK, Test_J, and Test_K are members of these tests). A digital multimeter is used to measure the DC voltage level of D+ and D- data lines after placing the controller in one of the test modes mentioned.

Test_SE0 places the controller in high-speed mode and keeps the controller from driving both D+ and D- data lines.

*Figure 20* displays the equipment setup used for DUT Host Test_J, Test_K, and Test_SE0.

---

**Figure 20. Equipment Setup for Downstream Test J/K, SEO_NAK**

4.6.1 **Test_J/ Test_K**

4.6.1.1 **Test_J**

When the D+ is driven high, the output voltage must be 400 mV ± 10% when terminated with precision 45 Ω resistor.

D+ data line DC voltage level: PASS

---

**Note:** Measured value: 0.420 V

D- data line DC voltage level: PASS

---

**Note:** Measured value: 0.004 V

4.6.1.2 **Test_K**

When the D- is driven high, the output voltage must be 400mV ± 10% when terminated with precision 45 Ω resistor.

D- data line DC voltage level: PASS

---

**Note:** Measured value: 0.418 V
D+ data line DC voltage level: PASS

Note: Measured value: 0.004 V

4.6.2 EL_9: Test_SE0

When either D+ and D- are not being driven, the output voltage must be 0V ± 10% when terminated with precision 45 Ω resistors to ground.

D+ data line DC voltage level: PASS

Note: Measured value: 0.002 V

D- data line DC voltage level: PASS

Note: Measured value: 0.002 V

4.7 Legacy USB Compliance Testing

An eye diagram provides an intuitive view of jitter. It is a composite view of all the bit periods of a captured waveform superimposed upon each other. Full-speed and low-speed signal quality tests are good enough to determine that the embedded high-speed Host is capable of interacting with legacy devices that happen to be full- or low-speed in nature.
4.7.1 Full-Speed Downstream Signal Quality Test

For a full-speed downstream signal quality test, it is necessary to cascade four self-powered high-speed hubs and one self-powered full-speed hub with five meters of USB cables. The TDSUSB2F fixture is connected to the embedded Host with a known good five meter USB cable. The self-powered full-speed hub is directly attached (without using a short cable) to the TDSUSB2F fixture on the opposite side at the Tier 1 position. The remaining high-speed hubs are cascaded with five meter cables. A known good full-speed device, in this case a USB 1.1 Flash drive, is connected to the last high-speed hub via a five meter USB cable. Figure 21 displays the equipment setup for a full-speed downstream signal quality test.

To capture the signal quality test, it is necessary to enumerate the attached USB 1.1 device. Since the embedded Host is configured to operate at full-speed after the completion of the enumeration process, it will generate a start of frame packet at the start of every frame. This packet is good enough to perform the full-speed signal quality test.

Figure 21 displays the equipment setup for the full-speed downstream signal quality test.

![Figure 21. Equipment Setup for Full-Speed Downstream Host Signal Quality Testing](image)
Figure 22 displays the screen capture of the waveform plot for the full-speed downstream signal quality testing along with the result summary.

**Figure 22. Full-Speed Downstream Signal Quality Test**
Figure 23 displays the full-speed waveform plot as it is captured by the TDSUSB2F software.
Figure 24 displays the eye diagram for the full-speed downstream Host.

![Eye Diagram](image)

Figure 24. Full-Speed Eye Diagram

Table 7 displays the detailed result for the downstream full-speed signal quality testing.

Table 7. Result Summary for Full-Speed Downstream Host Signal Quality

<table>
<thead>
<tr>
<th>Measurement Name</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Mean</th>
<th>pk-pk</th>
<th>Standard Deviation</th>
<th>RMS</th>
<th>Pop.</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye diagram test</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Pass</td>
</tr>
<tr>
<td>Signal rate</td>
<td>11.88213 Mbps</td>
<td>12.06564 Mbps</td>
<td>11.99616 Mbps</td>
<td>0.0000 bps</td>
<td>44.92540 kbps</td>
<td>11.99807 Mbps</td>
<td>30</td>
<td>Pass</td>
</tr>
<tr>
<td>Crossover voltage</td>
<td>1.480000 V</td>
<td>1.800000 V</td>
<td>1.668596 V</td>
<td>320.0000 mV</td>
<td>80.36886 mV</td>
<td>1.670423 V</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td>EOP width</td>
<td>-</td>
<td>-</td>
<td>165.8684 ns</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>Pass</td>
</tr>
<tr>
<td>Consecutive jitter</td>
<td>-517.1158 ps</td>
<td>602.8842 ps</td>
<td>49.24211 ps</td>
<td>1.120000 ns</td>
<td>285.8456 ps</td>
<td>281.6490 ps</td>
<td>17</td>
<td>Pass</td>
</tr>
<tr>
<td>Paired JK jitter</td>
<td>-543.4921 ps</td>
<td>657.7778 ps</td>
<td>84.28571 ps</td>
<td>1.201270 ns</td>
<td>373.0448 ps</td>
<td>355.5083 ps</td>
<td>7</td>
<td>Pass</td>
</tr>
<tr>
<td>Paired KJ jitter</td>
<td>-480.0000 ps</td>
<td>426.6667 ps</td>
<td>0.0000 s</td>
<td>906.6667 ps</td>
<td>342.5207 ps</td>
<td>320.3988 ps</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>

(1) Additional Information:
- Consecutive jitter range: 53.98 ps to 33.51 ps RMS jitter 16.98 ps
- KJ paired jitter range: -36.29 ps to 42.12 ps RMS jitter 13.10 ps
- JK paired jitter range: -37.51 ps to 27.63 ps RMS jitter 12.75 ps

(2) Because the individual status of the measurements are Pass and performed on Tier 6 (as per USB-IF), the overall result for this test is PASS.
4.7.2 Low-Speed Downstream Signal Quality Test

The best method to capture and analyze low-speed downstream signal quality is to capture both a keep-alive (low-speed EOP) and a packet. The embedded Host is required to either generate a keep-alive or send low-speed traffic once per frame whenever a low-speed device is directly attached to achieve this LOOP GET DESCRIPTOR command is issued from the embedded Host; this is achieved by the Host issuing the GET DESCRIPTOR Command continually. The scope is configured to trigger on the packets transmitted by the Host. The triggering part is sometimes found to be hard depending upon the type of scope and its bandwidth. High bandwidth scopes are not ideal for USB compliance testing.

To achieve a stable trigger, it was necessary on our setup to modify the trigger hold off parameter. For a stable display of repetitive signals, trigger hold off allows you to match the trigger timing with pseudo-random bit streams. It was necessary to play with this setting in order to get a stable trigger for the TDSUSB2 software to measure the signal quality for low-speed downstream configuration. Even though values larger than 1 ms would also work, it is advisable to obtain a hold off value less than one ms that allows stable trigger on multiple packets within a frame.

Figure 25 displays the equipment setup for a low-speed downstream signal quality test.

Figure 25. Equipment Setup for Low-Speed Downstream Host Signal Quality Testing
Figure 26 displays the screen capture of the GET DESCRIPTOR command packet that was used to trigger on to measure the low-speed signal quality testing as well as the summary of the test result.

Figure 26. Low-Speed Downstream Signal Quality Test
Figure 27 displays the low-speed waveform plot as it is captured by the TDSUSB2F software.

![Low-Speed Waveform Plot]

Figure 27. Low-Speed Waveform Plot

Figure 28 displays the eye diagram for low-speed downstream Host.

![Low-Speed Eye Diagram]

Figure 28. Low-Speed Eye Diagram
Table 8 displays the detailed result for the downstream low-speed signal quality testing.

**Table 8. Result Summary for Low-Speed Downstream Host Signal Quality Test**(1)

<table>
<thead>
<tr>
<th>Measurement Name</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Mean</th>
<th>pk-pk</th>
<th>Standard Deviation</th>
<th>RMS</th>
<th>Pop.</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye diagram test</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Pass</td>
</tr>
<tr>
<td>Signal rate</td>
<td>1.489520 Mbps</td>
<td>1.506821 Mbps</td>
<td>1.499897 Mbps</td>
<td>0.0000 bps</td>
<td>3.801528 kbps</td>
<td>1.500058 Mbps</td>
<td>30</td>
<td>Pass</td>
</tr>
<tr>
<td>Crossover voltage</td>
<td>1.493350 V</td>
<td>1.698076 V</td>
<td>1.609784 V</td>
<td>204.7254 mV</td>
<td>58.72229 mV</td>
<td>1.610808 V</td>
<td>23</td>
<td>Pass</td>
</tr>
<tr>
<td>EOP width</td>
<td>-</td>
<td>-</td>
<td>1.336667 µs</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>Pass</td>
</tr>
<tr>
<td>Consecutive jitter</td>
<td>-3.772394 ns</td>
<td>21.20905 ns</td>
<td>117.4377 ns</td>
<td>5.893298 ns</td>
<td>1.339743 ns</td>
<td>1.314198 ns</td>
<td>22</td>
<td>Pass</td>
</tr>
<tr>
<td>Paired JK jitter</td>
<td>-2.460405 ns</td>
<td>2.316324 ns</td>
<td>-95.82838 ps</td>
<td>4.776729 ns</td>
<td>1.672752 ns</td>
<td>1.589802 ns</td>
<td>10</td>
<td>Pass</td>
</tr>
<tr>
<td>Paired KJ jitter</td>
<td>-2.311418 ns</td>
<td>2.188858 ns</td>
<td>4.188858 ns</td>
<td>6.500276 ns</td>
<td>2.103298 ns</td>
<td>2.008471 ns</td>
<td>10</td>
<td>Pass</td>
</tr>
</tbody>
</table>

(1) Additional Information:
- Rising Edge Rate: 19.16116 V/µs (Equivalent rise time = 137.78 ns)
- Falling Edge Rate: 23.03332 V/µs (Equivalent fall time = 114.62 ns)

(2) Because the individual status of the measurements are Pass and performed on Tier 6 (as per USB-IF), the overall result for this test is PASS.

---

**Note:** The actual Tier level for the low-speed device used (mouse) was Tier 1, as is shown on the equipment setup diagram. During the time when the test was performed, the TDSUSB2 software has a bug that required the Tier number to be selected as Tier 6. Table 8 captures the test device position as such. This is a display error and does not comprise the integrity of the test.

---

5 References

- *Host High-Speed Electrical Test Procedure* documentation issued by the USB Implementers Forum ([http://www.usb.org/home](http://www.usb.org/home))
IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in medical/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<table>
<thead>
<tr>
<th>Products</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifiers</td>
<td>Audio</td>
</tr>
<tr>
<td>Data Converters</td>
<td>Automotive</td>
</tr>
<tr>
<td>DSP</td>
<td>Broadband</td>
</tr>
<tr>
<td>Clocks and Timers</td>
<td>Digital Control</td>
</tr>
<tr>
<td>Interface</td>
<td>Medical</td>
</tr>
<tr>
<td>Logic</td>
<td>Military</td>
</tr>
<tr>
<td>Power Mgmt</td>
<td>Optical Networking</td>
</tr>
<tr>
<td>Microcontrollers</td>
<td>Security</td>
</tr>
<tr>
<td>RFID</td>
<td>Telephony</td>
</tr>
<tr>
<td>RF/I and ZigBee® Solutions</td>
<td>Video &amp; Imaging</td>
</tr>
<tr>
<td></td>
<td>Wireless</td>
</tr>
</tbody>
</table>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated