Multiple TMS320DM6467 PCI Interface

ABSTRACT
The DM6467 contains a PCI interface that allows connecting it to a PCI bus in order to communicate with the other peripherals in the system. The DM6467 PCI has a 32-bit data bus. The operating frequency is specified in the device-specific data sheet. This document shows different ways to interface DM6467 devices with the PCI bus.

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1 Interface of DM6467 With Three Slave Devices

Figure 1 shows a system that contains one DM6467 as a Master and three target devices. Target0, Target1 and Target2 are slave devices; they do not have control over the PCI bus. On the DM6467, the PCI_REQ signal is left unconnected and the PCI_GNT signal is grounded so that the DM6467 will always have access to the PCI bus.

![Diagram of Interface of DM6467 With Three Slave Devices](image)

Figure 1. Interface of DM6467 With Three Slave Devices

The DM6467 can access the PCI targets through the master memory-map. The PCI memory space is divided into 32 windows of 8MB fixed size. Each window can map an 8MB of PCI memory to its corresponding DM6467 PCI memory address by using the PCI Address Substitute Register (PCIADDSUB). The address of three target devices can be mapped using any of the 32 PCI Address Substitute Registers (PCIADDSUB0 – PCIADDSUB31) that may be set through the ARM processor.
2 Interface of Three DM6467 Devices Without Arbiter

Figure 2 shows the interface of three DM6467 devices without an arbiter. It is not possible to have two Masters without an arbiter/bridge; out of three DM6467 devices, one should be the master device and the other two are forced to be slave devices only. The PCI_REQ signal of the master is left unconnected and the PCI_GNT signal is grounded. In case of slave devices, the PCI_REQ signal is left unconnected and the PCI_GNT signal is tied high through a pullup resistor. In this scenario, the PCI_GNT signal of all DM6467 are connected to the V\textsubscript{CCP} through the pullup resistor. To take control of the PCI bus, the PCI_GNT signal of selected DM6467 device should be grounded; this is achieved by using the switch or jumper as shown in Figure 2.

![Diagram of interface of three DM6467 devices without arbiter]

Figure 2. Interface of Three DM6467 Without Arbiter

The master DM6467 device can access the PCI slave memory through the master memory map by mapping to the slave DM6467 memory address through the address substitution registers (PCIADDSUB0 – PCIADDSUB31).

The PCI module on the slave DM6467 device provides full visibility to the master into its memory through six sets of PCI Slave Base Address Translation Registers (PCIBAR0TRL-PCIBAR5TRL).
3 Interface of Three DM6467 Devices Through IT8208M Extended PCI Arbiter

Figure 3 shows the interface of three DM6467 devices through the IT8208M extended PCI arbiter. This scenario also applies to other PCI master devices as well. Any of the three DM6467 devices in this configuration can act as either a master or a slave. The IT8208M extended PCI arbiter utilizes one set of PCI_GNT and PCI_REQ signals to support each PCI device connected on a secondary side.

If there is no Host connected to the primary side of the extended PCI arbiter, the PCI_GNT signal is always asserted (connected to the ground) and the PCI_REQ signal is kept floating as shown in Figure 3. The arbiter uses the rotation arbitration scheme to decide the priority of the requesting devices on the secondary side. For more details on the arbiter, see the IT8208M Extended PCI Arbiter Data Sheet that is available at http://www.ti.com/EN/index.aspx. If any one of the DM6467 devices gets the grant signal, it acts as a master and the remaining two DM6467 devices will be slaves.

The master DM6467 device has access to the other slave DM6467 devices through the master memory-map by mapping memory address through the address substitution registers (PCIADDSUB0 – PCIADDSUB31).

The PCI module on the slave DM6467 device provides full visibility for a master device into its memory through six sets of PCI slave base address translation registers (PCIBAR0TRL–PCIBAR5TRL) and the PCI Base Address Mask Registers (PCIBAR0MSK–PCIBAR5MSK).
4 Interface of Three DM6467 Devices, External Host and IT8208M Arbiter

Figure 4 shows the interface of three DM6467 devices and an external host through the IT8208M extended PCI arbiter. The PCI_REQ and PCI_GNT signals from the PCI bus are connected to the primary side of the IT8208M PCI arbiter. The arbiter uses rotation arbitration priority to select the one DM6467 device as a master out of the three DM6467 devices connected.

![Diagram of Interface of Three DM6467 Devices, External Host, and IT8208M Arbiter]

The external Host has access to all DM6467 devices. The DM6467 devices have access to the Host and all other devices.

If any one of the DM6467 devices asserts the request signal, then the arbiter asserts the request signal connected to the PCI bus. Once the arbiter receives the grant signal, it asserts the grant signal of the selected DM6467 device. The selected DM6467 device gets control over the PCI bus.

The master DM6467 device has access to the other slave device memory through the master memory-map by mapping memory address through the address substitution registers (PCIADDSUB0 – PCIADDSUB31).

The PCI module on the slave DM6467 device provides full visibility for a master device into the DM6467 memory through six sets of PCI slave base address translation registers (PCIBAR0TRL–PCIBAR5TRL) and the PCI base address mask registers (PCIBAR0MSK–PCIBAR5MSK).
5 Interface of Five DM6467 Devices Using IT8208M Arbiter

Figure 5 shows the interface of five DM6467 devices with a PCI bus. This connection is achieved by cascading two IT8208M arbiters as shown in the figure. Addition of more master devices in this system can be achieved by cascading one or more IT8208M arbiters. One IT8208M arbiter is required to add two master devices. This scenario also applies to other master devices as well.

![Diagram of Interface of Five DM6467 Devices Using IT8208M Arbiter]

The master DM6467 device has access to the other device memory through the master memory map by mapping memory address through the address substitution registers (PCIADDRSUB0 – PCIADDRSUB31).

The PCI module on the slave DM6467 device provides full visibility for a master device into its memory through six sets of PCI slave base address translation registers (PCIBAR0TRL-PCIBAR5TRL) and the PCI base address mask registers (PCIBAR0MSK-PCIBAR5MSK).

6 References

- **TMS320DM646x DMSoC Peripheral Component Interconnect (PCI) User's Guide** ([SPRUE2](http://www.ti.com))
- PCI Local Bus Specification Revision 2.3 is available at [http://www.pcisig.com/specifications/conventional/](http://www.pcisig.com/specifications/conventional/)
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