

Running a TMS320C64x+ Codec Across TMS320C64x+ Based DSP Platforms

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ABSTRACT

This application report describes the device differences to be taken care for running the C64x+™ video codec software on different C64x+ based platforms. This document assumes that the codec software is developed for the C64x+ digital signal processor (DSP) core. As many TI platforms have a C64x+ DSP, this document gives the details for running the standalone codec software on a C64x+ platform. This document also assumes that the enhanced direct memory access (EDMA3) is available in the system-on-chip (SoC) for data transfers. The devices considered in this document are TMS320DM6446, TMS320DM647/DM648, TMS320DM6437, TMS320DM6467 and OMAP3530, all of which have TMS320C64x+™ DSP cores.

All of the documentation mentioned in this application report are referenced in [Section 4](#) of this document.

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1 Introduction

1.1 Purpose and Scope

Typically, a C64x+ codec is developed and validated on a specific platform (e.g., DM6446). However, this codec can be used on another platform having a C64x+ DSP. This document explains the architectural details to consider before running it on a different platform.

The scope of this document is only for the codec software that runs on the C64x+ DSP.

1.2 Assumptions

It is assumed in this document that the codec has been implemented on a C64x+ DSP platform and runs on a given C64x+ SoC. To illustrate the changes that need to be done for running on different SoC's, an example codec MPEG4 Encoder is used. This is typically applicable to any video codec that is implemented on the C64x+ DSP and does not assume any hardware accelerators. Also, this is mainly to run a standalone codec and needs Code Composer Studio™ software along with the simulator/emulator for the specific platform.

1.3 Target Audience

All individuals involved in the development of video and image application software on the C64x+ DSP platforms. This is also very handy for field application engineers running a C64x+ library on different C64x+ platforms.

2 Background

Figure 1 shows the basic codec package, which has a codec library that contains sample test application, user's guide, data sheet, etc. The codec library considered here is a C64x+ library. The codec is developed and validated on a specific platform having C64x+ DSP core (this information is included in the release notes). The codec's are supplied with a standalone package or real-time software components (RTSC) package. The standalone package has a sample application that contains the Code Composer Studio Project and sample test files, which are configured to run on a specific platform. For the RTSC package, the sample app is included in the app folder (e.g, for MPEG4 encoder, the sample app is available at packages\ti\sd0\codecs\mpeg4enc\app folder).

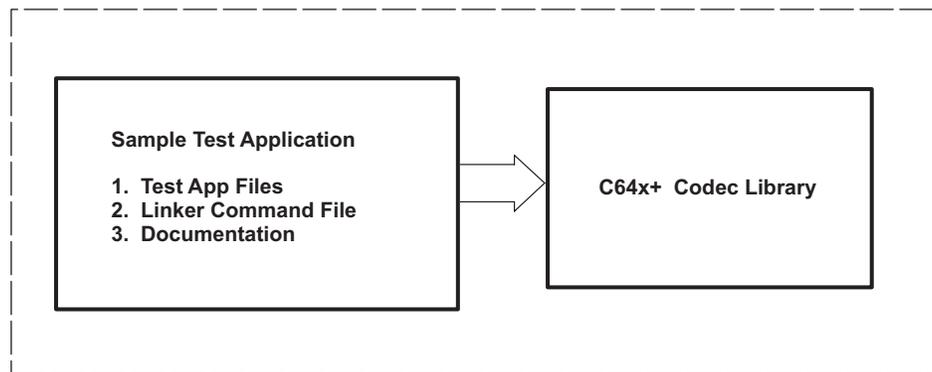


Figure 1. Codec Package

Ideally, the C64x+ library can be used for any platform having a C64x+ DSP. But sometimes, there will be changes required in the library/test application to make it run on a given C64x+ based platform depending on the device. The following section describes the SoC features that need to be considered before running the codec on a given C64x+ platform. The sample application needs SoC details that are discussed below so that it can run on an EVM or software development platform (SDP) that has C64x+ DSP.

3 Device Differences to Be Considered

3.1 L1 and L2 Memory Considerations

The video performance sensitive data (like macro block data) is often executed from L1 or L2 memories. This memory is requested by the codec through the IALG interface. The algAlloc function returns the request for memory type of IALG_DARAM0 with a specified size through a memTab [memory table], The application needs to allocate this on-chip memory (L1/L2). L1 memory is preferable due to performance reasons, if the required size is available in L1. For the given SoC, the L1 and L2 memory sizes is important to understand.

For performance reasons, the C64x+ video codec designs assume a specific configuration for L1D RAM size. If this is not fulfilled for a given SoC (i.e., the SoC does not have the required L1/L2 memories specified in the codec data sheet), it may still be possible to run the codec by allocating this memory in some other memory space (e.g., allocating it in L2 SRAM or DDR if l2 is not sufficient). This makes sure that the codec is functional, but the performance of the codec might need to be benchmarked with this change, since the performance might drop due to increased latencies.

The data sheet of a codec mentions the memory requirements and the assumptions based on which performance (L1/L2 sizes, clock frequencies, etc.) of the codec is measured and the platform on which the performance was benchmarked. The sample application has a function that configures the L1/L2 cache and RAM sizes. [Figure 2](#) shows the snapshot of this function.

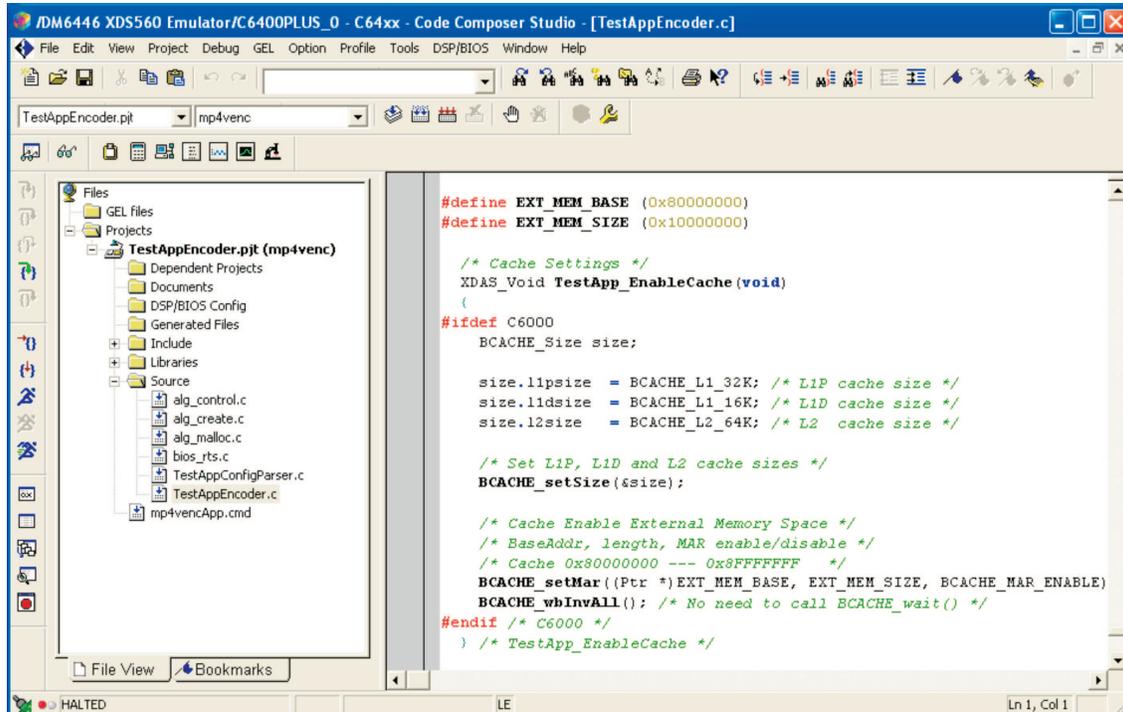


Figure 2. Setting the Device Configuration for L1/L2

[Table 1](#) gives the L1/L2 memory sizes for the different platforms considered in this document.

Table 1. L1 and L2 Memory Sizes

	DM6446	DM6437	DM648	DM647	DM6467	OMAP3530
L1D Size	80K-Byte L1D Data RAM/Cache	80K-Byte L1D Data RAM/Cache	32K-Byte L1D Data RAM/Cache	32K-Byte L1D Data RAM/Cache	32K-Byte L1D Data RAM/Cache	80K-Byte L1D Data RAM/Cache
L2 Size	64K-Byte L2 Unified Mapped RAM/Cache	128K-Byte L2 Unified Mapped RAM/Cache	512K-Byte L2 Unified Mapped RAM/Cache	256K-Byte L2 Unified Mapped RAM/Cache	128K-Byte L2 Unified Mapped RAM/Cache	64K-Byte L2 Unified Mapped RAM/Cache

Note that except for DM6446, DM6437 and OMAP3530, other devices have L1D memory of just 32KB. Taking the example of the MPEG4 Encoder, the C64x+ MPEG4 Encoder needs 52KB of L1D RAM. If we need to run this in DM6467, which has just 32KB of L1D RAM, we need to use L2 RAM instead. DM6437/DM6446 can be configured to have 64KB of internal memory, so the L1D memory is not an issue for these platforms.

Note that this might have some performance implications (placing the data in L2 instead of L1), so the performance benchmarking needs to be done with this change in memory.

So, if the L1/L2 configuration is different from what is expected by the codec (as per the data sheet), then there is no change required in the library, only the L1/L2 configuration need to be changed in the test application.

3.2 L1/L2 Base addresses

The memory map of the platform could be different. To run the codec, the memory map needs to be provided for linking, through the linker command file. Figure 3 is a snapshot of the linker command file that is provided with the standalone sample application.

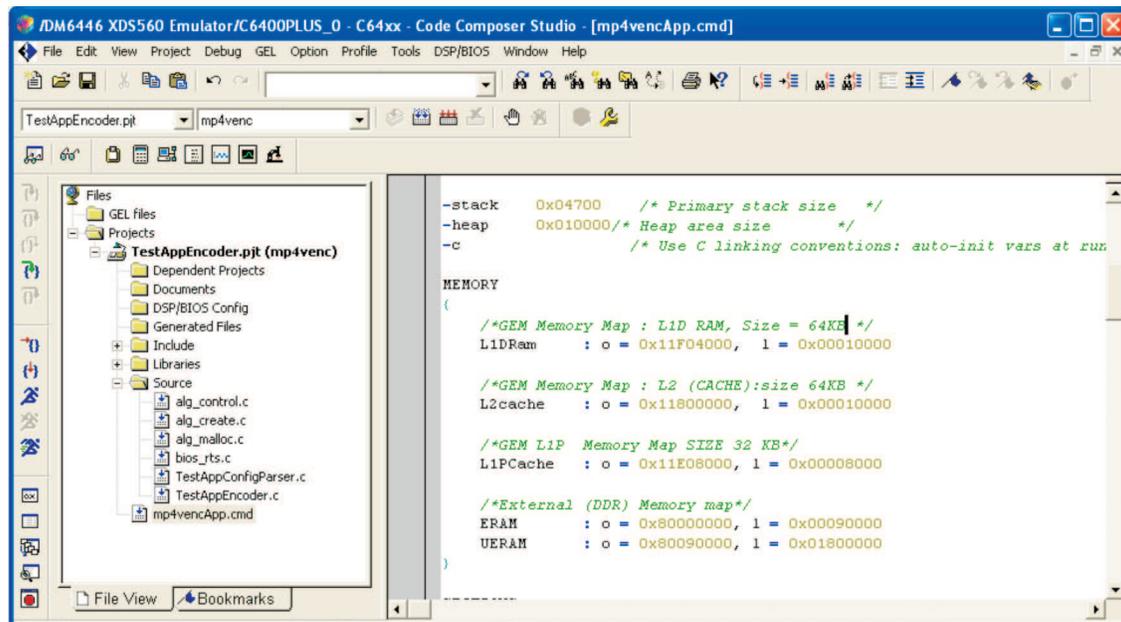


Figure 3. Linker Command File

The L1 and L2 base addresses can vary from one SoC to another; to run a codec on a given SoC, you need to know the start addresses of the memories. This information is summarized in Table 2.

Table 2. L1 and L2 Memory Base Addresses

	DM6446	DM6437	DM648	DM6467	OMAP3530
L1D base address	0x11F0 4000	0x10F0 4000	0x00F0 0000	0x11F0 0000	0x10F0 4000
L2 base address	0x1180 0000	0x1080 0000	0x00A0 0000	0x1181 8000	0x1080 0000

If the memory map is different, there is no change required in the library, only the L1/L2 addresses need to be changed in the test application linker command file.

3.3 EDMA features: TC's and QDMA Base Address

The MPEG4 encoder uses QDMA for all data transfers. QDMA requires many register settings for configuring transfers. The EDMA configuration base address varies for different platforms.

The base addresses for different platforms under consideration are provided in Table 3.

Table 3. EDMA Features

	DM6446	DM6437	DM648	DM6467	OMAP3530
QDMA config base address	0x01C0 0000	0x01C0 0000	0x02A0 0000	0x01C0 0000	0x01C0 0000
Number of TC's	2	3	4	4	2

Table 3. EDMA Features (continued)

	DM6446	DM6437	DM648	DM6467	OMAP3530
Number of QDMA channels	8	8	8	8	8

Also, the number of transfer controllers (TC's) could be different. [Table 3](#) also gives the TC's for different SoC's.

At present, the QDMA base address is chosen during build time, so if there is a change in the config base address (e.g., DM6446 to DM648) then the codec library needs to be rebuilt. It is possible to abstract this using the framework, (e.g., by defining the resource manager API's to take care of the EDMA base address), but such a framework is not available in some of the legacy codecs.

Another factor that affects the system performance is the number of TC's. This may not affect the standalone codec performance in the presence of other system traffic; but in the presence of other system traffic, the number of TC's can affect the overall performance of the system.

The number of QDMA channels available in these SoC's is 8. This is the upper bound on the channel usage for the codec (e.g., MPEG4 encoder uses 4 QDMA channels).

3.4 DDR Base Address

Due to differences in the memory maps, the DDR base address can change across platforms. This is needed for memory allocation for data and code. In [Figure 2](#), the linker command file specifies the DDR base address sections. This need to be updated based on the SoC's memory map. [Table 4](#) gives the address for the SoC's under consideration.

Table 4. DDR Base addresses

	DM6446	DM6437	DM648	DM6467	OMAP3530
DDR Address	0x8000 0000	0x8000 0000	0xE000 0000	0x8000 0000	0x8000 0000

If the DDR address is different, then there is no change required in the library; only the test application linker command file needs to be updated with the correct address.

3.5 Other Aspects

In addition to the architectural specifics explained above, there are some other compatibility aspects that need to be considered before running the codec. Some examples are given below that are very specific to the SoC; some can have software workarounds.

3.5.1 Color Formats

The DM6446 platform supports YUV 422ILE format, but the YUV format supported in DM6467 is YUV 420 semi planar. The MPEG4 encoder on C64x+ supports YUV420 planar and YUV422ILE. To run this on DM6467, some format conversion are needed. Similarly, the native colour format for DM648 is YUV 422 planar.

3.5.2 Performance

The performance or the maximum resolution possible on a given platform depends on the clock frequency of the DSP, the L1/L2 configurations, the EMIF/DDR bandwidth available, etc. Even though taking care of the device aspects makes the codec functional on a given platform, the performance has to be benchmarked separately.

4 References

- *TMS320DM6467 Digital Media System-on-Chip Data Manual* ([SPRS403](#))
- *TMS320DM6437 Digital Media Processor Data Manual* ([SPRS345](#))
- *TMS320DM6446 Digital Media System-on-Chip Data Manual* ([SPRS283](#))
- *TMS320DM647/TMS320DM648 Digital Media Processor Data Manual* ([SPRS372](#))
- *OMAP3530/25 Applications Processor Data Manual* ([SPRS507](#))

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