Optimized system-on-chip processor, DACs and ADCs for defense digitizer systems

This TI Design is for developers currently leveraging an FPGA or ASIC in their product solution with high-speed ADCs and DACs. Significant time savings are achieved by pre-integrating hardware and software for both the processor and ADC/DAC. Additionally, this solution saves cost, power and size versus a traditional FPGA-based solution. The design includes the first widely available processor integrating a JESD204B interface and Digital Front End (DFE), the 66AK2L06 SoC. Connecting the ADC12J4000 and DAC38J84 to the 66AK2L06 processor provides an efficient solution for test and measurement and defense applications.

Features
- Easy integration of signal processor to data converters over JESD204B
- Multichannel sampling rates up to 368Msps with 150MHz of processing bandwidth
- DFE processing for filtering, down-sampling or up-sampling
- Wideband sampling with JESD204B attached signal processing solution including DSP, ADC and DAC boards, demo software, configuration GUIs and getting started guide
- A robust demonstration and development platform including three EVMs, a deterministic latency card, schematic, BOM, user guide, benchmarks, software and demos
- New TI Design for synthetic aperture radar (SAR) applications coming soon (shown to the right)

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TI products in the TI Design

**66AK2L06 system-on-chip**

- Integrated DFE technology with programmable up/down sampling and filtering
- Latency optimization using 2× FFT co-processors up to 8K-points and >80dB SNR, 35 GFLOPS @ 8K
- Four TMS320C66x DSP cores with fixed- and floating-point processing providing 153.6GMACS and 76.8GFLOPS
- Two ARM® Cortex®-A15 RISC cores providing 8400 DMIPS
- Floating-point FFT with TMS320C66x DSP – any size FFT, >300dB SNR, 4GFLOPS @8K

**Software Programmable Digital Front End (DFE)**

- **Frequency Plan**
  - Max sample rate: 368Msps TX and 368Msps RX complex
  - 330MHz instantaneous and 150MHz occupied signal bandwidth

- **Input / Output**
  - 4× JESD204B lanes, 7.4Gbps each
  - 4RX and 4TX streams
  - 4 streams and 4/8/12 DDUC channels on each stream
  - 18-bit data path resolution

- **Performance**
  - > 90dB stopband performance
  - Programmable FIR with 399 taps maximum tap length
  - 1–16 integer decimation rates
  - Fractional decimation using resampling

**DAC38J84: Quad 16-bit 2.5-GSps DAC**

- Low power: 450 mW/ch @ 2.5GSps
- JESD204B, 8 lanes 12.5-Gbps interface
- 10×10mm, 0.8-mm pitch BGA

**ADC12J4000: 12-bit 4-GSps ADC**

- RF sampling to > 3GHz
- JESD204B, 8 lanes 10-Gbps interface

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