TPS65910 User Guide For OMAP3 Family of Processor

This document can be used as a reference for connectivity between the TPS65910 power-management integrated circuit (PMIC) and the OMAP3 family (OMAP35xx/OMAP36xx/DM37xx/AM37xx/AM35xx, except AM3517 and AM3505).

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1 Introduction
This document can be used as a reference for connectivity between the TPS65910 PMIC and OMAP3 family (OMAP35xx/OMAP36xx/DM37xx/AM37xx/AM35xx, except AM3517 and AM3505). For information about the power resources or the functionality of the device, see the device data sheet.

2 Platform Connection
Figure 1 shows the power supply connections between the TPS65910 and OMAP3.
Figure 1. OMAP3 Power Supply Connections With TPS65910

NOTE:

- This diagram does not apply to the AM3517 and AM3505 processors.
- The power-up sequence for OMAP core power rails (for VDD_CORE and VDD_MPU) is swapped. However, this does not affect OMAP power up. OMAP powers up without any issues.
- The reason for swapping the supply domains is that, based on experimentation, VDD1 is less board sensitive than VDD2 under heavy load (> 1200 mA) conditions, so it is recommended to use VDD1 for handling the heaviest load condition of the application, thus easing the board routing.
At power up, the maximum current capability (default setting) of the DCDC converters is as follows:

- VIO(max) = 500 mA
- VDD1(max) = 1000 mA
- VDD2(max) = 1000 mA

To have the maximum current capability, the user must program the following register bits:

- VIO_REG[ILMAX] = b01 for 1 A
- VDD1_REG[ILMAX] = b1 for 1.5 A
- VDD2_REG[ILMAX] = b1 for 1.5 A

3 Power-Up Sequencing

3.1 Power-Up Sequence for OMAP3 Family

This section describes the power-up sequence for the TPS65910 power rails that matches the power-up sequence for the processors named in Section 1, Introduction. To power up the system, the user should press and release the PWRON switch (generating a negative pulse) on the platform (see Figure 2.)

Table 1 describes the power-up sequence for TPS65910 where BOOT0 = 1 and BOOT1 = 0. This sequence is aligned for the family of processors named in Section 1, Introduction.

### Table 1. Power-Up Sequence for TPS65910 (BOOT0 = 1 and BOOT1 = 0)

<table>
<thead>
<tr>
<th>Power Domain</th>
<th>Pin Name</th>
<th>Voltage (V)</th>
<th>Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>IO CORE</td>
<td>VDDS_WKUP_BGVDDS_SRAMVDDS_MEMVDDS</td>
<td>1.8</td>
<td>1</td>
</tr>
<tr>
<td>PLL</td>
<td>VDDS_DPLL_DLLVDDS_DPLL_PER</td>
<td>1.8</td>
<td>2</td>
</tr>
<tr>
<td>Core</td>
<td>VDD_CORE</td>
<td>1.2</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>VDD_MPU</td>
<td>1.2</td>
<td>4</td>
</tr>
</tbody>
</table>

Event:

- 1 = PWRON button press falling edge
- 2 = Valid press after debounce
- 3 = First step of power-up sequence available for DCDC, LDO activation. Time slot 0 is for internal use.

Note: PWRON press must be maintained until PWHRHOLD acknowledge, or, for shorter PWRON press, PWHRHOLD must go high within 984 ms of valid PWRON press (event 2). To ensure this, PWHRHOLD is tied to VIO.
For correct power on of the device, the PWRHOLD signal should be high after PWRON is pressed. For an OMAP3 configuration, the PWRHOLD signal on TPS65910 is connected to VIO. PWRHOLD transitions to high when VIO powers up.

Table 2 describes the power domain mapping for the TPS65910 and OMAP35xx/AM35xx processors.

### Table 2. Power Domain Mapping

<table>
<thead>
<tr>
<th>TPS65910 Power Resource</th>
<th>Imax (mA)</th>
<th>OMAP35xx/AM35xx Power Domain</th>
<th>Imax (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIO</td>
<td>1000</td>
<td>Vdds_io</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td>vdds_mem</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td></td>
<td>vdds_sram</td>
<td>41</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Vdda_wkup_bg_bb</td>
<td>5</td>
</tr>
<tr>
<td>VPLL</td>
<td>50</td>
<td>Vdda_dplls_dll</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Vdda_dpll_per</td>
<td>10</td>
</tr>
<tr>
<td>VDD1</td>
<td>1500</td>
<td>Vdd_dmpu</td>
<td>1200</td>
</tr>
<tr>
<td>VDD2</td>
<td>1500</td>
<td>Vdd_core</td>
<td>300</td>
</tr>
<tr>
<td>VDAC</td>
<td>150</td>
<td>Vdda_dac</td>
<td>60</td>
</tr>
<tr>
<td>VAUX2</td>
<td>150</td>
<td>Vdds_mmc1</td>
<td>20</td>
</tr>
</tbody>
</table>

Table 3 lists the EEPROM configuration of the TPS65910.

### Table 3. EEPROM Configuration of TPS65910

<table>
<thead>
<tr>
<th>Register</th>
<th>Bit</th>
<th>Description</th>
<th>TPS65910 BOOT0/1</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD1_OP_REG</td>
<td>SEL</td>
<td>VDD1 voltage level selection for boot</td>
<td>1.2 V</td>
</tr>
<tr>
<td>VDD1_REG</td>
<td>VGAIN_SEL</td>
<td>VDD1 gain selection (x1 or x2)</td>
<td>x1</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>VDD1 time slot selection</td>
<td>3</td>
</tr>
<tr>
<td>DCCDCTRL_REG</td>
<td>VDD1_PSKIP</td>
<td>VDD1 pulse skip mode enable</td>
<td>Skip enabled</td>
</tr>
<tr>
<td>VDD2_OP_REG/VDD2_SR_REG</td>
<td>SEL</td>
<td>VDD2 voltage level selection for boot</td>
<td>1.2 V</td>
</tr>
<tr>
<td>VDD2_REG</td>
<td>VGAIN_SEL</td>
<td>VDD2 gain selection (x1 or x3)</td>
<td>x1</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>VDD2 time slot selection</td>
<td>4</td>
</tr>
<tr>
<td>DCCDCTRL_REG</td>
<td>VDD2_PSKIP</td>
<td>VDD2 pulse skip mode enable</td>
<td>Skip enabled</td>
</tr>
<tr>
<td>VIO_REG</td>
<td>SEL</td>
<td>VIO voltage selection</td>
<td>1.8 V</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>VIO time slot selection</td>
<td>1</td>
</tr>
<tr>
<td>DCCDCTRL_REG</td>
<td>VIO_PSKIP</td>
<td>VIO pulse skip mode enable</td>
<td>Skip enabled</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>VDD3 time slot</td>
<td>OFF</td>
</tr>
<tr>
<td>VDIG1_REG</td>
<td>SEL</td>
<td>LDO voltage selection</td>
<td>1.2 V</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>LDO time slot</td>
<td>OFF</td>
</tr>
<tr>
<td>VDIG2_REG</td>
<td>SEL</td>
<td>LDO voltage selection</td>
<td>1.0 V</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>LDO time slot</td>
<td>OFF</td>
</tr>
<tr>
<td>VDAC_REG</td>
<td>SEL</td>
<td>LDO voltage selection</td>
<td>1.8 V</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>LDO time slot</td>
<td>OFF</td>
</tr>
<tr>
<td>VPLL_REG</td>
<td>SEL</td>
<td>LDO voltage selection</td>
<td>1.8 V</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>LDO time slot</td>
<td>2</td>
</tr>
<tr>
<td>VAUX1_REG</td>
<td>SEL</td>
<td>LDO voltage selection</td>
<td>1.8 V</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>LDO time slot</td>
<td>OFF</td>
</tr>
<tr>
<td>VMIMC_REG</td>
<td>SEL</td>
<td>LDO voltage selection</td>
<td>1.8 V</td>
</tr>
<tr>
<td>EEPROM</td>
<td></td>
<td>LDO time slot</td>
<td>OFF</td>
</tr>
</tbody>
</table>
### 4 Getting Started With TPS65910 and Associated Processor

#### 4.1 First Initialization

**4.1.1 I/O Polarity/Muxing Configuration**

Program DEVCTRL2_REG.SLEEPSIG_POL = 0 to set the polarity of the SLEEP signal for active low. The software configuration allows specific power resources to enter low consumption state when the SLEEP signal goes low.

Set DEVCTRL_REG.DEV_SLP = 1 to allow sleep transition when requested.

Update the GPIO0 configuration (GPIO0_REG) as desired.

**4.1.2 Define Wakeup/Interrupt Event (SLEEP or OFF)**

Select the appropriate bits in the INT_MSK_REG and INT_MSK2_REG registers to activate an interrupt to the processor on the INT1 line.

**4.1.3 Backup Battery Configuration**

If a backup battery is used, set BBCH_REG[BBCHEN] to 1 to enable backup battery charging. Maximum voltage can be set based on backup battery specifications (BBSEL).
4.1.4 DCDC and Voltage Scaling Resource Configuration

**NOTE:** If the SmartReflex™ interface is not used for voltage scaling (power saving), then these pins can be used to control the power resources.

Configure two operating voltages for DCDC1 and DCDC2:
- \( VDDx\_OP\_REG\_SEL = \) roof voltage (Enx ball High)
- \( VDDx\_SR\_REG\_SEL = \) floor voltage (Enx ball Low)

Assign control of DCDC1 to SCLSR_EN1 and DCDC2 to SCLSR_EN2:
- Set \( EN1\_SMPS\_ASS\_REG\_VDD1\_EN1 = 1 \)
- Set \( EN2\_SMPS\_ASS\_REG\_VDD2\_EN2 = 1 \)
- Set \( SLEEP\_KEEP\_RES\_ON\_REG\_VDD2\_KEEPON = 1 \) (allow low-power mode).
- Set \( SLEEP\_KEEP\_RES\_ON\_REG\_VDD1\_KEEPON = 1 \) (allow low-power mode).

4.1.5 Sleep Platform Configuration

Configure the state of the LDOs when the SLEEP signal is used. By default, all resources go to SLEEP state. In SLEEP state the LDO voltage is maintained but transient and load capability is reduced.

Resources that provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG register.

Resources that can be set off in SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG register.

4.2 Event Management Through Interrupt

4.2.1 INT_STS_REG.VMBHI_IT

INT_STS_REG.VMBHI_IT indicates that the supply (VBAT) is connected. Leaving BACKUP or NO SUPPLY state, the system must be initialized (see Section 4.1, First Initialization).

4.2.2 INT_STS_REG.PWRON_IT

INT_STS_REG.PWRON_IT is triggered by pressing the PWRON button. If the device is in OFF or SLEEP state, then this interrupt acts as a wake-up event and resources are reinitialized.

4.2.3 INT_STS_REG.PWRON_LP_IT

INT_STS_REG.PWRON_LP_IT is the PWRON long-press interrupt and is generated when the PWRON switch is pressed for 6 seconds. The application processor can decide to acknowledge the interrupt. If this interrupt is not acknowledged in the following 2 seconds, the device interprets this as a power-down event.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of the die is reaching the limit. Software must decrease power consumption before automatic shutdown.

4.2.5 INT_STS_REG.VMBDCH_IT

INT_STS_REG.VMBDCH_IT indicates that the input supply is low and the processor must prepare a shutdown to avoid losing data.

This interrupt is linked to VBAT but does not apply in a system where PMIC is connected to 5-V rails and not connected directly to VBAT.
4.2.6 INT_STS2_REG.GPIO_R/F_IT

INT_STS2_REG.GPIO_R/F_IT is the GPIO interrupt event and can be used to wake up the device from SLEEP state. This can be an interrupt coming from any peripheral or similar device. This wake-up event is not valid for a transition from OFF state.

4.2.7 INT_STS_REG.RTC_ALARM_IT

INT_STS_REG.RTC_ALARM_IT is triggered when the RTC alarm set time is reached.
## 5 Revision History

### Table 4. Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Literature Number</th>
<th>Date</th>
<th>Notes</th>
</tr>
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<tbody>
<tr>
<td>*</td>
<td>SWCU078</td>
<td>December 2010</td>
<td>See (1).</td>
</tr>
<tr>
<td>A</td>
<td>SWCU078A</td>
<td>July 2011</td>
<td>See (2).</td>
</tr>
</tbody>
</table>

(1) TPS65910 User Guide For OMAP3 Family of Processor, SWCU071 - Initial release.
(2) TPS65910 User Guide For OMAP3 Family of Processor, and TMS320C674x, SWCU071A:

- Update Figure 1: Fix inductors on DCDC1 and DCDC2, change from 2.2 nH to 2.2 uH.
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