Shelf-Life Evaluation of Nickel/Palladium Lead Finish for Integrated Circuits

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Abstract

The integrated-circuit (IC) industry is converting to nickel/palladium (Ni/Pd)-finished leadframes for assembly of ICs. To date, Texas Instruments (TI™) has over 20 billion Ni/Pd ICs in the field. Users of IC components need to know the maximum length of time that components can be stored before being soldered. The goal of this study was to predict shelf life of Ni/Pd-finished components by exposing a sample set to a controlled environment with known age-acceleration factors. Ni/Pd-finished components were exposed to a Battelle Class 2 environment both in and without their normal packing materials. Results show that Ni/Pd-finished ICs stored in tubes, trays, or tape-and-reel packing material pass solderability testing after 96 hours of exposure to the Class 2 environment. This length of exposure correlates to eight years in an uncontrolled indoor environment.

Introduction

This study was undertaken to determine the shelf life of electronic components that have Ni/Pd-finished leads instead of the more conventional tin/lead (Sn/Pb). TI introduced the Ni/Pd plating finish for leadframes used in plastic-package ICs in 1989. There are more than 20 billion ICs with Ni/Pd-finished leads now in the field.

Uncontrolled assessments of shelf life measured by dip-and-look or surface-mount solderability testing have been performed by various groups within TI. The results have shown no degradation in solderability after two years of shelf storage of the components. This study looks at shelf-life solderability in a controlled fashion, using standardized environmental test conditions for accelerating aging.

The need for an Ni/Pd lead finish is due in part to the desire to remove lead (Pb) from electronics components and end products. Use of Ni/Pd preplated leadframes allows the entire Sn/Pb solder-plating operation and associated chemicals to be removed from the IC assembly process. Additional benefits of using Ni/Pd-finished leadframes include elimination of solder flakes/burrs, improved lead-tip planarity versus Sn/Pb, and a reduction in IC manufacturing cycle time.[1,2,3]

Background

One method used to examine shelf life, as measured by solderability, is to expose the subject devices to a known, controlled atmosphere that accelerates the effects from normal environmental exposure. This is a useful tool if reasonable care is taken to select a test method and conditions so that the time-acceleration factor is valid and the failure mechanism is consistent with actual conditions.

Steam aging of the IC units prior to solderability testing is a common method used to accelerate IC aging, and is used by many manufacturing operations. Previous work has shown that when Pd-finished components are exposed to a steam age environment, mold resins may be deposited onto the surface of the palladium. These deposits inhibit dissolution of the palladium during solderability testing.[4] In contrast, for Sn/Pb-finished leads, the soldering mechanism used is a reflowing of the solder on the lead. If there are contaminants on the surface from the steam aging procedure, then they simply are floated off the surface of the solder. This artifact of the steam aging process does not correlate with actual shelf storage conditions for Ni/Pd-plated leads. In the soldering process, the palladium dissolves and the solder wets to the underlying nickel. Steam age exposure prior to solderability testing has proven to be a nonreproducible method of predicting solderability performance of Ni/Pd-finished components. For this shelf-life study, it was decided to use an acceleration method with known acceleration factors, and with a mechanism more like that seen in actual practice.

Procedure

To study the shelf life and post-storage solderability of surface-mount ICs with an Ni/Pd finish, a Battelle Class 2 mixed flowing-gas environment was selected. This test has been well characterized by previous work and represents a slightly corrosive indoor atmosphere, where the gas concentrations and humidity levels result in pore corrosion of plated-copper (Cu) materials, but do not promote copper creep corrosion.[5,6] Class 2 environments generally are described as indoor environments having no humidity control.

This test is conducted in a mixed flowing-gas chamber designed to the schematic shown in Figure 1; the conditions are shown in Table 1 and described in ASTM B827-92.[7]

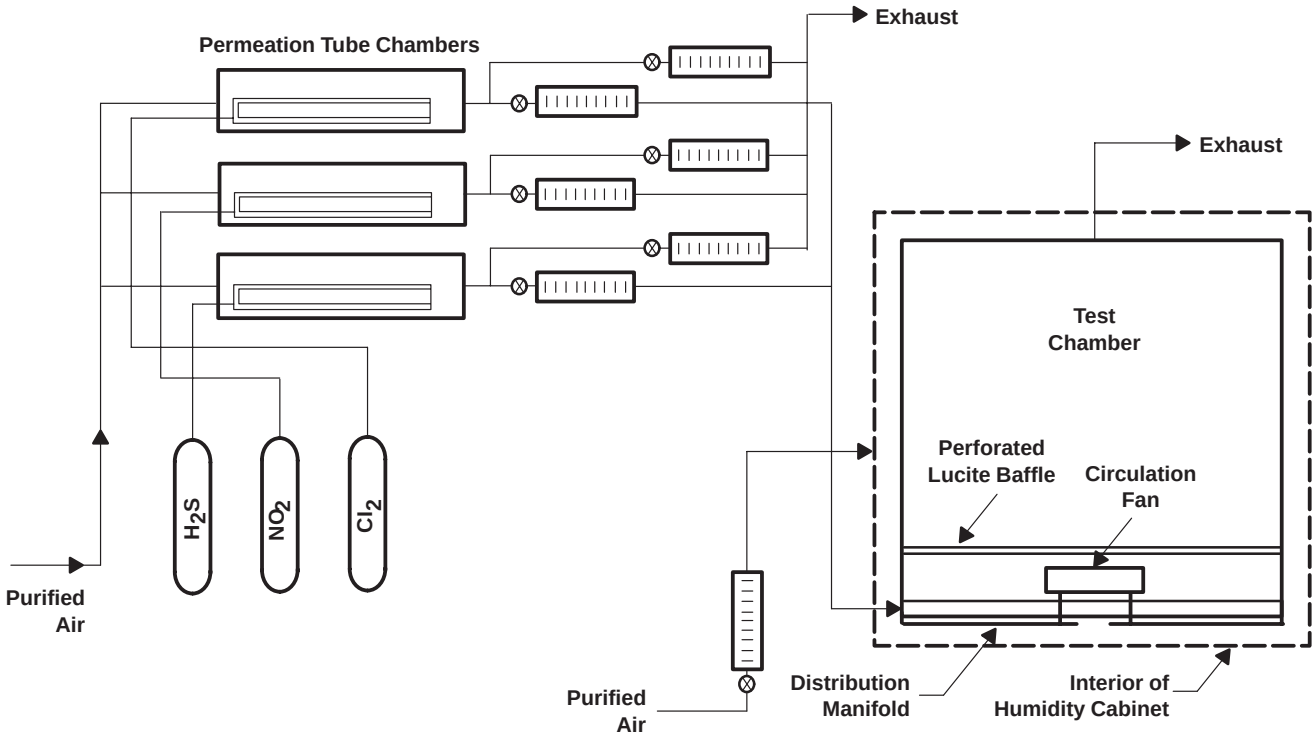

Figure 1. Schematic of Mixed Flowing-Gas Chamber

Concentrations of gases in the chamber are precisely controlled. It is important to include standard reactivity coupons, along with the test specimens. This allows measurements of mass gain, film thickness, and percent oxides on the coupons, so that proper test conditions are maintained, and to facilitate verification of acceleration factors.[8,9,10]

Subject surface-mount IC devices, assembled with Ni/Pd-plated Cu base-metal leadframes, were placed in the chamber, both unprotected and partially protected from the gas flow. Unprotected samples were totally exposed to the mixed flowing-gas environment. Additional samples from the same lots were left in the typical (opened) packing used in product shipment. Small-outline ICs (SOICs) were left in shipping tubes and in tape and reel. Quad flatpack (QFP) devices were in a stack of plastic shipping trays. None of these parts was in an antistatic bag or cardboard shipping/packing box.

The attenuation effects of the packing materials (tubes, trays, tape and reel) were found to be significant. Abbott (Battelle) has stated that the attenuation by packing materials perhaps is the major reason that electronic components can perform reliably in field environments.[11] Virtually any type of packing provides some degree of environmental attenuation compared to free surface exposure. Although it is beyond the scope of this application report, one could speculate that the kinetics are controlled by Fick's third law, since the reactive species are in the gas phase, and gas concentration at the metal surface controls the corrosion rate. This can be intuitively contrasted with the mechanism of the steam age test, which seems not to mimic actual storage conditions.

Device samples and reactivity coupons were removed from the chamber at intervals (12, 24, 36, 48, 72, and 96 hours). Visual microscopic examination was used to ‘‘grade” the visual effects of the gas exposure, followed by solderability testing. Measurement of the reactivity coupons was done to confirm reaction rates and to determine the appropriate acceleration factor.

Table 1. ASTM B827-92 Standard Practice for Conducting Mixed Flowing-Gas Environmental Test

CLASS 2 MIXED-GAS CONDITIONS	
Cl_2 concentration	10 ± 3 ppb
NO_2 concentration	200 ± 50 ppb
H_2S concentration	10 ± 5 ppb
Relative humidity	70 + 3%/–0%
Temperature	30 ± 2°C
Chamber volume change	3 to 6 times per hour
Acceleration factor	400–1000

Assessment Procedures

Visual Examination – Parts from each of the cells of the matrix were examined under a microscope at up to 40× magnification. The parts were graded subjectively as to the amount of corrosion products seen on the surface of the leads. An arbitrary scale of 0 to 5 was used to grade the amount of corrosion, with 0 being no corrosion and 5 being severe corrosion.

Analysis of Corrosion Products – The composition of corrosion products on the surface of representative parts was analyzed by SEM/EDAX. This was done for heavily corroded parts and corrosion-free parts.

Surface-Mount Solderability Test – Solderability of the components exposed to the Class 2 environment was judged with the Surface-Mount Solderability Test per ANSI/EIA-638.[12] This test method simulates the actual reflow environment that surface-mount devices encounter in a board-mount application. Testing has shown that this method is more appropriate for surface-mount devices than the traditional ‘‘dip-and-look” method.

This test procedure begins with screening solder paste onto a ceramic plate (0.035 inch thick) using a solder stencil (see Figure 2). The paste print must match the pattern of the leads to be tested. The devices to be tested are then placed onto the solder paste print (see Figure 3).

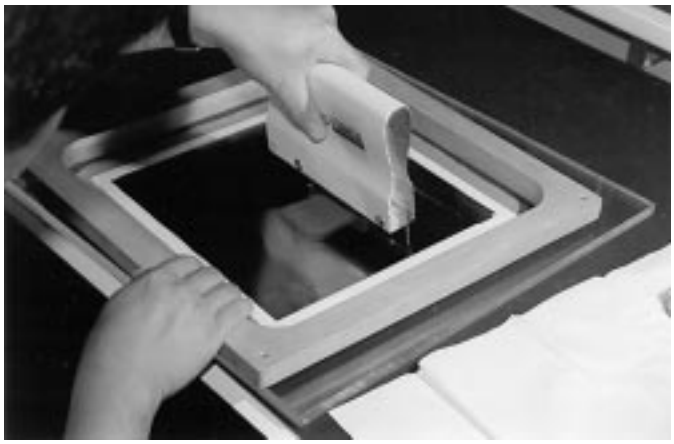

Figure 2. Solder Is Screened Onto the Ceramic Substrate

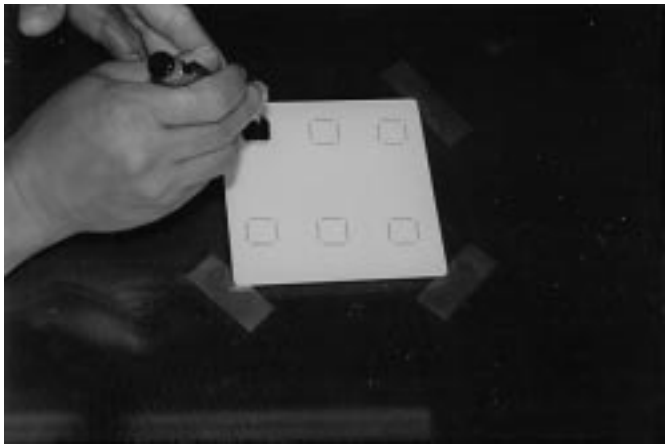

Figure 3. Devices Are Placed Onto the Solder Paste Print

The ceramic substrate is processed through a reflow cycle and allowed to cool. After reflow, the units are removed from the ceramic and inspected. The advantage of this test method is that the IC devices are subjected to the same reflow environment experienced in actual processing and use of a ceramic substrate allows for inspection of the surface to be soldered.

The accept/reject criteria given in ANSI/EIA-638 indicates that ‘‘all terminations shall exhibit a continuous solder coating, free from defects for a minimum of 95% of the critical surface area of any individual termination.” For the surface-mount packages tested, the critical area is defined as the underside of the leads, plus both sides of the leads, up to 1× the lead thickness.

Results

Results of the visual inspection (Table 2) indicate that all of the devices left in the normal shipping materials showed no visible corrosion products. The parts that were completely exposed to the mixed flowing gas showed a time dependency in which the amount of corrosion tracked well with exposure to the atmosphere.

Table 2. Visual Classification of ICs After Exposure to the Class 2 Environment

CLASS 2 EXPOSURE HOURS	GROUP 1 20-PIN SOIC OUTSIDE OF PACKING	GROUP 2 20-PIN SOIC TUBES	GROUP 3 20-PIN SOIC TAPE AND REEL	GROUP 4 80-PIN TQFP OUTSIDE OF PACKING	GROUP 5 80-PIN TQFP TRAY
12	1	0	0	2	0
24	1.5	0	0	2	0
36	3	0	0	2	0
48	4	0	0	3 – bottom 1 – top	0
72	5	0	0	4 – bottom 1.5 – top	0
96	5	0	0	5	0

There was little difference between the SOICs and the QFPs in the unprotected state. Likewise, whether the packing method was tube, tape and reel, or stacked tray, the attenuating effects of the packing were similar.

Micrographs are shown in Figures 4 through 7. The level of corrosion on QFPs not in their shipping trays is quite evident. EDAX analysis of the corrosion deposits confirms that the predominant species are oxides, sulfides, and chlorides of Cu. This is consistent with the nature of the corrosive gases in the Battelle Class 2 environment.

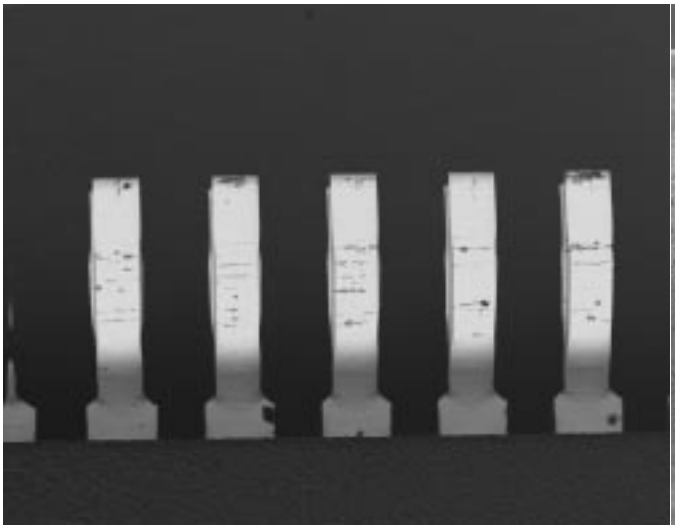

Figure 4. QFP in Tray After 48-Hour Exposure to Class 2 Environment

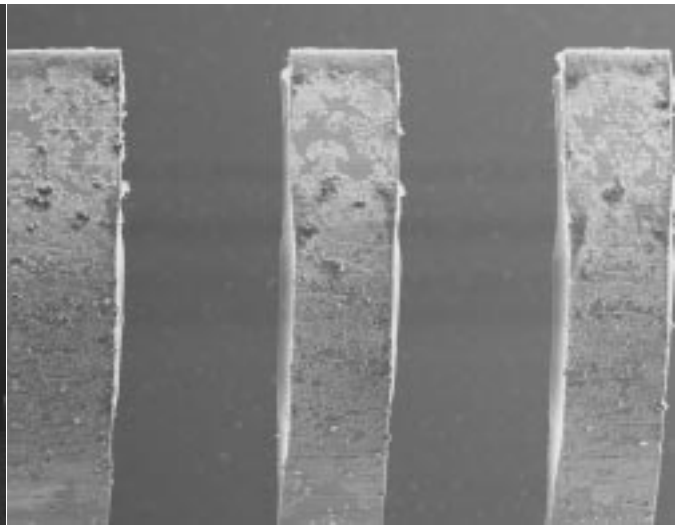

Figure 5. QFP Outside of Tray After 48-Hour Exposure to Class 2 Environment

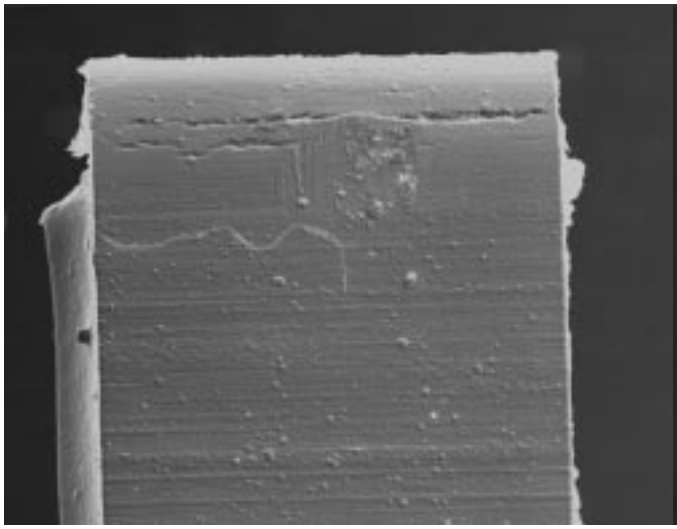

Figure 6. QFP Lead, Stored in Tray After 48-Hour Exposure to Class 2 Environment

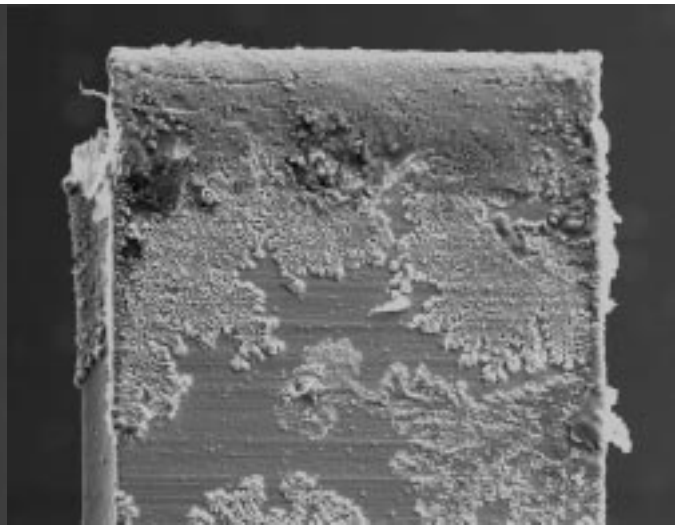

Figure 7. QFP Lead, Stored Outside of Tray After 48-Hour Exposure to Class 2 Environment

The results for the surface-mount solderability test method are shown in Table 3. Results are shown as sample size/number of fails for each group.

Table 3. Solderability Test Results

CLASS 2 EXPOSURE HOURS	GROUP 1 20-PIN SOIC OUTSIDE OF PACKING	GROUP 2 20-PIN SOIC TUBES	GROUP 3 20-PIN SOIC TAPE AND REEL	GROUP 4 80-PIN TQFP OUTSIDE OF PACKING	GROUP 5 80-PIN TQFP TRAY
12	4/0	4/0	4/0	4/0	4/0
24	3/3	4/0	4/0	4/2	4/0
36	4/4	4/0	4/0	4/4	4/0
48	4/4	4/0	4/0	3/3	3/0
72	4/4	4/0	4/0	3/3	4/0
96	5/5	4/0	4/0	4/4	6/0

Confirmation that the test conditions were as expected is shown in Table 4 and Figure 8. Two methods were used to assess test conditions. Simple mass gain measurements were taken and then converted to film thickness, using the area of the coupon and the average density of the film based on previously published experimental observations. The second method was an electrochemical reduction of the corrosion film. This method allows one to distinguish between CuO and Cu_2S, and is the reason for the *Percent Oxide* column in Table 4. The measurements on test coupons show good agreement between the film thickness calculated by mass gain and by electrochemical reduction. Based on field observations for films of these thicknesses, the acceleration factor for this test is roughly 730:1 or 48 hours = 4 years, as expected. At short exposure time, there is a discrepancy between the electrochemical reduction method and the mass gain. This, in part, may be caused by the error in weighing very small masses of material.

Table 4. Corrosion Effects on Copper Control Specimens

SPECIMEN NUMBER	EXPOSURE TIME (HOURS)	MASS GAIN (mg)	FILM THICKNESS BY MASS GAIN (ANGSTROM)	EQUIVALENT YEARS	FILM THICKNESS BY E-CHEM REDUCTION (ANGSTROM)	PERCENT OXIDE	EQUIVALENT YEARS	AVERAGE YEARS
1	24	0.18	730	1.3	1317	19%	2.4	
2	24	0.17	689	1.3	1277	16%	2.3	2.4
3	48	0.56	2269	4.1	2234	22%	4.1	
4	48	0.51	2066	3.8	2162	24%	3.9	4
5	72	0.84	3403	6.2	3624	25%	6.6	
6	72	0.91	3687	6.7	3644	24%	6.6	6.6
7	96	1.12	4538	8.3	4437	29%	8.1	
8	96	1.29	5277	9.5	4880	30%	8.9	
9	96	1.29	5277	9.5	4448	36%	8.1	8.4

Figure 8 graphically shows the data from Table 4. On the left Y-axis of the table, exposure time is expressed in hours. On the right Y-axis, units are the corresponding equivalent shelf times expressed in years (48 hours = 4 years) based on field observations. For each copper control specimen taken from the chamber at the various read points, the exposure time in hours is plotted against the Y-axis on the left side of the table. Equivalent years by mass gain and electrochemical reduction of the corrosion film are plotted against the Y-axis on the right side of the table for each specimen. Figure 8 graphically displays good correlation between measurements on test coupons and between the film thickness calculated by mass gain and by electrochemical reduction.

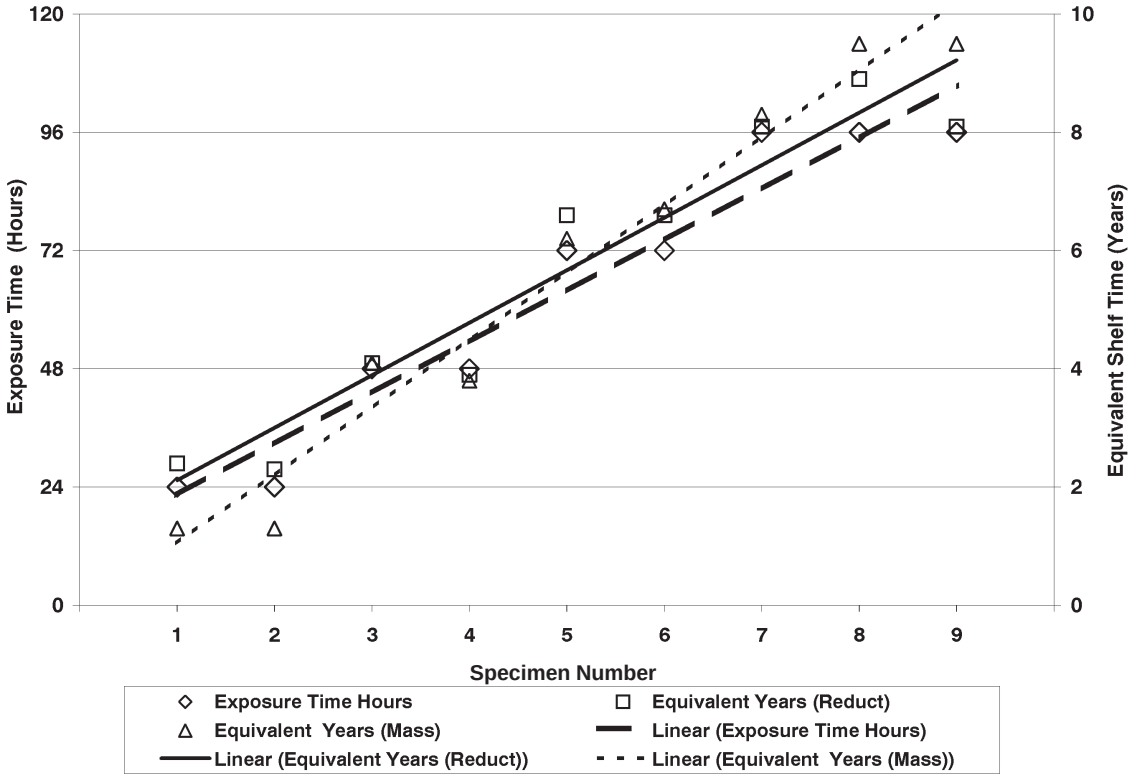

Figure 8. Time Acceleration Data for Battelle Class 2 Mixed Flowing-Gas Test

Conclusion

The results of this study indicate that NiPd-finished components can achieve good solderability after eight years of shelf storage in normal packing materials (tubes, trays, tape and reel). Finished ICs typically are stored in the tubes, trays, or tape-and-reel packing materials until immediately before being soldered by the end user. When storage is completely open to the atmosphere, with no packing materials, the Ni/Pd-finished components achieve good solderability after being stored for over one year.

Acknowledgment

The authors of this application report are Donald C. Abbott, Raymond A. Frechette, Gardner Haynes, and Douglas W. Romm.

References

1. D. Abbott, R. Brook, N. McLellan, and J. Wiley, *Palladium as a Lead Finish for Surface Mount Integrated Circuit Packages*, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 1991.
2. A. Murata and D. Abbott, Semicon Japan Technical Proceedings, 1990.
3. M. Kurihara, M. Mori, T. Uno, T. Tani, and T. Morikawa, SEMI Packaging Seminar Taiwan, 1997.
4. D. Romm, *Palladium Lead Finish User's Manual*, 1994.
5. W. Abbott, *The Development and Performance Characteristics of Mixed Flowing Gas Test Environments*, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 1988.
6. G. Koch, W. Abbott, G. Davis, *Corrosion of Electrical Connectors*, Materials Performance Journal, National Association of Corrosion Engineers, 1988.
7. ASTM B827-92, *Standard Practice for Conducting Mixed Flowing Gas (MFG) Environmental Tests*, 1992.
8. ASTM B825-92, *Standard Test Method for Coulometric Reduction of Surface Films on Metallic Test Samples*, 1992.
9. ASTM B810-91, *Standard Test Method for Calibration of Atmospheric Corrosion Test Chambers by Change in Mass of Copper Coupons*, 1991.
10. G. Haynes and R. Baboian, *Creep in Mixed Gas Tests*, Materials Performance Journal, National Association of Corrosion Engineers, 1990.
11. W. Abbott, *Comparison of Electronic Component Degradation in Field and Laboratory Environments*, Materials Performance Journal, National Association of Corrosion Engineers, 1991.
12. ANSI/EIA-638, *Surface Mount Solderability Test*, 1995.