PowerFLEX™
Surface-Mount Alternative for
Through-Hole Power Packages
IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (“CRITICAL APPLICATIONS”). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER’S RISK.

In order to minimize risks associated with the customer’s applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI’s publication of information regarding any third party’s products or services does not constitute TI’s approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated
Contents

Title Page

Abstract .................................................................................................................. 1
Introduction ........................................................................................................... 1
Background ........................................................................................................... 2
  Maximum Power Dissipation for Voltage-Regulator Packages ....................... 2
  Mounting Effects on Thermal Resistance ......................................................... 3
Thermal Test Procedures and Mounting Techniques ........................................... 4
  Test Setup ........................................................................................................... 4
Thermal-Resistance Measurement Results ......................................................... 5
  Thermal Resistance ........................................................................................... 5
  Effects of Different Land Patterns on Thermal Resistance ............................... 6
Board-Level Assembly Guidelines and Solder-Joint Reliability ......................... 8
  Experimental Results ......................................................................................... 8
Conclusion ............................................................................................................ 9
Acknowledgements .............................................................................................. 9
References .......................................................................................................... A–1
Appendix A .......................................................................................................... A–1
  Recommended Land Patterns, Mechanical Dimensions, and Tape-and-Reel Specifications ......................................................... A–1
Appendix B .......................................................................................................... B–1
Appendix C .......................................................................................................... C–1

List of Illustrations

Figure Title Page
1 PowerFLEX Package Family ........................................................................... 1
2 Maximum Power Dissipation for Voltage-Regulator Packages ....................... 2
3 Maximum Power Dissipation for Regulator Mounted on PCB ......................... 3
4 Multilayer, Two-Signal, Two-Plane Test-Board Dimensions ............................ 4
5 Multilayer PCB Cross Section Showing Cu and Dielectric Thickness ................. 4
6 Still-Air Junction-to-Ambient Thermal Resistance ........................................... 5
7 Junction-to-Ambient Thermal Resistance Under Various Airflow Conditions . 5
8 Land Patterns Used to Model Effects of Footprint Size on Thermal Resistance . 6
9 Comparison of SOT-223 and KTP Land Patterns Required for Equivalent Thermal Performance ......................................................... 7
10 Relationship Between Thermal Performance and Pad Size for KTP Package ................................. 7
11 PCB Land Patterns Used for Board-Level Assembly ........................................ 8
A–1 2KTP PowerFLEX ....................................................................................... A–1
A–2 3KTE/5KTG PowerFLEX ........................................................................... A–2
A–3 KTP PowerFLEX Plastic Flange-Mount Package .......................................... A–3
A–4 KTE PowerFLEX Plastic Flange-Mount Package .......................................... A–4
A–5 KTG PowerFLEX Plastic Flange-Mount Package .......................................... A–5
A–6 Reel Dimensions ......................................................................................... A–6
A–7 Tape Dimensions ......................................................................................... A–7
B–1 IR Reflow Profile Used for PowerFLEX Board-Level Study ......................... B–1
C–1 X-Rays of KTP Packages After Temperature Cycling (–65°C to 150°C) .......... C–1
C–2 SEM Photographs of KTP Packages After 3500 Temperature Cycles (–65°C to 150°C) ......................... C–2
Abstract

The Texas Instruments (TI™) PowerFLEX™ family of voltage regulators offers surface-mount packages with high thermal-dissipation capability that can be mounted using standard techniques and equipment. This application report addresses power dissipation characteristics, footprint sizes, and land patterns; provides mechanical dimensions and tape-and-reel packing information; and illustrates solder-joint reliability of PowerFLEX packages over a wide range of temperature and cycles.

Introduction

The thermally enhanced PowerFLEX family offers a surface-mount alternative to larger through-hole power packages, such as the TO-220, while maintaining high thermal-dissipation capability. PowerFLEX packages are available in a variety of footprints and pin counts and can be mounted using standard printed circuit board (PCB) mounting techniques and equipment. This application report focuses on the 2-pin KTP, 3-pin KTE, and 5-pin KTG members of the PowerFLEX package family used as voltage regulators (see Figure 1).

![Figure 1. PowerFLEX Package Family](image)

The main topics addressed in this application report are:

- Power dissipation characteristics of voltage-regulator packages
- Thermal effects of mounting a package on a PCB
- Test procedures, hardware, and mounting techniques used to determine junction-to-ambient thermal resistance and to obtain optimal thermal performance
- Comparison of the thermal characteristics and footprint sizes of the PowerFLEX family to other popular power packages
- Recommended land patterns, tape-and-reel packing information, and mechanical dimensions
- Board-level assembly guidelines and solder-joint reliability of PowerFLEX packages

PowerFLEX and TI are trademarks of Texas Instruments Incorporated.
Background

Maximum Power Dissipation for Voltage-Regulator Packages

The efficiency of a regulator is defined as \( \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{P_{\text{in}} - P_{\text{Loss}}}{P_{\text{in}}} \). The power losses of the regulator are converted directly to heat and must be dissipated by the package (see Figure 2). The maximum allowable power dissipation of a package radiating in free air can be defined as:

\[
P_{D(\text{max})} = \frac{T_{J(\text{max})} - T_A}{\theta_{JA}}
\]

(1)

Where:

- \( P_{D(\text{max})} \) = maximum allowable power dissipation (W)
- \( T_{J(\text{max})} \) = operating junction temperature (°C)
- \( T_A \) = ambient temperature (°C)
- \( \theta_{JA} \) = junction-to-ambient thermal resistance of the package (°C/W)

![Figure 2. Maximum Power Dissipation for Voltage Regulator Radiating in Free Air](image)

From Equation 1, the maximum allowable power dissipation is inversely proportional to the value of the thermal resistance. If \( \theta_{JA} \) is minimized, \( P_{D(\text{max})} \) can be maximized. In the past, only large form-factor through-hole power packages, such as TO-220, were capable of small values of \( \theta_{JA} \). The advantage of the PowerFLEX family of packages is that \( \theta_{JA} \) is kept low, while offering compact size and surface-mount capability.

An important thing to note about Equation 1 is that the user must select the operating junction temperature \( T_{J(\text{max})} \). Most data sheets specify an absolute maximum junction temperature of 150°C. However, operating at this temperature can severely impact reliability; TI recommends a maximum operating junction temperature of 125°C for its regulators.
Mounting Effects on Thermal Resistance

When a package is mounted on the surface of a PCB (see Figure 3), $\theta_{JA}$ can be described as the sum of several different elements of thermal resistance:

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

(2)

Where:

- $\theta_{JA}$ = junction-to-ambient thermal resistance ($^\circ\text{C/W}$)
- $\theta_{JC}$ = junction-to-case thermal resistance ($^\circ\text{C/W}$)
- $\theta_{CH}$ = case-to-heat-sink thermal resistance ($^\circ\text{C/W}$)
- $\theta_{HA}$ = heat-sink-to-ambient thermal resistance ($^\circ\text{C/W}$)

$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}

\begin{align*}
\theta_{JA} & = \theta_{JC} + \theta_{CH} + \theta_{HA} = 30^\circ\text{C/W} \\
P_{D(\text{max})} & = \frac{125^\circ\text{C} - 25^\circ\text{C}}{30^\circ\text{C/W}} = 3.33 \text{ W}
\end{align*}

**Figure 3. Maximum Power Dissipation for Regulator Mounted on PCB**

Most of the regulators available in PowerFLEX packaging have the die pad (metal tab) in electrical contact with ground. This presents an advantage to the designer by allowing thermal vias to be placed on the surface of the PCB that are connected electrically to an embedded ground plane. Direct electrical connection lowers the thermal resistance between the case and the heat-spreading copper (Cu) layer of the ground plane, $\theta_{CH}$. This results in a lower $\theta_{JA}$, and improves overall power-dissipation capability. For other fixed and adjustable regulators where the bias current flows through the output, the die pad must be isolated electrically from the ground plane. The high thermal resistance of the PCB reduces the amount of heat transfer between the case and the Cu plane. For devices of this type, thermal vias cannot be used, and the benefits of direct electrical connection are not available.
Thermal Test Procedures and Mounting Techniques

Test Setup

The thermal resistance of the PowerFLEX packages and the other packages discussed in this application report were measured and/or modeled according to JEDEC standards (JESD 51, JESD 51-1, JESD 651-2, and JESD 51-6). For measured data, the packages were soldered directly to the PCB. The test board used for the measured data meets the JEDEC standards for multilayer, direct-thermal-attachment test boards (JESD 5-7, JESD 5-5) and has the following characteristics:

- FR-4 PCB material (see Figure 3 for dimensions)
- Two embedded 1-oz Cu planes and one floating lower Cu plane (see Figure 5)
- Supplier-recommended land patterns on the top surface of the board (2-oz Cu)
- Thermal vias connecting the upper Cu plane to the package thermal pad where applicable

![Thermal Test Board Dimensions](image)

**Figure 4. Multilayer, Two-Signal, Two-Plane Test-Board Dimensions**

![Multilayer PCB Cross Section](image)

**Figure 5. Multilayer PCB Cross Section Showing Cu and Dielectric Thickness**

Still-air $\theta_{JA}$ measurements were performed with the test board in a 1-ft$^3$ box. Forced-airflow measurements were made in a calibrated wind tunnel. All measurements were performed at ambient temperature. Conditions used for the measured data also were used for the modeled data. The PowerFLEX data shown in this application report consists of both measured and modeled values; other package data was only modeled. All modeled data was gathered using Thermcal™, a proprietary program used internally by TI. The modeled PowerFLEX data is accurate to within 5% of the measured values.

Thermcal is a trademark of Texas Instruments Incorporated.
To maintain consistency between the thermal models, an array of 0.33-mm (0.013”) diameter vias on a 1.27-mm (0.050”) pitch grid was used. The vias extend from the top surface of the PCB to the first of two 1-oz buried Cu planes. These via grids are arranged within the recommended footprint for each package (see Appendix A). Vias were not placed outside of the recommended footprint when a larger Cu land pattern was used on the top surface of the PCB for enhanced thermal performance.

Thermal-Resistance Measurement Results

Thermal Resistance

Still-air $\theta_{JA}$ values are shown in Figure 6 for the KTP, DPAK (TO-252), SOT-223, and KTE packages. The KTP and DPAK thermal resistances are virtually the same, and their $\theta_{JA}$ values are 30% lower than for the SOT-223.

Because of the reduction in $\theta_{JA}$, the KTP package has better power-dissipation capability than the SOT-223. The KTP package has the same $\theta_{JA}$ as the DPAK, but has slightly smaller dimensions and a thinner profile.

![Figure 6. Still-Air Junction-to-Ambient Thermal Resistance](image)

In addition to still-air measurements, the value of $\theta_{JA}$ was modeled for forced airflow conditions. Figure 7 shows the results for the KTP, DPAK, SOT-223, and KTE packages.

![Figure 7. Junction-to-Ambient Thermal Resistance Under Various Airflow Conditions](image)

The SOT-223 package has much higher values of $\theta_{JA}$ than the KTP and DPAK packages. The KTE package has a lower $\theta_{JA}$ than SOT-223, KTP, and DPAK packages because of its larger form factor. Thus, the PowerFLEX devices have improved power-dissipation capability compared to the SOT-223 and DPAK packages.
Effects of Different Land Patterns on Thermal Resistance

Still-air $\theta_{JA}$ values were modeled for the KTP package using four different PCB land patterns (see Figure 8). The four land patterns selected represent approximate Cu footprint sizes for KTP, DPAK, KTE, and TO-220 packages. A thermal-test chip with dimensions of 3 mm (0.12") square was assembled in the test packages.

The measured thermal resistance values for the land patterns shown in Figure 8 are:

<table>
<thead>
<tr>
<th>Pattern</th>
<th>$\theta_{JA}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>30.5</td>
</tr>
<tr>
<td>2</td>
<td>29.4</td>
</tr>
<tr>
<td>3</td>
<td>27.2</td>
</tr>
<tr>
<td>4</td>
<td>25.8</td>
</tr>
</tbody>
</table>

See Appendix A for Recommended PowerFLEX Land Patterns

Figure 8. Land Patterns Used to Model Effects of Footprint Size on Thermal Resistance
Although power dissipation can be improved by increasing the size of the Cu land pattern on the top side of the PCB, the size of the land pattern may become impractical for smaller form-factor packages. For example, to obtain the same thermal performance of the KTP, the SOT-223 must use a Cu pattern that is at least four times the standard KTP land pattern (see Figure 9). With this enlarged pattern, $\theta_{JA}$ for the SOT-223 is lowered to 32–33 °C/W, but is still slightly higher than the 30 °C/W of KTP using the standard recommended pattern.

![Figure 9. Comparison of SOT-223 and KTP Land Patterns Required for Equivalent Thermal Performance](image)

Figure 10 shows the estimated land pattern required for various values of $\theta_{JA}$ using the KTP package. As the area of the pattern is increased, the value of $\theta_{JA}$ decreases; therefore, the maximum allowable power dissipation increases.

![Figure 10. Relationship Between Thermal Performance and Pad Size for KTP Package](image)
Board-Level Assembly Guidelines and Solder-Joint Reliability

The Morgan Newton Co., Garland, Texas, provided TI with their recommendations for stencil design, solder-paste type, and infrared (IR) profile. A board-level evaluation of the KTP package was performed using these recommendations. The objectives of the evaluation were:

- Show that the KTP package can be mounted onto the standard DPAK land pattern with no board-level reliability issues.
- Show that a solder mask applied over an enlarged Cu land pattern can provide improved thermal performance with no board-level reliability issues.

The stencil parameters, materials, etc., used for this experiment include:

- Solder paste type: No clean
- Alloy type: Sn62/Pb36/Ag2
- Solder past particle size: 325 to 500
- Stencil type: 301 stainless steel, laser cut
- Stencil thickness: 8 mil
- Squeegee type: Metal
- IR reflow profile: See Appendix B

Three different land patterns were used for board-level assembly of the KTP package: the KTP pattern, the standard DPAK pattern, and a modified KTP pattern with a larger area and solder mask over the Cu for improved thermal performance (see Figure 11).

See Appendix A for Recommended PowerFLEX Land Patterns

Figure 11. PCB Land Patterns Used for Board-Level Assembly
Experimental Results
Solder-joint inspections and electrical tests were made on all three copper patterns every 500 temperature cycles up to 3500 cycles. No solder-joint anomalies or opens were found.

X-rays of the solder joints at various stages of the temperature-cycle tests and scanning electron microscope (SEM) photos of cross-sectioned KTP packages (3500 temperature cycles) are shown in Appendix C.

Conclusion
The PowerFLEX voltage-regulator packages offer excellent thermal performance for medium- to high-power applications. The packages maintain low junction-to-ambient thermal resistance, while providing the added benefit of surface-mount capability. The KTP package has equivalent thermal performance to the DPAK (TO-252) package and improved thermal performance over the SOT-223 package. In addition, the PowerFLEX packages can be mounted using standard PCB mounting techniques and equipment. The KTP package can easily be soldered onto the standard DPAK footprint. Package land patterns with solder mask over an enlarged copper area offer improved thermal performance with no decrease in board-level reliability.

Acknowledgements
The authors of this application report are Patrick Griffith and Craig St. Martin. Terrill Sallee provided assistance for board-level assembly and reliability testing of PowerFLEX products; Doug Romm for thermal-impedance model generation of all packages discussed in this report; and Paul Hundt for thermal-impedance measurement of two PowerFLEX units on various land patterns.

References
EIA/JESD 51, Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).
EIA/JESD 51-5, Extension of Thermal Board Standards for Packages With Direct Thermal Attachment Mechanisms.
EIA/JESD 51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.
Texas Instruments, Thin Very Small-Outline (TVSOP) Application Report, literature number SCBA009.
Texas Instruments, PowerFLEX™ Surface-Mount Power Packaging Application Report, literature number SLIT115.
Appendix A

Recommended Land Patterns, Mechanical Dimensions, and Tape-and-Reel Specifications

NOTES:
A. All dimensions are in millimeters (mm).
B. Publication IPC-SM-782 is recommended for alternative designs.
C. Solder mask placed over Cu can be used for improved thermal performance.

Figure A–1. 2KTP PowerFLEX
Solder Mask Over Cu (optional)

<table>
<thead>
<tr>
<th>PINS</th>
<th>PACKAGE CODE</th>
<th>L</th>
<th>N</th>
<th>P</th>
<th>W</th>
<th>X1</th>
<th>X2</th>
<th>X3</th>
<th>X4</th>
<th>Y1</th>
<th>Y2</th>
<th>Y3</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>KTE</td>
<td>1.37</td>
<td>2</td>
<td>2.54</td>
<td>0.96</td>
<td>6.4</td>
<td>0.76</td>
<td>0.79</td>
<td>9.5</td>
<td>5.56</td>
<td>1.3</td>
<td>1.56</td>
<td>11.4</td>
</tr>
<tr>
<td>5</td>
<td>KTG</td>
<td>1.37</td>
<td>4</td>
<td>1.72</td>
<td>0.96</td>
<td>6.4</td>
<td>0.76</td>
<td>0.79</td>
<td>9.5</td>
<td>5.56</td>
<td>1.3</td>
<td>1.56</td>
<td>11.4</td>
</tr>
</tbody>
</table>

†N = number of leads

NOTES:
A. All dimensions are in millimeters (mm).
B. Publication IPC-SM-782 is recommended for alternative designs.
C. 3-pin PowerFLEX shown.
D. Solder mask placed over Cu can be used for improved thermal performance.

Figure A–2. 3KTE/5KTG PowerFLEX
NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

Figure A–3. KTP PowerFLEX Plastic Flange-Mount Package

PowerFLEX is a trademark of Texas Instruments Incorporated.
NOTES:  
A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. The center lead is in electrical contact with the thermal tab.  
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0.15).

Figure A–4. KTE PowerFLEX Plastic Flange-Mount Package
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).

Figure A–5. KTG PowerFLEX Plastic Flange-Mount Package

PowerFLEX is a trademark of Texas Instruments Incorporated.
NOTE A: Dimensions are in millimeters (mm).

### Figure A–6. Reel Dimensions

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>PINS</th>
<th>TAPE WIDTH (G) (mm)</th>
<th>REEL THICKNESS (T) (mm)</th>
<th>PARTS PER REEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>KTP</td>
<td>2</td>
<td>16</td>
<td>20</td>
<td>2500</td>
</tr>
<tr>
<td>KTE</td>
<td>3</td>
<td>24</td>
<td>28</td>
<td>1000</td>
</tr>
<tr>
<td>KTG</td>
<td>5</td>
<td>24</td>
<td>28</td>
<td>1000</td>
</tr>
</tbody>
</table>
NOTE A: Dimensions are in millimeters (mm).

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>PINS</th>
<th>WIDTH (W)</th>
<th>POCKET PITCH (P)</th>
<th>POCKET WIDTH (A₀)</th>
<th>POCKET LENGTH (B₀)</th>
<th>POCKET DEPTH (K₀)</th>
<th>TAPE DEPTH (K)</th>
<th>DIMENSION (F)</th>
</tr>
</thead>
<tbody>
<tr>
<td>KTP</td>
<td>2</td>
<td>16</td>
<td>12</td>
<td>6.50</td>
<td>10.0</td>
<td>2.20</td>
<td>2.60</td>
<td>7.50</td>
</tr>
<tr>
<td>KTE/KTG</td>
<td>3/5</td>
<td>24</td>
<td>16</td>
<td>9.80</td>
<td>11.0</td>
<td>2.20</td>
<td>2.60</td>
<td>11.50</td>
</tr>
</tbody>
</table>

Figure A–7. Tape Dimensions
Appendix B

Company: Morgan Newton Co.
Process: CONC
Printed: 06/25/1998
Site: Cambridge
Product: PR2001-E
Line Speed: 25 in/min

![Graph showing temperature profile with annotations for different zones and times above specific temperatures.]

<table>
<thead>
<tr>
<th>ZONE</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Upper</td>
<td>140</td>
<td>190</td>
<td>210</td>
<td>180</td>
<td>190</td>
<td>255</td>
<td>220</td>
</tr>
<tr>
<td>Lower</td>
<td>140</td>
<td>190</td>
<td>210</td>
<td>180</td>
<td>190</td>
<td>255</td>
<td>220</td>
</tr>
</tbody>
</table>

Figure B–1. IR Reflow Profile Used for PowerFLEX Board-Level Study
Figure C–1. X-Rays of KTP Packages After Temperature Cycling (–65°C to 150°C)
Figure C–2. SEM Photographs of KTP Packages After 3500 Temperature Cycles
(–65°C to 150°C)