

# 66AK2L06 DSP+ARM<sup>®</sup> Processor JESD204B Attach to ADC12J4000/DAC38J84 Design Getting Started Guide

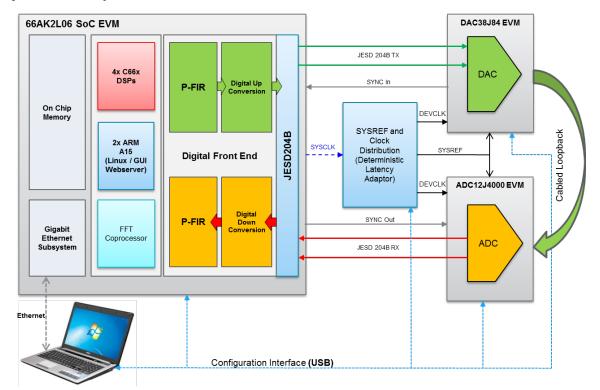
#### Nitin Sakhuja

#### 1 Overview

The TI 66AK2L06 system-on-chip (SoC) is the industry's first JESD204B-compliant multicore DSP+ARM<sup>®</sup> SoC that can interface with high-performance JESD204B data converters. The device also includes a digital front end (DFE) that can process TX and RX signals, forming a system-optimized alternative to FPGAs.

This demonstration focuses on the JESD attach and DFE signal-processing capabilities of the SoC interfaced with TI's high-performance ADC12J4000 and DAC38J84 wideband-data converters. The demonstration consists of transmitting a sample file from the SoC through the DAC38J84 and looping it through the ADC into the SoC. The sample data files include dual-tone and multi-tone test patterns.

#### 1.1 System Description





ARM is a registered trademark of Texas Instruments. Linux is a registered trademark of Linus Torvaldis. Windows is a registered trademark of Microsoft Inc. Silicon Labs is a trademark of Silicon Laboratories.

1



#### Getting Started

www.ti.com

The DSP provides baseband data for two 75-MHz antenna carriers (FS = 92.16 Msps/carrier) to the DFE of the 66AK2L06 SoC. In the downlink path, one carrier is up-shifted by 43.5 MHz and the other is down-shifted by 43.5 MHz, giving a total bandwidth of 162 MHz. Carrier data is up-sampled from 92.16 Msps at baseband to provide 368.64 Msps at the JESD interface. The two carriers are combined onto one antenna and packed in parallel IQ format at the JESD204B SerDes. Although there are 4 JESD lanes on the 66AK2L06 SoC, only two are used (one lane for I and one lane for Q. The JESD204B SerDes link rate is 7.3728 Gbps).

DAC38J84 gets its input over JESD as parallel IQ data with a byte clock of 368.64 MHz. The DAC output rate is 737.28 Msps with an interpolation ratio of 2. The output of the DAC38J84 is centered at 184.32 MHz.

TI recommends using a spectrum analyzer to check the DAC output before running the loopback test. In the loopback case, the DAC output signal of the device is sent through a low-pass filter to the ADC12J4000. The DEVCLK of the ADC12J4000 is 2949.12 MHz. The ADC12J4000 is configured in Decimate-by-8 DDR P54 mode. It sends IQ data to the DFE over JESD in parallel IQ format with a byte clock of 368.64 MHz.

In RX side, the DFE inside 66AK2L06 SoC down-samples the data steam and shifts the two carriers back to a center frequency of zero.

#### 2 Getting Started

#### 2.1 Required Hardware and Software Components

#### **Hardware Components**

- The 66AK2L06 EVM, rev. 3.0, with the following accessories:
  - A 12-V power supply
  - A mini-USB cable for a UART connection
  - An Ethernet cable
- The K2L-HSP FMC Adapter Rev.A with the following accesories:
  - A mini-USB cable to connect with a PC
- The DAC38J84, rev. D, with the following accessories:
  - A 5-V DC power supply
  - A mini-USB cable for connection with a PC
- The ADC12J4000 EVM with the following accessories:
  - A 5-V DC power supply
  - A mini-USB cable for GUI SPI program
  - An ADC-WB-BB EVM with short marching-length SMA (male) cables
- DC-264 MHz low-pass filter
- 4 SMA cables

2

#### Software Components (with links to downloadable GUI installers)

The demonstration package is a Windows<sup>®</sup> installer executable. Running this installer on the Windows host extracts the software components per the following directory structure:

- RFSDK2 <latest\_version> Top level directory includes:
  - RFSDK2 <latest\_version>-full-bin.tar.gz: Demo package to be installed on top of MCSDK 3.1.4.7 on 66AK2L06 EVM
  - RFSDK2 <latest\_version>-66AK2Lx-Design-Demo-Win-GUI-Configs.zip: Board initialization and configurations files for ADC12J4000 and DAC38J84 EVM GUIs
  - mcsdk314\_rfsdk.tar.gz: MCSDK patches for the demo
  - RFSDK2 <latest\_version>-doc.tar.gz: Documentation and Release notes
- Configuration GUIs for data converter EVMs (Windows-based)
  - ADC12J4000 EVM GUI

#### - DAC38J84 EVM GUI

#### 2.2 Hardware Setup

- 1. To connect the 66AK2L06, DAC38J84, and ADC12J4000 EVMs, do the following:
  - (a) Plug the FMC male connector of the ADC12J4000 into J11 (FMC female) of the DLC.
  - (b) Plug the FMC male connector of the DAC38J84 into J10 (FMC female) of the DLC.
  - (c) Plug the J4 FMC male connector of the DLC into CN16 (FMC female) of the 66AK2L06 EVM. For a view of the setup with all the boards connected, see Figure 2.
- 2. To connect the clocks, do the following:
  - (a) Connect an SMA cable from J15 of the DLC to the DEVCLK of the ADC12J4000.
    - **NOTE:** The LMK04828 on the DLC is a dual-PLL clock chip. The clock-in reference for PLL1 comes from the 66AK2L06 EVM (122.88 MHz). The onboard VCXO of 122.88 MHz on the deterministic latency adapter (DLA) is a reference for PLL2. The output of LMK04828 provides device clocks to both DAC38J84 and ADC12J4000.
- 3. To connect the DAC38J84 output to ADC12J4000 input (the loopback configuration), do the following:
  - (a) Use length-matching SMA cables to connect J2 (VOUT+) and J3 (VOUT-) of the ADC-WB-BB EVM to VIN+ and VIN- of the ADC12J4000.
  - (b) Connect DAC38J84 output at J2 (IOUTAP) to the DC-264 MHz low-pass filter.
  - (c) Connect the other end of the DC-264 MHz low-pass filter to the input of ADC-WB-BB EVM J1 to complete the loop back.

For a view of the setup with all the clock and loopback connections, see Figure 3.

- 4. To connect USB and Ethernet cables, do the following:
  - (a) Using a mini-USB cable to connect the mini-USB port J6 on the 66AK2L06 EVM to the PC. (The J6 provides the board-management controller [BMC] and Linux<sup>®</sup> serial-terminal interfaces multiplexed onto the same port.)
  - (b) Use mini-USB cables to connect the ADC12J4000, DAC38J84, and DLC to the Windows host.
  - (c) Connect the 66AK2L06 EVM ETH-0 (lower port) to the same network as the Windows host over a 1-Gbps connection (either directly or through a gigabit switch).
  - **NOTE:** Follow the correct power-up sequence for proper initialization of the setup. The K2L EVM is powered up first, followed by the DAC and ADC EVMs. Finally, the K2L-HSP FMC Adapter is powered up.
- 5. For power considerations, do the following:
  - (a) Using the 5-V DC power supplies to provide 5 V to both the ADC12J4000 and the DAC38J84.
  - (b) Use the 12-V DC power supply to provide 12 V to the 66AK2L06 EVM.
- 6. For other considerations, do the following:
  - (a) For initial test and debug purposes, check the output of the DAC38J84 on a spectrum analyzer before trying to loop back. Connect the DAC38J84 J2 (IOUTAP) to the spectrum analyzer input.
  - (b) When the DAC38J84 J2 output is working, configure and connect the DAC38J84 and the ADC12J4000 to loop back.

3



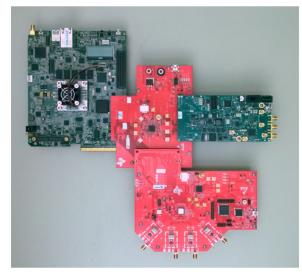


Figure 2. Boards Connected Together

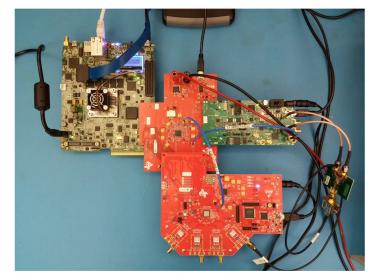


Figure 3. Complete Setup With Cables and Power Supplies Connected



#### 2.3 Setup Software

#### 2.3.1 Preparing the 66AK2L06 EVM for the Demonstration

To prepare the 66AK2L06 EVM for the demo, connect a terminal program (for example, Tera Term) to the 66AK2L06 EVM Linux COM port.

Use the following serial-port settings in the terminal program:

- Baud Rate: 115,200
- **Data**: 8 bit
- Parity: None
- **Stop**: 1 bit
- Flow Control: None

NOTE: The Silicon Labs<sup>™</sup> CP210x VCP driver must be installed to enumerate the 66AK2L06 EVM virtual COM ports in Windows device manager.

🖃 🖤 Ports (COM & LPT)	
ECP Printer Port (LPT1)	
	4 Port (COM10)
Silicon Labs Dual CP210x USB to UART Bridge: Standard COM	I Port (COM9)

Figure 4. 66AK2L06 EVM Virtual COM Ports

Though port numbers on your system may vary, the higher-numbered COM port (COM10) is for Linux.

To prepare the 66AK2L06 EVM for the demonstration, do the following:

#### 1. Update the UBIFS image on the 66AK2L06 EVM.

- (a) Update the factory-installed MCSDK image on the 66AK2L06 to the image provided with MCSDK 3.01.04.07.
- (b) To update the UBIFS image on the 66AK2L06 EVM, tftp server is needed. Download the appropriate MCSDK installer (mcsdk\_3\_01\_04\_07\_setupwin32.exe for Windows or mcsdk\_3\_01\_04\_07\_setuplinux.bin for Linux) for your tftp host.
- (c) Run the installer and follow the prompts to install the new MCSDK on your tftp host machine.
- (d) When installed, the UBIFS image for the 66AK2L EVM is available in the images subdirectory under the MCSDK install directory. The image is named *k2I-evm-ubifs.ubi*.
- (e) Follow the instructions given in Using UBIFS File System to update the existing image on the EVM with the UBIFS image.
  - The image and directory names in this section may not match *k2l-evm-ubifs.ubi* but the procedure is the same. Use the appropriate *tftp\_root* directory path, image name, and *serverip* according to your setup.
  - TI recommends using automated u-boot scripts *get\_ubi\_net* and *burn\_ubi* to download and flash the UBIFS image, respectively.

#### 2. Install the device tree binary (dtb) patch.

- (a) When the UBIFS image on the 66AK2L06 EVM is updated, update the dtb file on the EVM with the file in *mcsdk314\_rfsdk.tar.gz* in the demonstration package.
- (b) Extract the dtb binary file from *mcsdk314\_rfsdk.tar.gz* and follow the instructions in Updating Boot Volume Images From a Linux Kernel in the *Keystone-II MCSDK User Guide*.
  - The name of the patched dtb in the demo package may vary from the working dtb filename in the boot volume on the EVM. Ensure you copy the new dtb file to the boot volume with the original dtb filename. Failing to do this will cause the Linux boot to fail when restarting the board.

5



Running the Demo

- 3. Install the demonstration package (user entries are *italicized*).
  - (a) The Demo software is provided as a compressed archive named RFSDK2\_<latest\_version.tar.gz> in the Demo package. Copy this file to the tftp root directory of your tftp server.
  - (b) With Linux booted, copy the above file to /home/root on the EVM (using tftp or scp). root@k2l-evm:~# pwd /home/root root@k2l-evm:~# tftp -g -r RFSDK2\_<latest\_version.tar.gz> <tftp\_server\_ip\_addr>
  - (c) Extract RFSDK2\_<latest\_version>-full-bin.tar.gz in the root directory root@k2l-evm:~# cd / root@k2l-evm:/# tar xvf /home/root/ RFSDK2\_<latest\_version>-full-bin.tar.gz
  - (d) Create a soft link to the default board configuration to finalize the installation root@k2l-evm:/# cd /etc/radio/board root@k2l-evm:/etc/radio/board# In -s lamarr-evm-demo1-mcsdk3147 default root@k2l-evm:/etc/radio/board# Is -I default lrwxrwxrwx 1 root 42005 18 Dec 12 21:30 default → lamarr-evm-demo1-mcsdk3147
  - (e) Reboot Linux on the EVM.

#### 2.3.2 Installing PC-Side Software

Download GUI installers for the DAC38J84 and ADC12J4000 EVMs from the links in Section 2, Getting Started, and perform the following steps to install the corresponding GUIs:

- 1. Install the ADC12J4000 GUI.
  - (a) After ADC12J4000 GUI is installed, go to the configuration files directory. Find this directory at C:\Program Files (x86)\Texas Instruments\ADC12J4000EVM GUIv<version\_no>\Configuration Files.
  - (b) Replace ADC12J4000\_DB8\_DDR.cfg with the corresponding file provided under RFSDK2\_<latest\_version>.66AK2Lx-Design-Demo-Win-GUI-Configs in the demo package.
- 2. Install the DAC34J84 GUI.

#### 3 Running the Demo

#### 3.1 Setting Up the DAC38J84 and ADC12J4000 EVMs

#### 3.1.1 Power Up the Boards in the Following Sequence

- 1. 66AK2L06 EVM
- 2. ADC12J4000 EVM
- 3. DAC38J84 EVM



7

#### 3.1.2 K2L-HSP FMC Adapter

1. Start the K2L-HSP FMC Adapter GUI. Ensure the USB Status indicator is green.

Det Latency Adapter						- • •
File Debug Settings Help						
	Det L	atency A	dapter			
LMK04828 🔝 Low Level View						USB Status 🔵 Reconnect FTDI ?
Register Map           Block / Register Name           □         LM049428           >000         >003           >005         >006           >006         >006           >006         >006           >006         >006           >006         >006           >006         >006           >006         >006           >006         >006           >001         >001           >001         >001           >000         >001           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >000           >000         >0	Address         Default           0x00         0x00           0x12         0x00           0x12         0x00           0x12         0x00           0x12         0x00           0x01         0x01           0x02         0x00           0x04         0x00           0x05         0x00           0x100         0x02           0x101         0x55           0x103         0x00           0x104         0x00           0x105         0x00           0x107         0x00           0x100         0x04           0x100         0x04	Mode         Size           R/W         8           R/W         8           R         8           R         8           R         8           R/W         8	Value         •           0x000         •	Write Data d 0 Write All Read Data x 0 Read All Current Address x 0 Note: Load Config will Overwrite all Registers. Load Config Save Config Block CONNECTED	Register Data RW Address x 0	Write Data       Read Data_Generic         Write Register       Read Register

Figure 5. K2L-HSP FMC Adapter GUI

 Click Load Config and select 66AK2L06\_dac737p28.cfg under RFSDK\_<latest\_version>.66AK2Lx-Design-Demo-Win-GUI-Configs in the demo package. (This programs the required registers of the LMK04828.)

💀 Det Latency Adapter						
File Debug Settings Help						
	Det La	tency Ad	apter			
LMK04828 🗄 Low Level View				U	SB Status 🧿 Reconnec	t FTDI ?
	🔹 Choose or Ent					r Read to Write
Register Map	4	🔒 DLC	•	G 🤌 📂 🛄 -		nead to write
Block / Register Name / A □ LMK0428 002 002 003 004 005 006 006 006 006 006 006 006	Recent Places Desktop Libraries Computer Network	Name 66AK2L06_ File name: Save as type:	م dac137p28.cfg 666AK2L06_dac737p28.cfg Custom Pattern [`cfg]	Date modified 7/29/2015 2:33 PM	Type CFG File V OK Cancel	
Register Description						
			Block	Address x 0	x 0 x	0 ad Register
Operation Successful. 6/2	2016 2:34:48 PM	Build	CONNECTED		🗾 🦊 Texas	INSTRUMENTS

Figure 6. GUI-Load CFG



Running the Demo

8

www.ti.com

3. For the LMK04828 clock output settings, see Figure 7.

Level View	1						
ELOW Level View USB Status Reconnect FTD1?							
uration	PLL2 Configura	ation SYSREF ar	nd SYNC Clock	Outputs			
CLK	out 2 and 3	CLKout 4 and 5 Nat Used	CLKout 6 and 7 SMP Clock Outputs	CLKout 8 and 9 Extra FMC Clocks	CLKout 10 and 11 Not Used	CLKout 12 and 13 Extra FMC Clocks	
evel 📃 🔇		Group Powerdown V Output Drive Level	Group Powerdown	Group Powerdown	Group Powerdown	Group Powerdown Output Drive Level Input Drive Level	
DO	LK Divider	DCLK Divider	DCLK Divider	DCLK Divider	DCLK Divider	DCLK Divider	
. 8		20	1 💌	16 💌	20	4	
DC	LK Source	DCLK Source	DCLK Source	DCLK Source	DCLK Source	DCLK Source	
▼ Div	rider 💌	Divider 💌	Divider + DCC + HS 💌	Divider 💌	Divider 💌	Divider -	
nvert 🔲 DO	LK Type Invert	DCLK Type Invert	DCLK Type Invert	DCLK Type Invert	DCLK Type Invert	DCLK Type Invert	
NV V Po	werdown	Powerdown 💌	LVPECL 2000 mV	Powerdown 💌	LVDS 💌	LVPECL 2000 mV	
50	CLK Source	SDCLK Source	SDCI K Source	SDCLK Source	SDCLK Source	SDCLK Source	
- S1	(SREF	Device Clock	Device Clock	SYSREF .	SYSREF	SYSREF	
						SDCLK Type Invert	
		Powerdown 💌	Powerdown 💌	LYDS .	Powerdown 💌	LVPECL 2000 mV	
tate SD	CLK ENDIS State	SDCLK ENDIS State	SDCLK ENIDIS State	SDCLK ENIDIS State	SDCLK ENDIS State	SDCLK EN/DIS State	
		Active/Active	Active/Active	Active/Active	Active/Active	Active/Active	
						SDCLKout PD	
	- Sind					DCLKout_DDLY_PD	
						DCLKout_HSg_PD	
	LKout ADLYg PD	DCLKout ADLYg PD	DCLKout_ADLYg_PD		DCLKout ADLYg PD	DCLKout ADLYg PD	
			DCLKout_ADLY_PD		DCLKout_ADLY_PD	DCLKout ADLY PD	
	SSREF CLKKS SSREF FPG PG0 Covered Cove	CLKout 2 and 3     SREF     FPGA Clock & SYSREF     FOOM     Group Powerdown //     cdpA Drive Level     CdpA Drive Level     CdpA Drive Level     CdcK Type Invert     DCLK Source     Drivder     SOLCK Type Invert     SOLCK Spurce     SYSREF     wrvet     SOLCK Type Invert     SOLCK Spurce     SOLCK Spurce     SOLCK Spurce     SOLCK Spurce     SOLCK ENDIS State     Active(Active u      d_FO     SOLCK OA_FO     DCLKoa_DCL/p0     DCLKoa_DCL/pC, Type	CLKouf 2 and 3 SREF FPGG Clock 8 SVSREF PGG Clock 8 SVSREF Coup Powerdown V Coup Powerdown V Coup Powerdown V Coup Powerdown V Coup Powerdown V Doub Cleve hpu Drive Level Dpu Drive Level Dpu Drive Level DCLK Source DCLK Source DCLK Source DCLK Source SVSREF SOCLK Source SVSREF SOCLK Source SOCLK Source	CLKout 2 and 3 SREF         CLKout 4 and 5 Net Used         CLKout 6 and 7 SMP Clock Outputs           Oroup Powerdown [V evel]         Oroup Powerdown [V Output Drive Level]         Oroup Powerdown Poult Source         DCLK Divider         DCLK Divider         DCLK Divider           DCLK Source         DVider         DCLK Source         DVider         DCLK Type Inverti Powerdown [V         DCLK Source         DVider         DCLK Type Inverti DVIK Source         DVIK Source	CLKout 2 and 3 SREF         CLKout 4 and 5 Net Used         CLKout 6 and 7 SMP Clock 0 Dubust         CLKout 8 and 9 Edtar FMC Clocks           Oroup Powerdown // Oroup Powerdown // Oroup Doverdown // DCLK Divider         CLKout 8 and 9 Drough Doverdown // DCLK Divider         CLKout 8 Oroup Doverdown // DCLK Divider         CLKout 8 Oroup Doverdown // DCLK Divider         CLKout 8 Droup Doverdown // DCLK Divider         CLKout 8 Droup Doverdown // DCLK Divider         CLKOU DCLK Divider         DCLK Source         DCLK Source         DCLK Type Invert         DCLK Type Invert         DV/ Powerdown // Powerdown //         SOCLK Source         SDCLK Type Invert         SDCLK Source         SDCLK PLOTE State         SDCLK ENDIS State         SDCLK ENDIS State         SDCLK ENDIS State         SDCLK Mode State         SDCLK Mode State         SDCLK Mode State         Active/Active // Active/Active <td>CLKout 2 and 3 SREF         CLKout 4 and 5 Add Used         CLKout 6 and 7 SMP Clock 0 uputs         CLKout 8 and 3 Edta FMC Clock 8 SMP Clock 0 uputs         CLKout 18 and 1 Add Used         CLKout 10 and 11 Add Used           Oroup Powerdown [////////////////////////////////////</td>	CLKout 2 and 3 SREF         CLKout 4 and 5 Add Used         CLKout 6 and 7 SMP Clock 0 uputs         CLKout 8 and 3 Edta FMC Clock 8 SMP Clock 0 uputs         CLKout 18 and 1 Add Used         CLKout 10 and 11 Add Used           Oroup Powerdown [////////////////////////////////////	

Figure 7. GUI Clock Outputs

The details of the clock configuration are the following:

- CLKOUT 6: ADC12J4000 device CLK is GTX CLKP (J15), div 1 for 2949.12 MHz, LVPECL. ADC12J4000 SysRef is unused.
- CLKOUT 12: DAC38J84 device CLK, div 4 for 737.28 MHz, LVPECL. DAC38J8x SysRef CLK is SDCLKOUT 13, LVPECL.
- When configured, the LMK PLL LOCK and VCXO LOCK LEDs on the DLC should be ON (see Figure 8). Ensure that the LMK LOCK LED is lit. If not, power-cycle the DLC and try to configure again.



Figure 8. LED Status

#### 3.1.3 DAC38J8x EVM GUI

- 1. Start the DAC34J84 GUI (Start → All Programs → Texas Instruments DACs → DAC3xJ8x GUI)
- 2. Ensure that the status of the USB is green.
- 3. Set the EVM Clocking Mode to Onboard.
- 4. Select DAC38J82 as the Device (this demonstration uses 2- of the 4-DAC channels on the DAC38J84).
- 5. Select DAC Data Input Rate to 368.64 Msps.
- 6. Select 2 as the Number of SerDes Lanes and as the Interpolation.
- 7. Click Program LLMK04828 and DAC3XJ8X.

💀 DAC3XJ8X GUI				
File Debug Setting	is Help			
		DAC3XJ8X GUI	v1.1	
Quick Start	DAC3XJ8X Controls LMK048	328 Controls Low Level View	Check ALARMS USB	Status Reconnect USB ?
	EVIM Clocking Mode Onboard  Step 2 - Choose Device DAC38J82 DAC Data Inpu 368.64 Step 4 - Program EVM Programming Order: 1. Program LMK04828, toggle DAC RESETB Pin, program DAC3J8X Core	▼ MSPS 2 ▼	737.28 MSPS 2221	4B Mode (LMFS) Linerate Mbps
	3. Trigger SYSREF	Not in RESET		
	QUICK Start message			
	,			
Updated the Tree w	vith register details	1/12/2011 11:44:30 AM = CONN	IECTED Idle	TEXAS INSTRUMENTS

Figure 9. DAC38J8x GUI Start Page

8. When the programming is complete, click the Low-Level View tab and click Load Config.

9



Running the Demo

www.ti.com

 Load the file K16\_66AK2L06\_rev3\_737p28.cfg under RFSDK2\_<latest\_version>.66AK2Lx-Design-Demo-Win-GUI-Configs in the demonstration package.

🙅 DAC3XJ8X GUI	
File Debug Settings Help	
	DAC3XJ8X GUI v1.1
Quick Start DAC3XJ8X Controls	LMK04828 Controls Low Level View Check ALARMS USB Status O Reconnect USB ?
Register Map	Write Data Register Data Transfer Read to Write
Block / Register Name Address	Default Mode Size Value 🔺 x 0
E LMK04828	💀 Choose or Enter Path of File
x000 0x00 x002 0x02	0x 0x Save in: 👔 DAC38J84 🗸 🌀 🌮 🖽 -
x002 0x02 0x02	
x004 0x04	0x Name A Date modified V Type V
x005 0x05	0x K16_66AK2L06_rev3_737p28.cfg 11/3/2015 12:48 CFG File
x006 0x06	0x Recent Places K16_66AK2L06_rev3_interpx2.cfg 11/3/2015 12:48 CFG File
x00C 0x0C	Ox I I I I I I I I I I I I I I I I I I I
x00E 0x0E	
x100 0x100 x101 0x101	Ox Desktop Ox
x103 0x101	
x104 0x103	
x105 0x105	Ox Libraries
x106 0x106	ox 🔊
x107 0x107	Ox Contraction of the second sec
x108 0x108	Ox Computer
x109 0x109	
x10B 0x10B	
x10C 0x10C x10D 0x10D	
	File name: K16_66AK2L06_rev3_737p28.cfg V OK
Register Description	Read Data Generic
	Save as type: Custom Pattern (*.cfg)
	Write Register Read Register
Updated the Tree with register details	

Figure 10. Low-Level View to Load Registers



For the SerDes configuration for the 66AK2L06, see Figure 11.

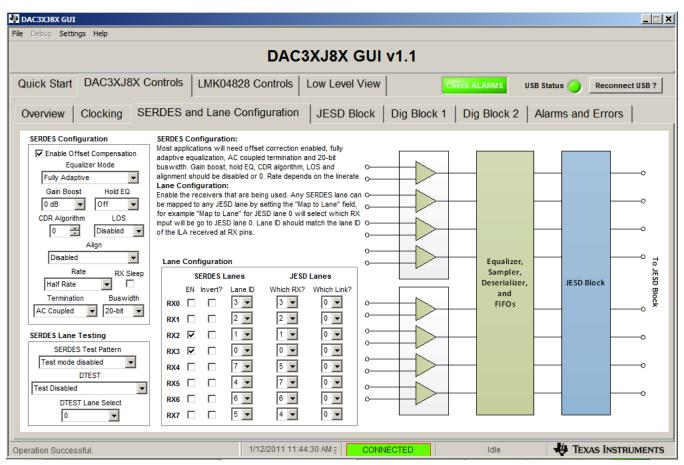


Figure 11. DAC38J8x GUI SERDES Lane Configuration

The course mixer of fs/4 is enabled, shifting the signal to 184.32 MHz. Refer to Figure 12.



Running the Demo

www.ti.com

Debug Settings Help			
	DAC3XJ	8X GUI v1.1	
uick Start DAC3XJ8X Contr	ols LMK04828 Controls Low I	Level View Check ALARMS	USB Status 🧿 Reconnect USB ?
Overview Clocking SERDI	ES and Lane Configuration   JE	SD Block Dig Block 1 Dig Bloc	ck 2 Alarms and Errors
Coarse Mixer Mixer Block EN ✓ Coarse Mixer Select Mixer Gain state of the select Mixer Gain 0 dB ✓ Quick NCO Configuration First enable the mixer block and choose "Bypass" for the coarse mixer. Enable the NCO below and enter the DAC output rate, desired frequency, and desired phase for each complex data path. Then, choose the desired SYNC source. The AB and CD mixers must be sync'd before the NCO accumulator is sync'd. Finally, click "Update NCO" and trigger a SYNC event.	Hap JESD Output to DIG Block Input	Interpolation 2	To QMC EN + → + + Phase AB + → + + Phase AB 1024 - Gain B
NCO Enable DAC Output Rate (SPS) 0 Frequency (Hz) Phase (deg) AB 0 0 CD 0 Update NCO	SYNC Sources  Perform SIF SYNC SIF SYNC Auto SYNC JESD SYNC UMC PA PA Pot SIF SYNC V V V V V V V V V V V V V V V V V V V	EN 64 Samples V /2 V	r. The Frequency AB Phase AB

Figure 12. DAC38J8x GUI Course Mixer Setting



#### 3.1.4 ADC12J4000 GUI

- 1. Start the ADC12J4000 GUI (Start  $\rightarrow$  All Programs  $\rightarrow$  Texas Instruments ADCs  $\rightarrow$  ADC12J4000EVM GUI).
  - (a) Ensure that the USB status is green. If the GUI does not connect to the board, click Reconnect FTDI until the green USB Status LED indicates a connection.
  - (b) You may need to close the GUI for the DAC38J84 for the ADC12J4000 to work.
- 2. Set the clock source to External and set External Fs to 2949.12 MHz.
- 3. Set the mode to Decimate-by-8; DDR; P54
- 4. Click Program Clocks and ADC.
- 5. With the ADC12J4000\_DB8\_DDR\_P54.cfg file replaced according to Section 2.3.2, the default configuration is best for this setup.

ADC1	2J4000EVM G	UI							
File Deb	ug Settings	Help							
			ADC	12J40	DOEVM	GUI v1.3			
EVM	Control	JESD204B / DD	C NCO Configu	ration Ba	nk Correct	Low Level View		USB Status 🥥	Reconnect FTDI ?
#1. ( #2a #2b 294 #3.	Program Clo p Sensor: 1234000 Temp ent Temp	Selection Msps selection MHz nd Serial Data Mode	is programmed, the oth 1. User Inputs - How to #1. Clock Source - the I is selected, choose the #2a. On-board Fs Select DEVCLK, as well as pr #2b. External Fs Select Users Guide for details #3. Decimation and Se in the future. #4. Program Clocks an LMK04828, and ADC12	er tabs allow ti program the E DEVCLK to the Fs at #2a. If th ttion - The LMX ovide the clock ion - The user in regarding exter rial Data Mode d ADC - once a J4000.	Nu clocks and / ADC may be su e external clock 2581 will be pro- for distribution in must provide thi must provide the - Choose the di Il modes have	DC12J4000: pplied by the on-board I (is selected, enter the F ogrammed to provide an ia the LMK04828 for the external Fs supplied (i	LMX2581 or ext is at #2b. ny of the availab JESD204B clo n MHz). The LM rial data mode is button to writ	ernally by the user. le sampling clock fr ccks. IX2581 will be powe for the ADC. More o	If the on-board clock requencies to the ered down; see the options will be added
Updated	I the Tree with	register details 1/12	2/2011 11:44:30 AM	Build:	CO	NNECTED	Idle	TEX	kas Instruments

Figure 13. ADC12J4000EVM GUI Start Page

#### To view the JESD204B / DDC tab on the ADC12J4000 GUI, see Figure 14.

**NOTE:** While the data is in two's complement format and SYNC~ is differential, the corresponding status indicators on the GUI may reflect incorrect values.

							_ <u> </u>		
EVM Control JESD204B /	DDC	NCO Configuration	Bank Corre		Low Level View	USB Status	Reconnect FTDI ?		
1. JESD204B Clock Control: Enable SYSREF Receiver Enable SYSREF Process SYSREF DC-coupled Delay SYSREF Clear SYSREF Edge Detecte Clear SYSREF Edge Detecte Clear Dirty SYSREF Detected Dirty SYSREF Detected		ESD204B Block Control: JESD Block Enable Scrambler Enable 1 Frames per UT 20 31 10 20 31 10 20 31 10 20 31 SNNC- Select SD Test Mode Normal Operation	the AD 1. JES DEVCI 2. JES 3. The allows	D204 LK. D204 DDC all th	4000. B Clock Control can be u B Block Control can be u has various decimation e converted samples at	V4B control block and clocks, used to configure various asp used to configure multiframes options. Bypass Mode (DDC the output. to single or dual data rate.	ects of the SYSREF and , and test modes.		
3. Digital Down-Converter: Decimation Mode Bypass Mode (DDC OFF) Output Sample Format Signed 2's complement OdB Final Filter Gain	P	DDR Serial Data Rate re-emphasis Strength					Texas Instruments		

Figure 14. ADC12J4000EVM GUI -- JESD204B



15

#### 3.2 Starting the Demonstration on 66AK2L06 EVM

- 1. Connect a terminal program (for example, Tera Term) to the 66AK2L06 EVM Linux COM port and login as the root user.
- 2. Determine the IP address assigned to the board using ifconfig. See Figure 15.

root@k21-evm:~# ifconfig
eth0 Link encap:Etȟernet HWaddr 08:00:28:32:BA:5C
inet addr:128.247.121.3 Bcast:0.0.0.0 Mask:255.255.254.0
inet6
UP BROADCAST RUNNING MULTICAST MTU:1500 Metric:1
RX packets:11519 errors:0 dropped:0 overruns:0 frame:0
TX packets:13 errors:0 dropped:0 overruns:0 carrier:0
collisions:0 txqueuelen:1000
RX bytes:910369 (889.0 KiB) TX bytes:1679 (1.6 KiB)

Figure 15. Querying the Board IP Address

- 3. Type "touch /tmp/rfsdk\_stubbed\_afe" in the 66AK2L06 Linux terminal. This requires running a loop back test with ADC and DAC, but not when JESDlpbk configuration is selected.
- 4. Open a browser and navigate to <EVM\_IP\_ADDRESS>:8080. To view the RFSDK Web GUI, see Figure 16.
- 5. Press "Wideband ADC12J4000 and DAC38J84 Demo".

## RFSDK v2.0

TCI6630K2L / 66AK2L06 Release 02.00.05.00 <u>User Guide</u> / <u>Installation Guide</u> / <u>Release Notes</u>

Demos: Small Cell Demo - Using AFE75xx Wideband ADC12J4000 and DAC38J84 Demo High IF Sampling Receiver ADC14X250 Demo

NOTE: When changing from one demo to a different demo, the target board configuration file link (located at /etc/radio/board/default) must be updated to point to the corresponding demo config file and then the K2L EVM must be rebooted.



#### Figure 16. RFSDK Web GUI

6. The web GUI will navigate to the RFSDK v2.0 ADC12J4000 and DAC38J84 Demo Mode.



- 7. Press the Select button once the reset is completed to bring up the Radio Configuration Selection dialog as shown in Figure 17.
- 8. Select a configuration from 1×1-2xLTE75-HC-JESD121121x-DEMO1 or 1×1-2xLTE75-HC-JESD121121x-JESD1pbk. Press "Select".

Name S	Selec	t a Radio	Config	uration		
THE OTHER	Ix1-2xLTE7 Normal Cor	75-HC-JESD121121x-	DEMO1 🔻			EMO1
BB Ch Comb	I <mark>x1-2xLTE</mark> 7 JESD Loop	75-HC-JESD121121x-				
JESD Inte	x1-2xLTE	75-HC-JESD121121x-	JESDlpbk		RFSDK_JESD_368P64	
Radio Stat	tus	READY	Play	yback Status	Not Started (or radio is	s not on)
Radio Co TX Data		Radio Init	MHz +2MHz •		-92.16 240 Tones (75MHz BW)	Load

#### Figure 17. Radio Configuration Selection

 In "Radio Control", press "Radio Init", "Load Playback", and "On" buttons in sequence to start the playback demonstration. (The status of playback should change to Started/Alive [this indicates the test is running]).



Click the AxC0 drop-down menu and select "Fs=92.16 2 tones, -1 MHz and +2 MHz", "Fs=92.16 2 tones, -2 MHz and +4 MHz" or "Fs=92.16 240 tones(75MHz BW)". This loads the selected signal patterns into the corresponding transmit buffers. Click the "load" button. The test patterns can be changed without having to stop the test.

Name		R	efresh Status	Status		
RFSDK Software	Revision			02.00.05.00		
Radio Configura	ion		Select	1x1-2xLTE75-HC-JESD121121x-	DEMO1	
BB Channel Sam	pling Rate			RFSDK_SAMPLE_RATE_92P16MF	ΗZ	
Combined Strea	m Sampling Rate			368.64		
JESD Interface Ra	ite	RFSDK_JESD_368P64				
Radio Status	ON	Playback	Status	us Started/Alive		
Radio Control	Radio Init	Load Playback	On	Off Reset		
TX Data AxC	Fs=92.16 2 tones -1MH:	z +2MHz ▼	AxC1 Fs=92	2.16 240 Tones (75MHz BW) 🔻	Load	
			zero Fs=92	2.16 2 tones -1 MHz +2 MHz 2.16 2 tones -2 MHz +4 MHz		

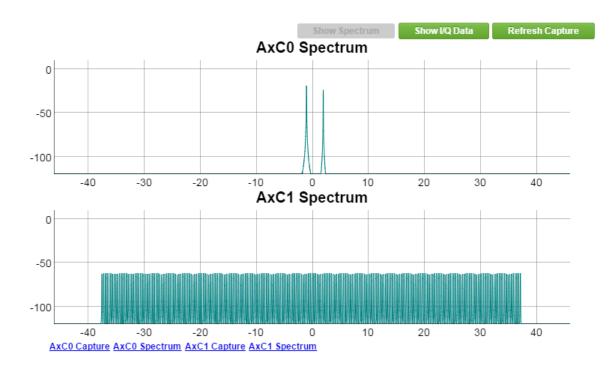


Figure 18. Loading Test Patterns



11. Navigate to the "TX Signal Capture @ DSP" page and press "Refresh Capture". This sends a request to the DSP to perform a signal capture of the Baseband data on the TX side (that is, before the signal data is sent to the digital front-end).

## TX Signal Capture @ DSP (4k FFT, Hanning)



#### Figure 19. TX Signal Capture at DSP

Figure 19 shows that different test patterns are transmitted on both of the carriers. The first carrier is transmitting a 2-tone test pattern with the tones centered at -1 MHz and 2 MHz, respectively. The second carrier is set up to transmit 240 tones spread across a 75-MHz bandwidth.



12. Navigate to the "RX Signal Capture @ DSP" page and press "Refresh Capture". This sends a request to the DSP to perform a signal capture of the baseband data on the RX side (that is, after it has been looped back from the DAC38J84 to the ADC12J4000 and after being down-converted and filtered by the DFE). As shown in Figure 20, the test patterns transmitted on the respective carriers are recovered at the DSP after DAC to ADC loopback.

## RX Signal Capture @ DSP (4k FFT, Hanning)

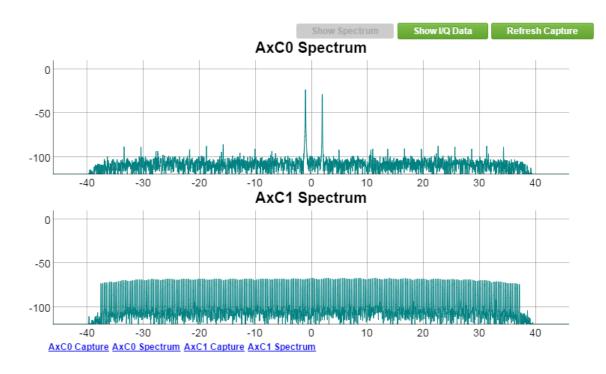
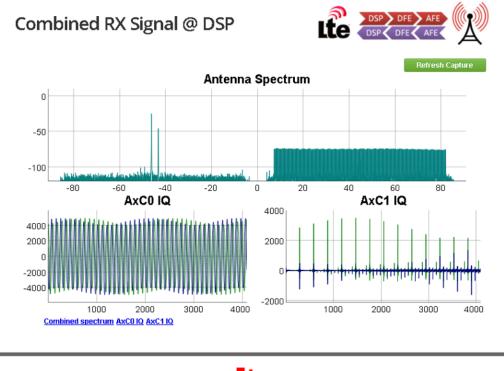


Figure 20. RX Signal Capture at DSP



For an alternative view of the combined RX spectrum from both carriers, go to the "Combined RX Signal Capture @ DSP" page as shown in Figure 21.



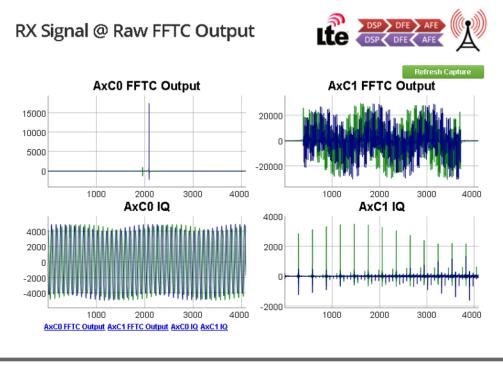
This data is not refreshed automatically.



Figure 21. Combined RX Signal Capture at DSP



13. The RX captured data can be picked up by FFTC co-processor and display as shown in Figure 22.



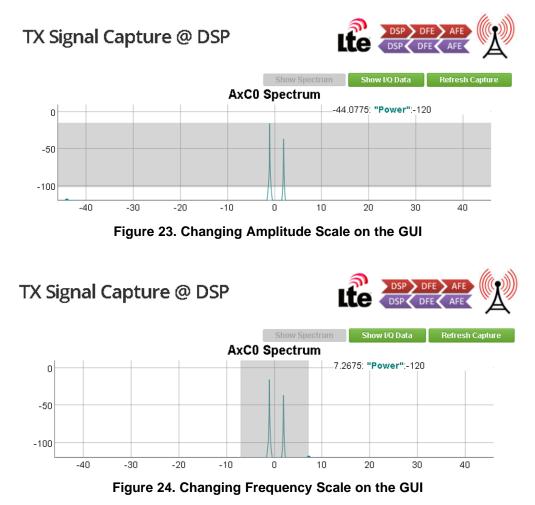
This data is not refreshed automatically.

🔱 Texas Instruments





14. Drag the mouse to zoom in on the graphs both vertically (to change the amplitude scale) and horizontally (to change the frequency scale) as shown in Figure 23 and Figure 24.



15. To stop the test, press the "Off" and "Reset" buttons on the Status-Control page.

#### 4 Test and Debug

For a first-time setup, TI recommends using a spectrum analyzer to check the DAC38J8x output . For the 2-tone output and 75-MHz output, see Figure 25 and Figure 26.

Agilent Spectrum Analyzer - Swept SA												
LXI		RF 50 s			SENS	6E:INT	AL	IGN AUTO				3 PM Sep 16, 2015
Cent	ter Frec	184.32	0000 MHz	PNO: Fa IFGain:Lo		Trig: Free Atten: 10 d		Аvg Туре	: Log	g-Pwr	אד ר	ACE 123456 TYPE WWWWWWW DET N N N N N N
10 dB Log r	/div R	ef 0.00 d	IBm				1					
-10.0 -												
-20.0 -										I		
-30.0 -												
-40.0												
-40.0												
-60.0 -												
-70.0										1		
-80.0												
-90.0					<b>                                    </b>		 			╽╷╷	<mark>t¦₽₽₽₩₽₽₽₽</mark> ₩₩ Iv I v v Ive	
	er 184.3 BW 100				#VBW 2	200 kHz				Sweep		200.0 MHz (1001 pts)
MSG								STATUS				

Figure 25. DAC Output – 2×75 MHz 2-Tone Data



Test and Debug

www.ti.com

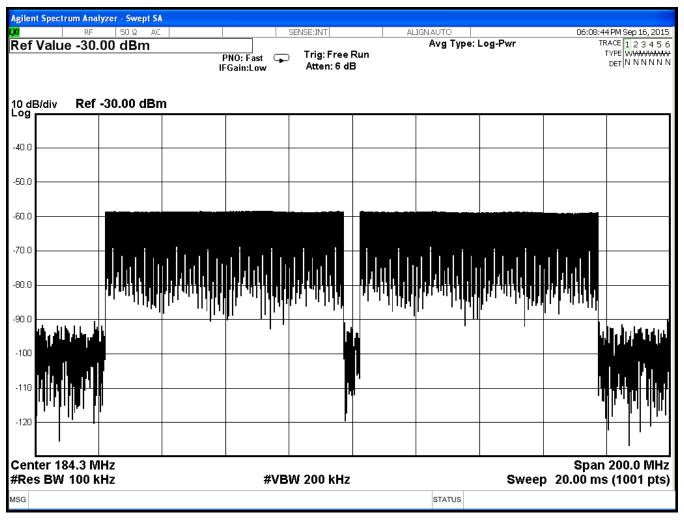


Figure 26. DAC Output -- 2×75 MHz Multi-Tone Data

Test and Debug

The DAC38J8x EVM output is a real image and has the image in the second Nyquist zone. This image will be visible without the filter. To view the DAC output, see Figure 27.

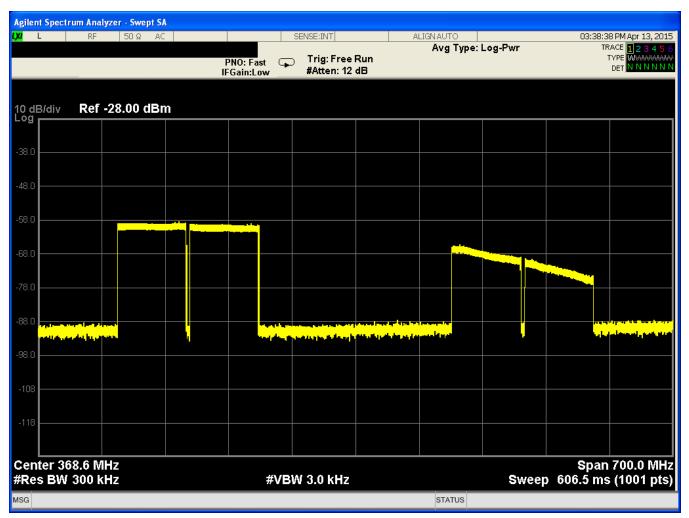


Figure 27. DAC Output -- 2×75 MHz Signal With its Image With no Filter Installed



#### Test and Debug

When the DC-264 MHz low-pass filter is used, the image is filtered out. About 1-dB suppression exists at the high end of the band because the signal span is from 103.32 MHz to 265.32 MHz for 2x75 MHz. To view how the low-pass filter filters out the image, see Figure 28.

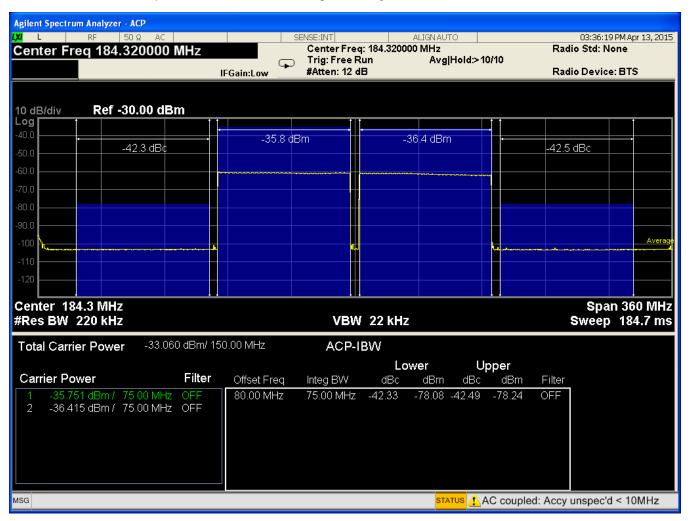


Figure 28. 2×75 MHz DAC Output with DC-264 Low Pass Filter

By default, the output power of the 2xLTE60 is –24 dBm. The adjacent channel power ratio is –58.7 dBc for the high side. The low side crosses DC and is unable to provide an accurate ACP measurement. To view the 2xLTE60 ACP test, see Figure 29.

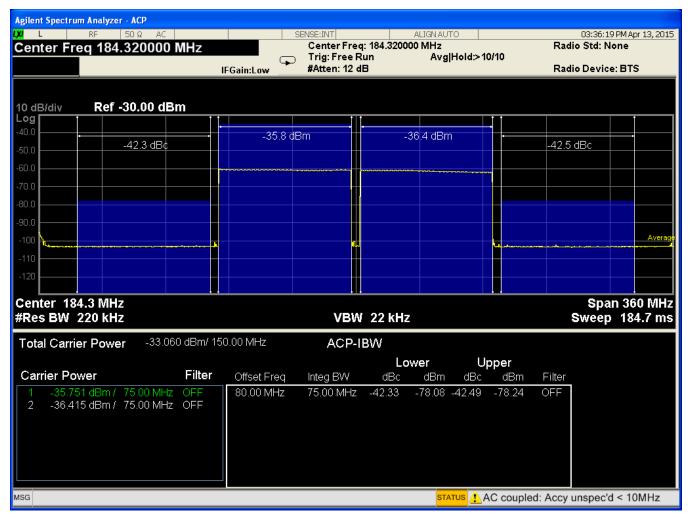


Figure 29. 2×75 MHz Data: Adjacent Channel Power Ratio Test

#### 5 References

Refer to the following links for more information related to the hardware and software components in this demonstration:

66AK2L06 EVM

ADC12J4000 EVM

DAC38J84 EVM:

Keystone-II MCSDK User Guide

Keystone-II Architecture DFE User Guide



Revision B History

www.ti.com

#### **Revision B History**

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

#### Changes from A Revision (November 2015) to B Revision

Page

•	Changed the directory structure	2
•	Changed from 3.01.02.05	5
•	Changed from 3.01.02.05	5
•	Changed from 3.01.02.05	5
•	Changed from mcsdk312	5
•	Changed from mcsdk312	5
•	Changed structure and file names in Demo package description	6
•	Changed file name from "66AK2Lx-Design- Demo_Win_GUI_RFSDK_ <latest_version>-DEMO1_<latest_version>.zip"</latest_version></latest_version>	6
•	Deleted K2L-HSP FMC Adapter and note	
•	Changed Figure 5	7
•	Changed file name from "66AK2Lx-Design-Demo_Win_GUI_RFSDK_ <latest_version>-DEMO1_<latest_version>"</latest_version></latest_version>	7
•	Changed Figure 6	7
•	Changed Figure 7	8
•	Changed from "div 5" to "div 4"	8
•	Changed from "PLL2 LOCK and LMK LOCK LED"	8
•	Changed Figure 8	8
•	Changed location name from "666AK2Lx-Design-Demo_Win_GUI_RFSDK_02.00.00.11-DEMO1_01.01"	10
•	Changed the procedure on how to start the 66AK2L06 EVM demonstration	15
•	Changed Figure 16	15
•	Changed Figure 17	16
•	Deleted DEMO 1–Status and Control	17
•	Changed Figure 18	17
•	Changed Figure 19	18
•	Changed Figure 20	19
•	Changed Figure 21	20
•	Added Figure 22: FFTC Output	21
•	Changed Figure 23	22
•	Changed Figure 24	22



#### **Revision A History**

#### Changes from Original (April 2015) to A Revision

Page

•	Changed how "Sync In" and "Sync Out" appear in the system block diagram	1
•	Changed from K16_Lamarr_rev3_737p28.cfg to 66AK2L06_dac737p28.cfg	7
•	Updated Image GUI-Load CFG	7
•	Updated Image RFSDK Web GUI	15
•	Updated Image Radio Configuration Selection	16
•	Updated Image DEMO1 - Loading Test Patterns	17
•	Updated Image TX Signal Capture at DSP	18
•	Updated Image RX Signal Capture at DSP	19
•	Updated Image Combined RX Signal Capture at DSP	
•	Updated Image Changing Amplitude Scale on the GUI	
•	Updated Image Changing Frequency Scale on the GUI	22
•	Updated Image DAC Output – 2x75 MHz 2-Tone Data	23
•	Updated Image DAC Output 2×75 MHz Multi-Tone Data	24
•	Updated Image DAC Output 2x75 MHz Signal With its Image With no Filter Installed	
•	Updated Image 2x75 MHz DAC Output with DC-264 Low Pass Filter	26
•	Updated Image 2x75 MHz Data: Adjacent Channel Power Ratio Test	

#### **IMPORTANT NOTICE**

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products Audio Amplifiers Data Converters DLP® Products	www.ti.com/audio amplifier.ti.com dataconverter.ti.com www.dlp.com	Applications Automotive and Transportation Communications and Telecom Computers and Peripherals Consumer Electronics	www.ti.com/automotive www.ti.com/communications www.ti.com/computers www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	TI E2E Community	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconne	ctivity	

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2016, Texas Instruments Incorporated